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# Ceramic substrates for high voltage power electronics: past, present and future

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**Abstract**—In the present work, we report a review of the ceramic substrate technologies used for high voltage power electronics modules is detailed. These technologies will be confronted with the different challenges undertaken to improve the properties of the ceramic substrate, from thermal, mechanical and dielectric performance point of view. We describe some of the current developments on the design of substrate both from the architecture and from the material points of view. In particular, a new strategy on the design and realization of a ceramic substrate based on aluminum nitride is presented.

**Keywords**—Power modules, high voltage packaging, ceramic substrates, field grading strategies

## I. INTRODUCTION

The use of ceramic substrates in power electronics dates from the 1990's, where significant developments of the modular technology arise in medium and high power modules [1]. In this “module” (Figure 1) the ceramic has two main roles, the first concerns the electrical insulation of electronic circuit that hosts mainly the active semiconductor device(s), while second permits the heat extraction due the power losses within the active devices.

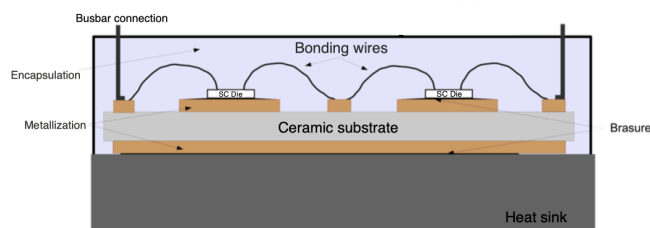


Fig. 1. Power module schematic showing the ceramic substrate

Other than their electrical insulation capabilities, the main reason to use ceramic substrates is to take advantage of their exceptional thermal properties that grant them thermal conductivities up to 200 W/m-K (Table 1, thermal properties of ceramics). Along with the ceramics, different technologies became available with varying metallization types and methods that enabled their use in a wide variety of circuit designs, from planar technology [2] to more integrated

approaches, such as bump-type stacked 3D packaging [3]. This couple ceramic-metallization is often referred as ceramic substrate.

TABLE I. THERMAL CONDUCTIVITIES OF COMMON CERAMICS USED IN POWER MODULE PACKAGING [4].

Ceramic substrate	Thermal conductivity (W/m-K) (typical values)
$\text{Al}_2\text{O}_3$	30-40
$\text{Si}_3\text{N}_4$	35-60
AlN	140-200

As the power module architecture gets more and more adopted in power electronics, especially for the high power range, the ceramic substrate remains the first choice for insulating the high voltage and allowing the cooling of the module package.

The type of applications may vary, but one constant is the use of high voltage ( $> 600$  V), and high current semiconductors, such as IGBT's or MOSFET's, which require, in a multi-chip packaging, high thermal power dissipation and electrical isolation. The purpose of this paper is to provide an overview on the main characteristics of the ceramic substrates and how they are taken into account when selecting them for high voltage and/or high power electronic modules. Recent progress and perspective approaches in the development of future ceramic substrates for high voltage applications are presented as well.

## II. DEVELOPMENT OF CERAMIC SUBSTRATE TECHNOLOGIES

One of the main concerns when developing the ceramic substrates is the thermo-mechanical constraint that the metallization imposed to the ceramic. Indeed, ceramic materials have very different coefficient of thermal expansion compared to most of the metallization materials. One of the first ceramic-metal couples used in power modules is the alumina ( $\text{Al}_2\text{O}_3$ ) with direct bonded copper (DBC). DBC technology relies in particular on the bonding of copper to alumina by the inter-diffusion of copper oxide (at the surface of copper) with the alumina to form a very specific copper aluminate ( $\text{CuAl}_2\text{O}_3$ ) at  $1065^\circ\text{C}$  [5]. This

bonding method was subsequently applied to aluminum nitride (AlN), using a slight oxidation of AlN to have also form a Al<sub>2</sub>O<sub>3</sub>-CuO bonding. Besides DBC, it is also possible to bond the ceramic with a metal using a brazing alloy (typically Ti or Ag-based) through a method known as Active Metal Brazing (AMB) [6], [7].

This metal-ceramic couple has its drawbacks, especially when submitted to thermal cycling. If the amplitude of the latter is large enough, there can be work hardening of the metal (Fig. 2) [8], [9]. Moreover, if the bending strength of the ceramic is surpassed, the metal ‘pulls’ and breaks the ceramic arising, in most of the times in a conchoidal fracture (Figure 2). Mechanical properties of ceramics and metals for the current ceramic substrate technologies are shown in Table 2.

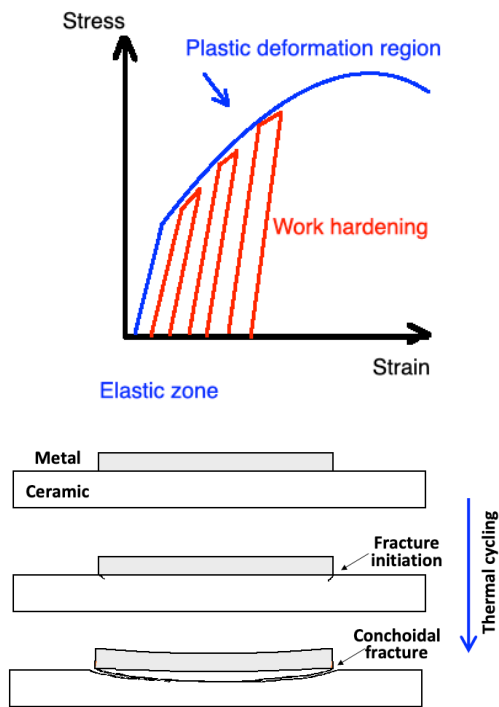


Fig. 2. Schematics of the work hardening undergone by the metallization and for a conchoidal fracture in the ceramic.

TABLE II. TYPICAL THERMO-MECHANICAL PROPERTIES OF THE CERAMICS AND METALS COMMONLY USED IN THE CERAMIC SUBSTRATE TECHNOLOGIES (AT ROOM TEMPERATURE)

Material	Thermal expansion coefficient $\mu\text{m}/\text{m}\cdot\text{K}$	Elastic limit (MPa)	Bending strength (MPa)	Elastic modulus (GPa)	Yield stress (MPa)
Al <sub>2</sub> O <sub>3</sub>	6,7	1	400	370	2
AlN	4,2	3	270	330	4
Si <sub>3</sub> N <sub>4</sub>	2,8	5	900	320	6
Cu	16	70	7	110	300
Al	24	28	8	70	76

Thus, if for a given application thermal cycling is a major concern, like e.g. in aeronautical applications, with medium power dissipation needs, the natural choice will be to use the most mechanically resistant ceramic (Si<sub>3</sub>N<sub>4</sub>) with copper[10], [11]. On the other hand, if thermal exchange requirement limits the choice to AlN ceramic, and the thermal cycling is a concern as well, metallization with aluminum (Al) could improve the cycling performance, compared with DBC.

In current applications, there is no doubt that AlN offers the best thermal performance of all available substrates. However, one must take into account evolution of the thermal conductivity with the temperature if wideband semiconductors such as SiC are intended to be used at high temperature. In Fig. 3 there is the negative temperature dependency of the thermal conductivity of an AlN commercial substrate.

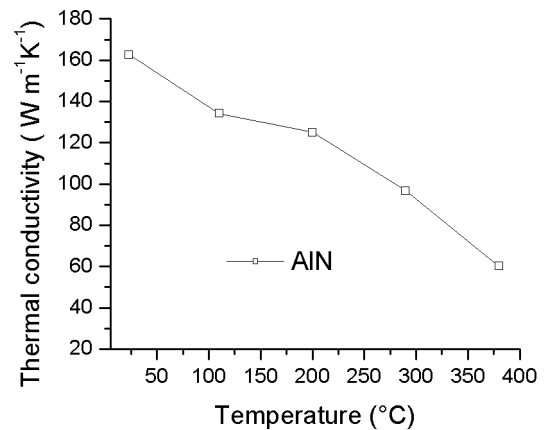


Fig. 3. Measured thermal conductivity of a commercial AlN ceramic used for fabricating DBC or AMB substrates (thickness = 1 mm). Measurements performed by the “hot-disk” method.

These ceramic substrates are intended to address applications of temperature of approximately 200°C, but in all cases the limit will be tied to the thermal and chemical stability of the metal-ceramic bonding. It could be possible to use a refractory metal (tungsten or molybdenum) to extend the operating range of the metallization [12]. Also in a prospective approach [13], it could be even possible to replace the metallization by another ceramic, with the final aim to extend their compatibility to match high temperature semiconductor devices as future diamond ones (Fig. 4).

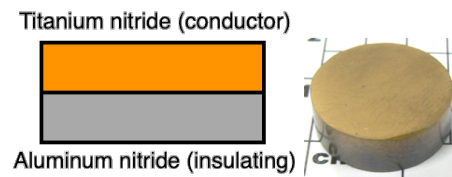


Fig. 4. All-ceramic substrate made by titanium nitride co-sintered with aluminum nitride.

### III. DIELECTRIC PROPERTIES AS A DIMENSIONING FACTOR

Beside the thermo-mechanical considerations, one major dimensioning parameters for the ceramics substrates is its dielectric performance. This is their ability to withstand the electrical constraints derived from the applied voltage (i.e. their breakdown field), and to keep the stability of their dielectric properties (permittivity and losses). The dielectric permittivity of the ceramic plays a major role when using

fast switching devices, as the substrate participates to the common mode capacitance of the circuit [14].

As well as other properties, dielectric breakdown strength largely depends on the temperature (Fig. 5). We have previously identified that AlN ceramics can depict very different behaviors depending on the elaboration parameters. This can be related in great measure to the final microstructure of the ceramics [4].

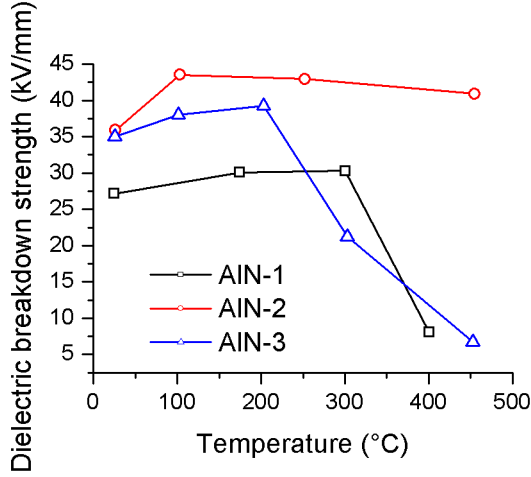


Fig. 5. Dielectric breakdown of three commercial AlN ceramics (thickness = 1 mm) (AIN-1 and AIN-2 values extracted from ref. [4]).

Beside the intrinsic properties, other characteristics can also play a significant role in the selection of well-suited ceramic substrate technology, such as surface resistivity and surface breakdown voltage, that will limit the distance between two metallic paths in the final substrate layout.

#### IV. CHALLENGES WHEN INCREASING THE VOLTAGE IN POWER MODULES

The ceramic substrate must withstand at least the full blocking voltage of the power module, however, other insulating materials, are also constrained by the voltage and electric field, such as the passivation and encapsulation. Moreover, owing to the geometry of the system, there are regions that are subjected to non-homogeneous electrical fields. Other than the immediate vicinity of the semiconductor, electrical fields can be very high at the edges of the metallization, at the triple point that joins the metal, the encapsulation and the ceramic. In addition to the dielectric breakdown, the field reinforcement at the triple point can induce different types of extrinsic phenomena, such as acting as active sites for partial discharge activity, treeing and ultimate breakdown of one of the insulators. In current applications (3.3 kV power modules), when care is taken in the design and the choice of materials, it is possible to withstand the electric fields at these triple points (Figure 6).

In the near future, as SiC components will be available reaching past the 10 kV mark, the constraints will be much higher in terms of the electric field. Consequently, the insulating materials will not be able to withstand such level of electrical constraints, thereby requiring either the application of electric field grading strategies, or the development of insulating materials possessing larger intrinsic resistance.

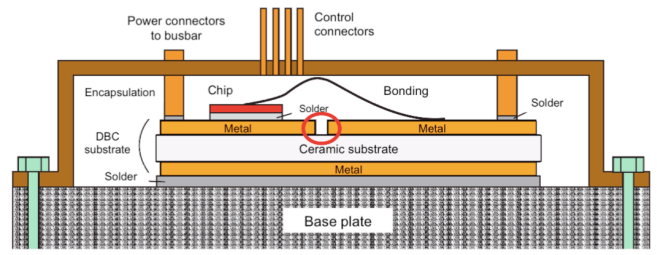


Fig. 6. Schematic of a power module. The circle shows the triple points at the metallization tracks edges.

#### A. Management of field reinforcement in the encapsulation.

There are several electric field grading strategies that can be applied for attenuating the electric field peak or its impact on the insulation materials at the triple point. Most of the solutions that are proposed for this, address the following:

- Modifying the tracks geometry, for example optimizing the metallization edges [15], or burying the tracks in the substrate [16] or raising the metallization with a rounded geometry [17].
- Enhancing the intrinsic dielectric breakdown strength or partial discharge resistance of the encapsulation materials, by either changing the nature of the polymers or using (micro or nano) composite materials [18], [19].
- Using resistive coatings based on hydrogenated amorphous silicon (a-Si:H) [20], or non-linear semi-resistive varnishes based on polyimide filled with micro-particles of zinc oxide (ZnO) [21].
- Modifying the electric field distribution through the control of the dielectric properties of the encapsulation, by either the homogeneous addition of high permittivity composites [22], or tailoring them to address only the regions where the electric field is higher [23] (Figure 7).

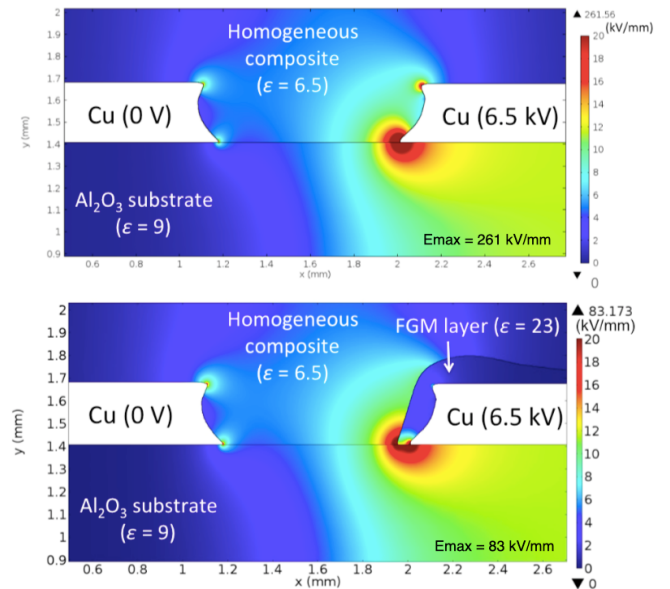


Fig. 7. FEM simulations evidencing the impact of a Functionally Graded Material FGM (layer of high permittivity near the high voltage electrode) on the maximum electric field area.  $E_{max}$  # 260 kV/mm without (top plot.), resp. 83 kV/mm with FGM (bottom plot.). [23].

All the strategies described above deal with the issue of reducing the impact of the electrical field constraint at the triple point by modifying the encapsulation.

Another possibility is to address the electrical field reinforcement by modifying the ceramic material itself.

**B. Management of field reinforcement in the ceramic substrate.**

*a) Mesa structure at the ceramic.* This proposal is inspired from what is done in semiconductor devices to modify the electric field configuration. It implies creating a protruding ceramic volume (mesa) that changes the angle and geometrical configuration of the triple point [24](Fig. 8).

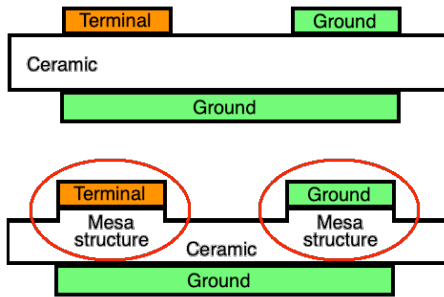


Fig. 8. Scheme of ‘mesa’ structures on a ceramic substrate.

Depending on the mesa height and lateral clearance dimensions, it is possible to effectively reduce the electrical field reinforcement at the triple point (Fig. 9)

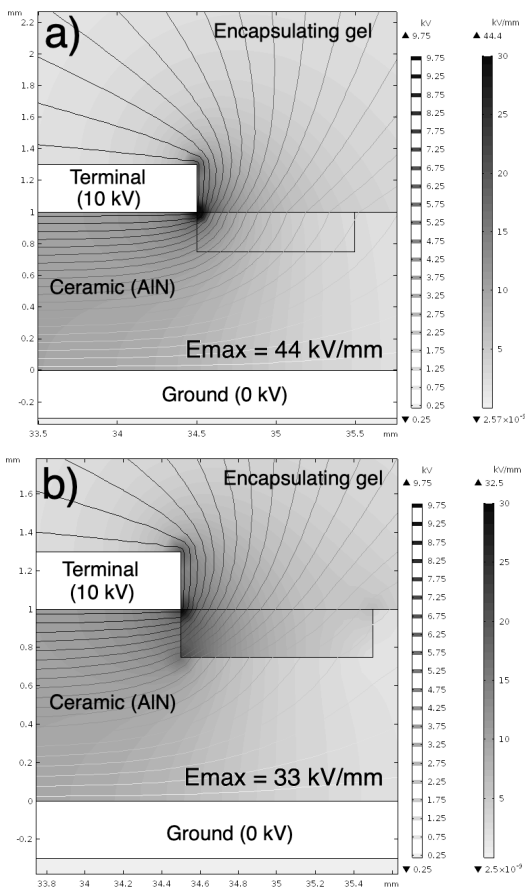


Fig. 9. FEM simulations illustrating the impact of a mesa structure on the maximum electric field of a ceramic substrate. To maintain a constant mesh, domains must be defined prior simulation, changing only the

dielectric properties to match a) a standard ceramic structure or b) a substrate with a mesa structure (simulated potential difference between electrodes = 10 kV).

One of the key parameters when making the mesa structure is to keep the alignment and verticality at the edge of the ceramic and copper metallization. This has been accomplished by making an ultrasonic machining of the ceramic substrate with metallization (Figure 10).

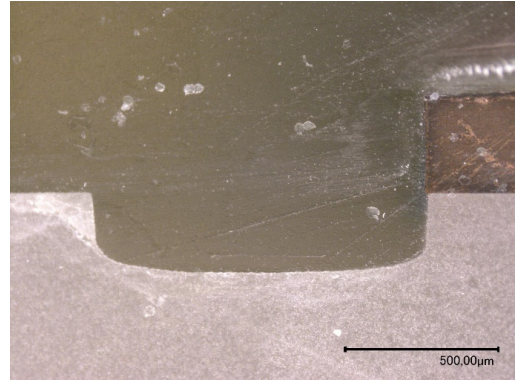


Fig. 10. Mesa structure realized in a DBC (AlN) of 1 mm thickness.

So far, the field grading strategies implied the use of the ceramic substrate ‘as it is’ considering a single homogeneous material and the strategies to alleviate the triple point electric field reinforcement came either from what is done in the encapsulation (volume or surface) or from the modification of the geometry of the triple point. In this last section, we present a novel strategy that consists in modifying the properties in the volume of the ceramic material.

*b) Field grading substrate (FGS).* This A ceramic that would integrate directly a B region (or several) of different dielectric properties within its volume would be capable to modify the field configuration at the triple point and in the neighboring volume of the encapsulation.

Fig. 11 presents a schematic of such field grading substrate with the corresponding modified electrical properties regions.

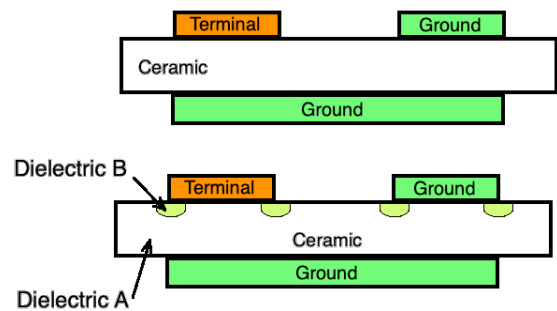


Fig. 11. Scheme of a functionally graded substrate (FGS) that incorporates regions (Dielectric B) of different dielectric properties compared to the ceramic substrate (Dielectric A).

One of the possible approaches is to modify and increase the dielectric losses (or AC conductivity) of a base ceramic, like aluminum nitride.

To our knowledge, this approach has not been reported yet.

In Fig. 12, we present the impact such kind of FGS would have on the electric field distribution when modifying the AlN conductivity by a factor of  $1 \times 10^6$ . The maximum



electric field value is greatly reduced and occurs at the region B edges (away from the triple point area).

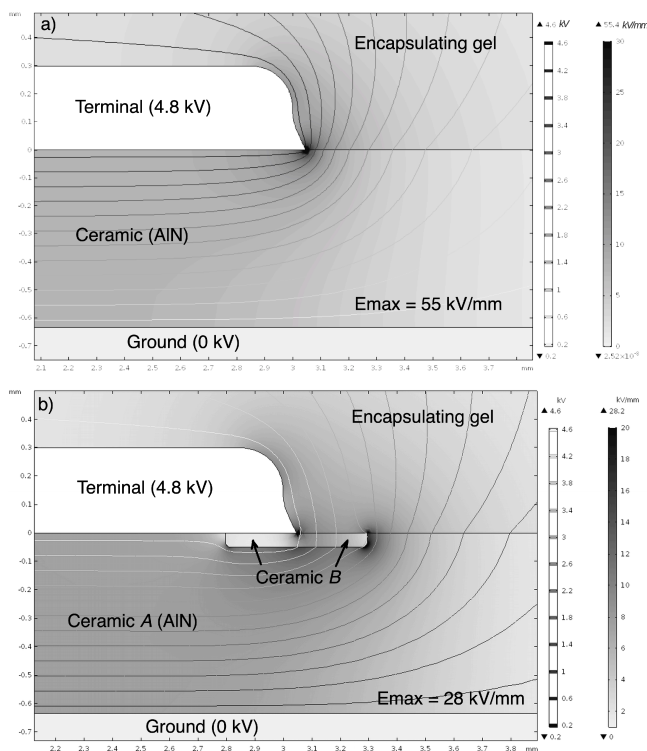


Fig. 12. FEM simulations illustrating the impact of a functionally graded ceramic structure (FGS) on the maximum electric field. a) standard ceramic structure *A* or b) a substrate with a higher conductivity region *B* ( $10^6$  higher than that of AlN ceramic). Simulated difference potential between electrodes = 4.8 kV.

## V. CONCLUSIONS

In this work we presented an overview on the main parameters that must be taken into account when increasing the voltage of power modules that use ceramic substrate technology. When packaging higher voltage semiconductors  $> 6.5$  kV, the consequences will not be only thermo-mechanical, but other problems might arise due to the existing limits of the design rules and the available dielectric materials. New strategies, like electrical field grading, should be applied to reduce the effects of the voltage increase on the insulating materials. A broad range of field grading strategies have been presented, along a new proposal for a field grading ceramic substrate.

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