# GaN-based transistors using buffer-free heterostructures for next generation RF devices

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## INTRODUCTION

Compared to other mainstream technologies, GaN power devices cover wider bandwidth for any given power level, and facilitate smaller system form factors due to their high power density. Higher voltage also results in higher impedance for optimal match, and therefore enables the use of simpler and more compact matching circuits. High breakdown voltage significantly improves ruggedness under load mismatch conditions. That is why, GaN will play a significant role in space and military applications requiring high-frequency and size-constrained small cells. Currently, the 0.15 µm GaN technology is commercialized or being qualified by several industrial players, enabling reliable high power operation up to the Ka band [1]-[2]. Despite the fact that GaN can also dissipate heat better and run hotter more reliably than any other power semiconductor technology to date, heat is still a critical consideration for small cells. As a matter of fact, the self-heating, especially when operating under high power density generally affects the power added efficiency as well as the device reliability[3].Therefore, from a practical point of view, a significant derating in terms of power density and/or drain voltage operation has to be performed in order to maintain a high reliability.
However, for future high frequency applications requiring shorter gate length of 100 nm and below, the electric field peak at the gate vicinity is even higher, resulting in a more pronounced self-heating also at lower drain bias ($V_{DS}$ = 15 V for instance). Although the preferred substrate, SiC, for these types of devices has a high thermal conductivity, it has been shown that the buffer layers including many interfaces generate a high thermal resistance limiting severely the thermal dissipation. In turn, mismatch in phonon density of states at the interfaces between different materials results in a thermal-boundary resistance [4]. On the other hand, the buffer layers are needed in order to screen the charges due to defects, dislocations, and spontaneous/piezoelectric polarization present at the interface with the nucleation layers or the substrate [5][6][7]. Theoretically, a thin nucleation layer with an outstanding quality would be enough to accommodate the growth of high quality GaN HEMTs avoiding the use of a complex stack and thus enhancing significantly the thermal dissipation. Recently, the company SweGaN demonstrated the growth of a buffer-free AlGaN/GaN heterostructure using solely a thin AlN nucleation layer (NL) with a thickness well-below 100 nm [8].

## MATERIAL AND DEVICE PROCESSING

The buffer-free AlGaN/GaN heterostructure was grown by the company SweGaN using a hot-wall metal organic chemical vapor deposition (MOCVD) on 4 in. SiC substrates. The HEMT structure consists of a thin AlN transition layer directly to the undoped 220 nm thick GaN channel, followed by a 14.0 nm $Al_{0.29}Ga_{0.71}N$ barrier layer and a 2 nm cap GaN layer. Thus, the total HEMT thickness is less than 300 nm as can be seen in Fig.1. Hall measurements performed on Van der Pauw patterns reveal a carrier concentration close to $1\times10^{13}$ $cm^{-2}$ with an electron mobility at room temperature above 2100 $cm^2/Vs$, which is comparable to the state-of-the-art transport properties of standard AlGaN/GaN HEMTs [9]. The electron mobility reflects the high material quality with the absence of rough interfaces or defects.

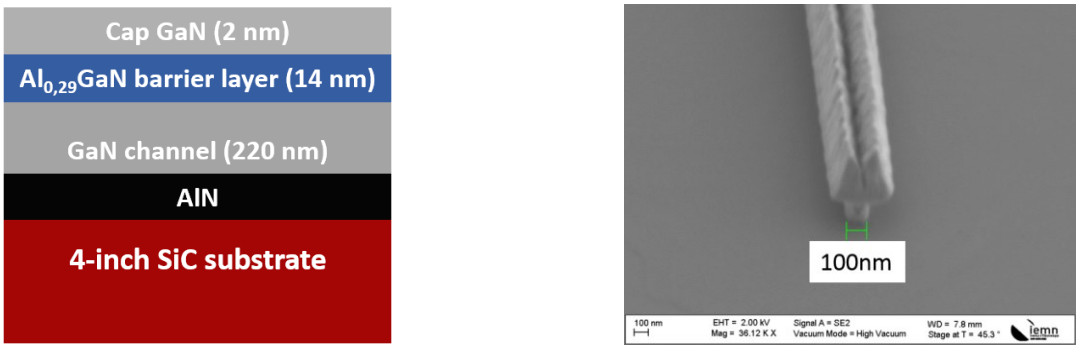


Fig. 1 : Schematic cross section of the AlGaN/GaN buffer-free and a MEB picture of the gate

A Ti/Al/Ni/Au metal stack followed by a rapid thermal annealed has been used to form the ohmic contacts directly on top of the GaN cap. Device isolation was achieved by nitrogen implantation. Ohmic contact resistance ($R_c$) extracted from linear transmission line model (TLM) structures was of 0.75 Ω.mm, which can still be significantly optimized. Then, a 0.10 µm Ni/Au T-gate length was defined by e-beam lithography (see Fig.1). The gate-source and gate-drain spacings were 0.3 and 1.7 µm, respectively, and the device width was 50 µm. Finally, 200 nm PECVD $Si_3N_4$ was deposited as final passivation.

## DC AND SMALL SIGNAL CHARACTERIZATION

The typical I-V characateristics are shown in Fig.2. The gate source voltage was swept from -4V to +2V with a step of 1V. A maximum current drain density ($I_{Dmax}$) of 0.85 A/mm is observed at $V_{DS}$ = 10V and $V_{GS}$=2V, which is in agreement with the carrier concentration. This is combined to an excellent pinch-off and an off-state leakage current of 10 µA/mm. The extrinsic transconductance characteristics at $V_{DS}$ = 6, 8 and 10 V show a peak of 280mS/mm despite non-optimized high ohmic contact resistances.

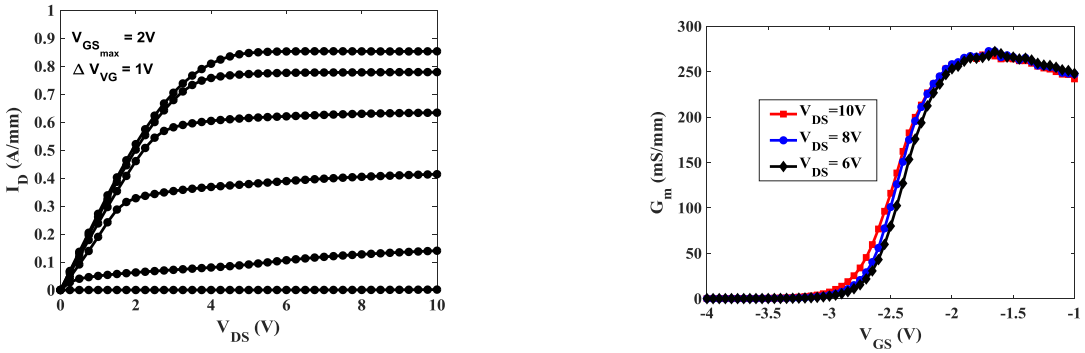


Fig. 2 : DC characteristics of the buffer-free HEMT

At these respective biases, using Rhode and Schwarz ZVA67GHz, the cut-off frequency ($f_T$) and maximum oscillation frequency $f_{max}$ are extracted from the scattering (S) parameters (Fig.3). Good RF performances are achieved with = 57 GHz and $f_{max}$ = 176 GHz, in spite of the unoptimized processing on this new heterostructure.

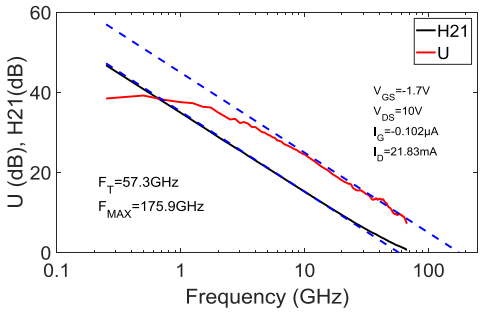


Fig. 3 : Small signal characteristic of 0.1x50µm² devices

Before the final passivation, the breakdown voltage carried out on transistors with different Gate-Drain (GD) distance, increases as expected as a function of the Gate-Drain distance to reach almost 200 V with a GD = 2.7 µm (Fig.4-left).

In order to confirm the high material quality and the absence of parasitic conduction within these epi-layers, a lateral breakdown voltage assessment was performed between two isolated contacts separated by 25 µm showing about 1600V (substrate floating) (Fig.4-right). These results reflect indeed the high quality of the thin AlN transition layer.

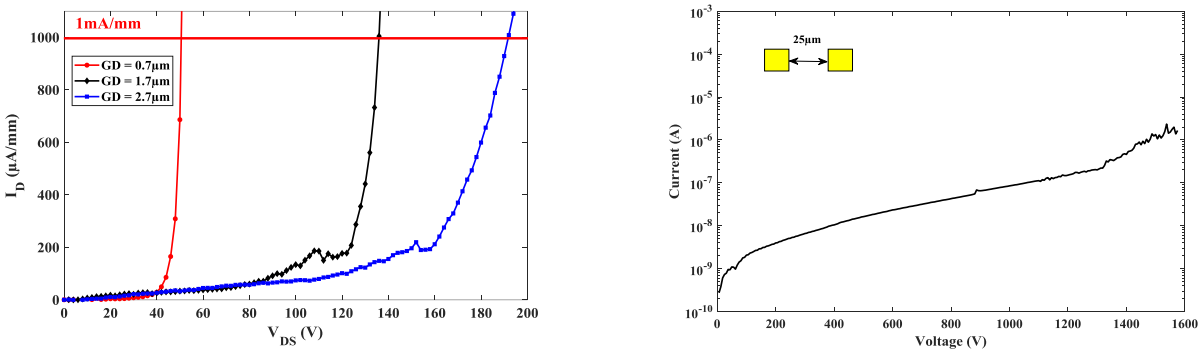


Fig. 4 : Three-terminal off-state breakdown voltage of short transistors with various Gate – Drain distance (left) and lateral buffer breakdown voltage between two isolated contacts separated by 25µm (right)

The trapping effect analysis was performed by pulsed DC measurement using a pulse duration of 1µs with 1% of duty cycle for various quiescent bias point. A reasonable current collapse is observed, highlighting limited trapping effects in this ultrathin heterostructure.

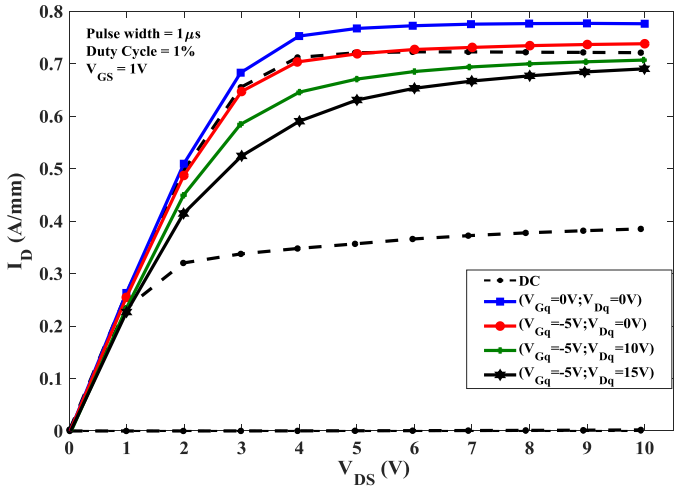


Fig. 5 : Pulsed DC for different quiescent points for 1µs/1%

## CONCLUSION AND PERSPECTIVES

These preliminary results demonstrate the high quality of this novel ultrathin heterostructure despite the absence of thick transition layers as currently used in standard GaN HEMTs. Good RF performances was achieved despite a non-optimized ohmic contact resistances. The obtained frequency performance coupled with the high 3-terminal breakdown voltage (200V) and lateral breakdown voltage prove the potential of this “buffer-free” structure for future millimetre-wave applications. Furthermore, this novel structure shows rather low trapping effects that can certainly be optimized. The trapping level in these intial devices is found to be quite similar to that of standard HEMTs. Future work includes large signal characterizations and thermal analysis.

## ACKNOWLEDGMENT

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