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Scaling of AlN/GaN HEMT for millimeter-wave power applications

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Abstract

In this paper, we report on AlN/GaN HEMTs for high frequency applications. Various gate lengths have been studied as a function of the gate-drain distance in order to analyze the impact on the DC, RF and power performances. Electrical characteristics of this structure for 110 nm gate length show a maximum drain current of 1.2 A/mm, an extrinsic transconductance G_m of 400 mS/mm and a F_T/F_{max} of 63/300 GHz at a drain bias voltage $V_{DS} = 20$ V. An excellent electron confinement with a low leakage current below 10 μ A/mm is achieved. Furthermore, a breakdown voltage of 55 V for GD0.5 and up to 140 V for GD2.5 are observed when using a 110 nm short gate length. Large signal characteristics at 40 GHz reveal a state-of-the-art combination of power added efficiency (PAE) (50%) with an output power density (P_{out}) of 3.6 W/mm at $V_{DS} = 20$ V in continuous wave mode (CW) and PAE of 50% associated with a P_{out} of 8.3 W/mm at 40 V in pulsed mode. It can be noticed that the 110 nm gate length GD0.5 showed no degradation after semi-on robustness tests and large signal measurements up-to $V_{DS} = 20$ V.

Introduction

Gallium Nitride (GaN)-based RF power devices have made substantial progress in the last decade, which will enable new applications such as military wireless communication and SATCOM. Indeed, those applications operating at high frequency need compact systems, for which the power-added-efficiency (PAE) is a critical parameter. That is why, achieving both high PAE and output power density (P_{out}) in the millimetre-wave range represents currently one of the key goals for the GaN technology. High Electron Mobility Transistors (HEMT) on SiC have already demonstrated attractive efficiencies up to Ka band [1]-[3] but limited data have been reported so far in the Q band [4] and above. To obtain very high frequency performance, it is necessary to optimize wisely the structure configuration especially the barrier thickness [5]. In this paper, we used an ultrathin barrier layer and investigated the impact of the gate-drain distance and the gate length with the aim of reaching high RF performances in the Q band and above.

Experimental

The epitaxial layer structure is based on an AlN/GaN heterostructure grown by metal organic chemical vapor deposition (MOCVD) on 4 in. SiC substrates. Figure 1 shows the cross section of the HEMT structure consisting in an AlN transition layer, a C-doped GaN buffer layer followed by a 100 nm GaN channel and a 3.0 nm ultrathin AlN barrier layer. The HEMT was capped with an in-situ SiN layer both as early passivation as well as to reduce trapping effects. Room-temperature Hall measurements showed a high electron sheet concentration of 1.9×10^{13} cm⁻² with a mobility of 965 cm²/Vs. A Ti/Al/Ni/Au metal stack annealed at 850°C

has been used to form the source-drain ohmic contacts directly on top of the barrier by etching the in-situ Si₃N₄ layer. Then, Ni/Au T-gates with various lengths were defined by e-beam lithography. The SiN underneath the gate was fully removed by SF₆ plasma etching through the e-beam lithography. Finally, 200 nm PECVD Si₃N₄ was deposited as final passivation.

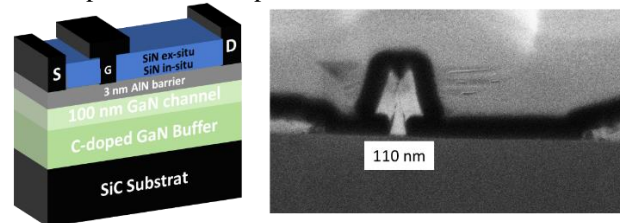


Figure 1. Schematic cross section of the fabricated AlN/GaN-on-SiC HEMTs (left) and FIB view of a 110 nm T-gate (right)

Results and discussion

DC characteristics:

DC measurements have been carried out with a Keysight A2902A static modular and source monitor. Figures 2 and 3 show the output and transfer characteristics as well as the extrinsic transconductance.

The gate source voltage was swept from -4 V to +2 V with a step of 1 V. A maximum drain current I_{Dmax} is about 1.2 A/mm and 1.1 A/mm for GD0.5 = 0.5 μ m and GD1.5 = 1.5 μ m respectively.

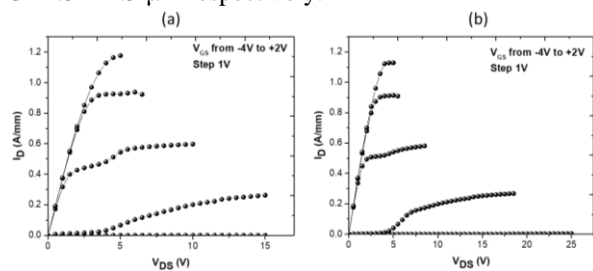


Figure 2. Output characteristics of an AlN/GaN HEMT with $L_g = 110$ nm 2×25 μ m devices with GD0.5 (a) and GD1.5 (b).

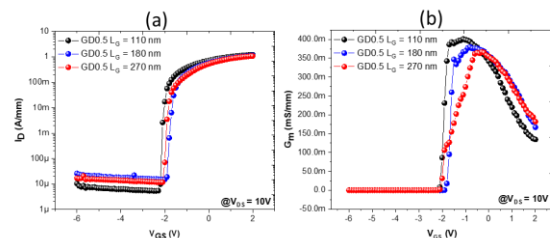


Figure 3. Transfer characteristics (a) and extrinsic transconductance (b) of an AlN/GaN HEMT 2×25 μ m devices with a gate-drain distance of 0.5 μ m (gd0.5) as a function of various gate lengths

A pinch-off voltage $V_{TH} = -2$ V (shown in Figure 3) is observed for the different gate lengths with a drain leakage current below $20 \mu\text{A}/\text{mm}$ which reflects the absence of short channel effects. Furthermore, a decrease of the extrinsic transconductance as a function of the gate length has been observed from $400 \text{ mS}/\text{mm}$ for $L_g = 110$ nm to $360 \text{ mS}/\text{mm}$ for $L_g = 270$ nm. The transconductance can be significantly optimized by reducing the access resistances as the contact resistance is as high as $0.45 \Omega \cdot \text{mm}$ for these devices.

Figure 4 shows some basic DC parameters as a function of the gate length for GD0.5 and GD1.5. As expected, a drop of $I_{D\text{max}}$ and $G_{M\text{max}}$ are observed due to the increase of the gate-drain distance and the gate length. As mention earlier, the leakage current shown in Figure 4.b, is still below $50 \mu\text{A}/\text{mm}$ for all gate lengths and GD, which reflects the high material and processing quality.

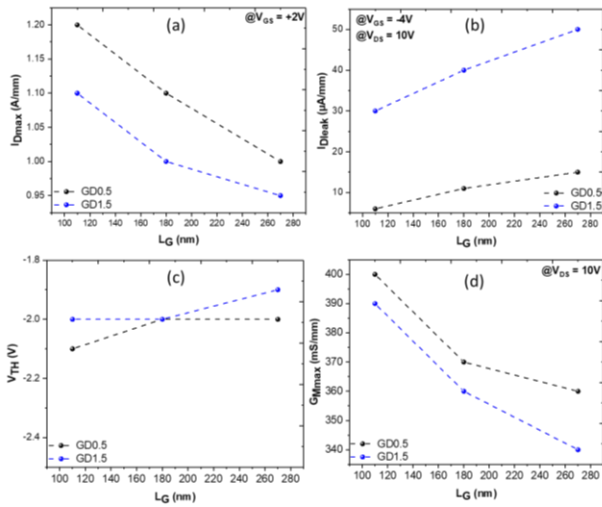


Figure 4. $I_{D\text{max}}$ (a), $I_{D\text{leak}}$ (b), V_{TH} (c), and $G_{M\text{max}}$ (d) as a function of gate length for GD0.5 and GD1.5

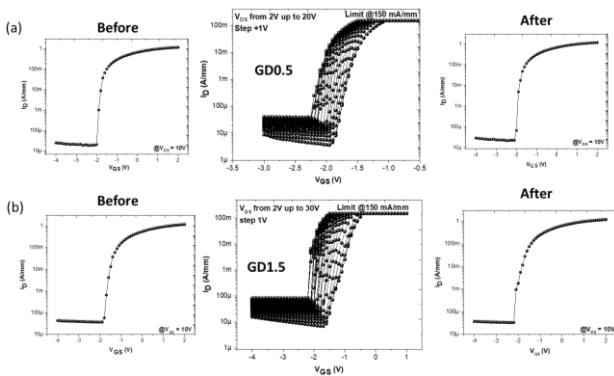


Figure 5. Semi-On robustness test up to $V_{DS} = 20V$ of a $2 \times 25 \mu\text{m}$ GD0.5 (a) and up to $V_{DS} = 30V$ GD1.5 (b) with $L_g = 110$ nm.

A semi-on robustness test has been performed on GD0.5 and GD1.5 with $L_g = 110$ nm. The maximum current density is limited to $150 \text{ mA}/\text{mm}$ and the $I_D V_D$ transfer characteristics are swept from $V_{DS} = 2$ V up to $20V$ for GD0.5 and up to $30V$ for GD1.5. The initial transfer characteristic is then compared to the one after the stress. Even for the short gate length of 110 nm, we observed a good electron confinement and no degradation during

and after the semi-on robustness test as shown Figure 5. The excellent robustness can be attributed to the absence of parasitic surface leakage resulting from the in-situ SiN cap layer.

The breakdown voltage at $V_{GS} = -4V$ is shown in Figure 6 for various GD and L_g . It can be noticed that a leakage current still below $500 \mu\text{A}/\text{mm}$ is observed (figure 6.a) for short GD. The breakdown voltage scales well versus GD with for instance $50V$ for GD0.5 to more than $100V$ for GD1.5 as shown figure 6.b.

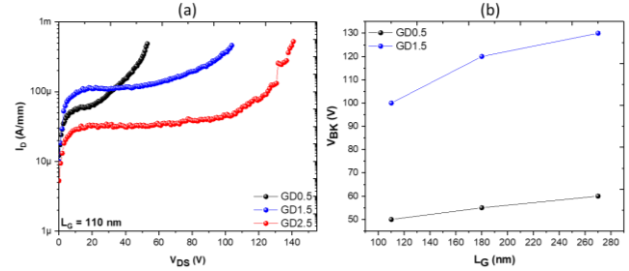


Figure 6. Breakdown Voltage characteristics of an AlN/GaN HEMT $2 \times 50 \mu\text{m}$ for various GD with $L_g = 110$ nm (a), and for various L_g with GD0.5 and GD1.5 (b).

Small signal characteristics:

The S-parameters have been measured from 250 MHz to 67 GHz with a Rhode and Schwarz ZVA67GHz network analyser as shown in Figure 7. As expected, the current gain extrinsic cut-off frequency (F_T) decreases as a function of V_{DS} and L_g (shown in figure 7a). There is a large room for improvement by both reducing the contact resistances and the gate length. The maximum oscillation frequency (F_{max}) and unilateral power gain (U_{max}) increase as function of V_{DS} (figure 7b and 7c), which in turn confirm the absence of short channel effects for the designs that have been used. F_T/F_{max} of $63/300$ GHz are achieved at $V_{DS} = 20V$ for a GD0.5 with $L_g = 110$ nm (figure 7d). It can be pointed out that the power gain is in excess of 17 dB at 40 GHz for the shortest design. The F_{max}/F_T ratio close to 5 is explained by the highly favourable aspect ratio: gate length / gate-to-channel distance.

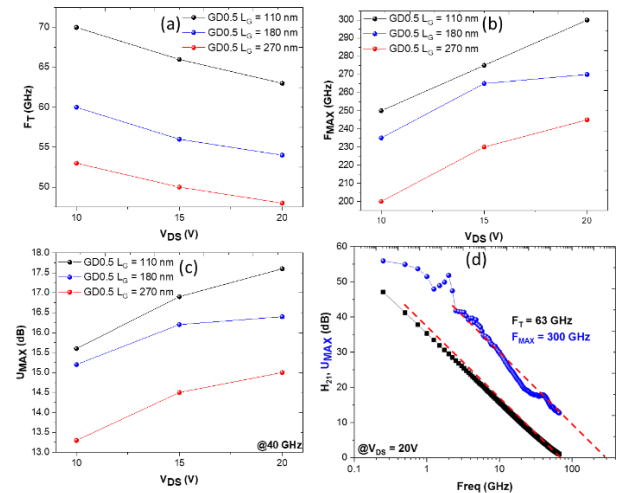


Figure 7. Small signal characteristics of an AlN/GaN HEMT $2 \times 25 \mu\text{m}$ GD0.5 for various gate lengths: F_T (a), F_{max} (b), U_{max} (c) and F_T / F_{max} at $20V$ with $L_g = 110$ nm (d)

Large signal characteristics:

Large signal characterizations have been carried out at 40 GHz on a nonlinear vector network analyzer system (Keysight Network Analyser: PNA-X, N5245A-NVNA) capable of on-wafer large signal device characterization up to the Q-band in continuous and pulsed mode. Further details of this specific power bench can be found in [6]. Figures 8a and 8b show CW power performances of 2x50 μm with $L_g = 110$ nm for GD0.5 at $V_{DS} = 10$ V and GD1.5 at $V_{DS} = 30$ V, respectively. A high saturated power (P_{out}) of 1.5 W/mm associated to power added efficiency (PAE) of 51.7% at $V_{DS} = 10$ V for GD0.5. For GD1.5 and at $V_{DS} = 30$ V, a P_{out} of 4.4 W/mm associated to a PAE of 46.3% has been achieved. It can be stressed out that in power matching a P_{out} of 6.2 W/mm is reached.

Figure 8c depicts the PAE, P_{out} and gain of 2x25 μm GD0.5, 2x50 μm GD0.5 and GD1.5 as a function of V_{DS} (PAE matching) at 40 GHz. For all device design, the PAE remains above 45 % up to $V_{DS} = 20$ V and up to 30 V when using a gate-drain distance of 1.5 μm . This capability of maintaining a high PAE above 45% up to $V_{DS} = 30$ V under high power density sets a new performance benchmark at this frequency band.

An increasing evolution of P_{out} is observed up to 3.5 W/mm at $V_{DS} = 20$ V for GD0.5 devices and 4.4 W/mm at $V_{DS} = 30$ V for GD1.5 devices. Furthermore, the power gain is maintained above 11 dB in all cases up to $V_{DS} = 30$ V. In pulsed mode a PAE of 58% combined to a P_{out} of 3.8 W/mm at 20V is reached. At $V_{DS} = 40$ V the PAE is maintained above 50% with a P_{out} of 8.3W/mm.

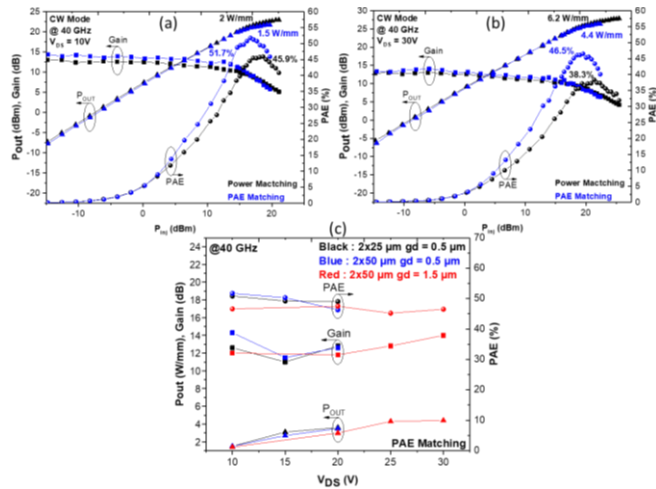


Figure 8. CW power performances of an AlN/GaN HEMT 2x50 μm with $L_g = 110$ nm for GD0.5 at $V_{DS} = 10$ V (a), GD1.5 at $V_{DS} = 30$ V (b) and CW output power density (triangle), PAE (circle) and Small signal Gain (square) vs. V_{DS} at 40 GHz (c).

Despite the short gate length and GD, we observed no degradation of the devices up to $V_{DS} = 20$ V for GD0.5 and $V_{DS} = 30$ V for GD1.5 as seen in Figure 9. The excellent robustness is attributed to the high quality of the epitaxial structure and the optimized processing.

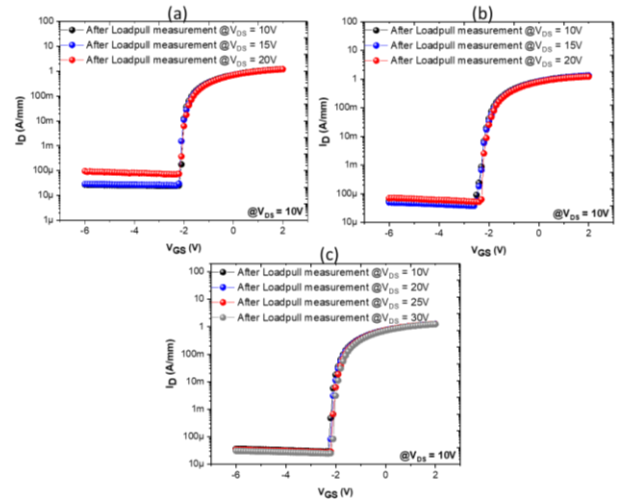


Figure 9. Transfer characteristics after large signal measurements with $L_g = 110$ nm for an AlN/GaN HEMT 2x25 μm GD0.5 (a) 2x50 μm GD0.5 (b) and 2x50 μm GD1.5 (c).

Conclusions

We have developed high frequency AlN/GaN HEMTs grown on SiC substrate. We showed that with a 110 nm gate length, high frequency performance (F_T/F_{max} of 63/300 GHz) can be reached at $V_{DS} = 20$ V. The optimized AlN/GaN HEMT structure enabled to deliver high power density together with state-of-the-art PAE > 50% at $V_{DS} = 10$ V and > 45% at $V_{DS} = 30$ V in CW mode at 40 GHz. This achievement is mainly attributed to the optimization of both material, design as well as processing quality enabling namely a high electron confinement together with reduced short channel effects under high electric field.

Preliminary CW results at 94 GHz on the same devices already demonstrated a combination of PAE about 14.5% and an outstanding P_{out} of 4 W/mm at $V_{DS} = 20$ V.

Acknowledgments

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