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GaN-on-Silicon buffer decomposition experiment: analysis of the vertical leakage current

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Abstract

In this work an extensive analysis on the leakage current of three samples obtained by stopping the epitaxial growth of a GaN-on-Silicon stack is presented. We studied the current leakage behavior and the breakdown voltage as a function of the ambient temperature, as well as the trapping phenomena that lead to a hysteresis on a double-sweep measurement. We demonstrate that the leakage current through the AlN nucleation layer is mainly related to the conduction within defects and dislocation, while as the epitaxial layer become thicker the dislocation density drops as well as both the leakage current level and the device-to-device variability. Hysteresis measurements demonstrate that the trapping within the vertical stack depends on both the ambient temperature and the injected charge during the upward sweep. Moreover, we shown that the presence of a carbon doped layer cause positive charge to be trapped within the epitaxial layers.

Introduction

GaN-on-Silicon technology is nowadays the most suitable solution for the fabrication of high-voltage and high-power High Electron Mobility Transistors [1]. The epitaxial growth of thick (Al)GaN stack over a silicon substrate is crucial to guarantee both robustness and reliability of the devices [2]. The first epitaxial layer grown over the silicon is an AlN nucleation layer, which quality is fundamental to achieve good performance of the final devices. Li et al. [3] presented an extensive analysis showing that the conduction through the AlN layer is ascribed to defect-related conduction mechanisms. As the epitaxial stack become thicker and more complex, and several layers are grown, the conduction is determined by a Space Charge Limited (SCL) process, which involve local defects and traps [4][5]. In this paper we present an analysis on the vertical leakage current and the related charge trapping on three key structures which compose a standard GaN-on-Silicon stack.

Experimental

The analysis presented within this paper is focused on three samples, namely sample A, sample B and sample C (Figure 1). These three samples were obtained by interrupting the epitaxial growth of a standard GaN-on-Silicon epitaxial stack at different stages of the growth process. Sample A consists of a 200nm-thick AlN layer growth over a conductive n-doped silicon substrate. Sample B has a similar structure than sample A, but over the AlN layer a 350nm-thick AlGaN layer is grown. Lastly, in sample C, over the n-doped silicon substrate, an AlN layer, a 2350nm-thick (Al)GaN multilayer and a 2450nm-thick carbon doped GaN layer are grown. Within each sample several ohmic contact were processed, so that the conduction between the substrate and the top layer could be evaluated.

The electrical characterization presented within this work have been carried out by means of a Keysight B1505 semiconductor parameter analyzer, equipped with a high voltage Source/Measure Unit (SMU) capable to supply $\pm 3000\text{V}$ with a current of 4mA.

Results and discussion

In order to obtain a preliminary overview on the behavior of the three samples under test when submitted to an electrical stress, we started the analysis by sweeping the voltage of the

top ohmic contact of several devices for each sample from 0V up to the failure of the vertical stack.

Devices on sample A (Figure 2 (a)) exhibit a remarkably noisy current over the applied voltage, as well as a high device-to-device variability. This can be ascribed to the high defectivity of the AlN layer grown over the Silicon substrate; even though the nucleation layer is fundamental for the growth of the subsequent (Al)GaN layers, the high lattice mismatch between Aluminum Nitride and Silicon as well as the low surface mobility of the Al species during the epitaxial growth, result in the creation of defects and dislocations. These latter cause the conduction to be a local process, thus resulting in the high variability observed.

From Figure 2 (b), it can be noticed that the AlGaN layer grown over the AlN nucleation layer, considerably improve the stability of the devices, resulting in a more repeatable behavior of the leakage currents over the applied voltage. Usually, in a standard GaN-on-Silicon buffer, several AlGaN layers are interposed between the substrate and the active region of the device: the aim of these layers is to compensate the tensile stress that generate during the epitaxial growing process, as well as to reduce the dislocation density that propagate from the nucleation layer toward the buffer.

Lastly, sample C, is composed by the AlN nucleation layer, a complex (Al)GaN stress compensation layer, and most important for this analysis, a 2450nm thick carbon doped GaN layer. The carbon impurities act as acceptor states, thus compensating the intrinsic conductivity of the unintentionally doped GaN; the resulting highly resistive layer either considerably improve the vertical robustness of the GaN-on-Silicon stack and prevent the punch through effect. Figure 2 (c) demonstrate that the leakage current of the devices within sample C is very stable up to the failure of the vertical stack; moreover, it can be noticed that the robustness of the whole stack is remarkably enhanced, and the failure voltage at room temperature is above 700V.

In Figure 3 the current-voltage characteristics at low- and at high-temperature of the three analyzed samples are compared. The leakage current on sample A is not strongly affected by the ambient temperature, meaning that the conduction is mainly related to tunneling and hopping processes which might occur within the dislocations that propagate from the Si/AlN interface toward the ohmic contact on the top of the AlN. On the other hand, the leakage current on sample B has a higher dependence on the ambient temperature, meaning that there is not only a conduction through dislocations, but also either thermal emission or band conduction play a role. Blue lines in Figure 3 show the strong impact of the ambient temperature on the vertical leakage of the sample C. The high temperature dependence is compatible with the presence of a deep acceptor level (i.e. carbon); a tentative explanation is that at high temperature the compensation of the residual conductivity of the GaN is less effective than at low temperature, resulting in a strongly increase of the vertical leakage with the increasing ambient temperature.

Figure 4 shows the hysteresis measurements performed on all the three samples presented within this analysis at both room temperature and high temperature. The hysteresis between the upward and the backward sweep is mostly related

to charges that are trapped and to the electrostatic effect they have either in the charge-injection and in the conduction. On sample A (Figure 4 (a)), as the ambient temperature increases from 30°C to 150°C, the hysteresis is considerably reduced. This can be ascribed to the effect of the temperature on the detrapping kinetic, which results in a lower amount of trapped charges during the backward sweep with respect to the upward sweep. Unlike sample A, sample B exhibit a comparable hysteresis at both room temperature and high temperature; it is worth noticing that, unlike sample A in which the current level during the upward sweep is not depending on the ambient temperature, the leakage current in sample B strongly depends on the temperature, as discussed in the previous paragraph. This leads to a higher carrier injection, which results in an increased availability of charge that might be trapped. Sample C, beside being the more complex structure within the experimental set, thanks to the carbon acceptor states, is the only structure where also a source of positive charges is present. The role of the carbon in the hysteresis of the leakage current through the stack is clear in Figure 4 (c): the current during the backward sweep is higher than the current during the upward sweep, meaning that positive charges which promote the carrier injection are trapped within the stack. The high temperature even enhances this phenomenon, thanks to the higher availability of positive charges within the epitaxial layers.

Conclusions

In this work we demonstrate that the current on the AlN nucleation layer is mainly related to the conduction through defects and dislocation. Moreover, we evaluated the impact of the ambient temperature on the vertical leakage through both the AlN nucleation layer, and on two more complex structures. Lastly, we shown that during an IV sweep the presence of a carbon doped layer results in the trapping of positive

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References

- [1] H. Amano et al., “The 2018 GaN power electronics roadmap,” *J. Phys. D: Appl. Phys.*, vol. 51, no. 16, p. 163001, Apr. 2018, DOI:10.1088/1361-6463/aaaf9d.
- [2] M. Borga, M. Meneghini, I. Rossetto, S. Stoffels, N. Posthuma, M. Van Hove, D. Marcon, S. Decoutere, G. Meneghesso, and E. Zanoni, “Evidence of Time-Dependent Vertical Breakdown in GaN-on-Si HEMTs,” *IEEE Trans. Electron Devices*, vol. 64, no. 9, 2017, DOI:10.1109/TED.2017.2726440.
- [3] X. Li, M. Van Hove, M. Zhao, B. Bakeroot, S. You, G. Groeseneken, and S. Decoutere, “Investigation on Carrier Transport Through AlN Nucleation Layer From Differently Doped Si(111) Substrates,” *IEEE Trans. Electron Devices*, vol. 65, no. 5, pp. 1721–1727, May 2018, DOI:10.1109/TED.2018.2810886.
- [4] C. Zhou, Q. Jiang, S. Huang, and K. J. Chen, “Vertical leakage/breakdown mechanisms in AlGaIn/GaN-on-Si structures,” *2012 24th Int. Symp. Power Semicond. Devices ICs*, vol. 33, no. 8, pp. 245–248, 2012, DOI:10.1109/ISPSD.2012.6229069.
- [5] P. Moens, A. Banerjee, M. J. Uren, M. Meneghini, S. Karboyan, I. Chatterjee, P. Vanmeerbeek, M. Casar, C. Liu, A. Salih, E. Zanoni, G. Meneghesso, M. Kuball, and M. Tack, “Impact of buffer leakage on intrinsic reliability of 650V AlGaIn/GaN HEMTs,” *Tech. Dig. - Int. Electron Devices Meet. IEDM*, vol. 2015–Decem, p. 35.2.1–35.2.4, 2015, DOI:10.1109/IEDM.2015.7409831.

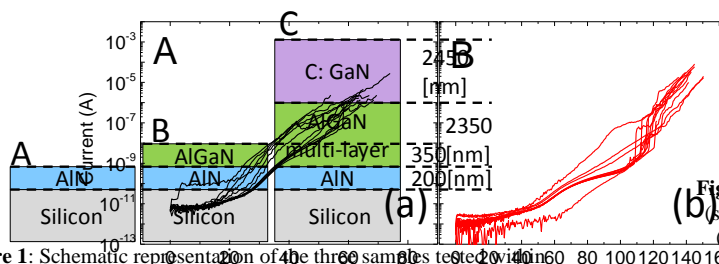


Figure 1: Schematic representation of the three samples tested in this work: Sample A (left), Sample B (center) and Sample C (right). Voltage (V)

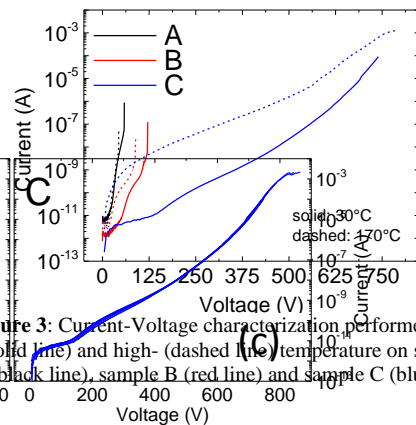


Figure 3: Current-Voltage characterization performed at low- (solid line) and high- (dashed line) temperature on sample A (black line), sample B (red line) and sample C (blue line). Voltage (V)

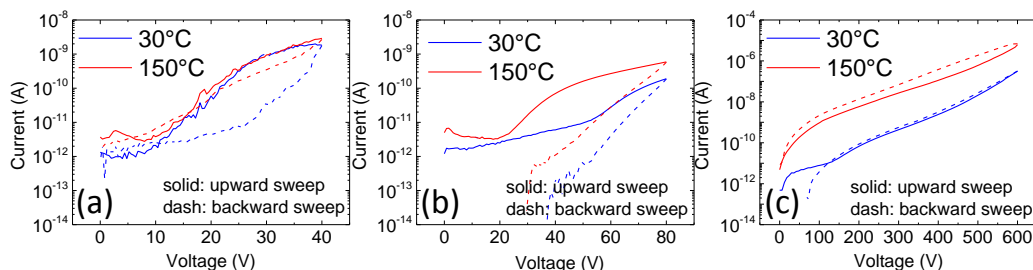


Figure 4: Double sweep (upward: solid, backward: dashed) Current-Voltage characterization on (a) sample A, (b) sample B and (c) sample C. The measurements have been carried out at 30°C (blue line) and at 150°C (red line)