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# Superlattice GaN-on-silicon heterostructures with low trapping in 1200 V

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## Abstract

*The aim of this work is to investigate the role of the epitaxial structure on the low trapping effects of GaN-on-silicon heterostructures use for power application. Structures with and without superlattices (SL) are analysed. In particular, it is shown that the insertion of SL into the buffer layers allows pushing the vertical breakdown voltage above 1200 V without generating additional trapping effects as compared to a more standard GaN-based epi-structure using similar total buffer thickness. A low trapping effect down to -1.2 kV has been observed with substrate ramp measurements. Indeed, we demonstrated that a structure with SL shows a reduction in the trapping effects with high vertical breakdown.*

## Introduction

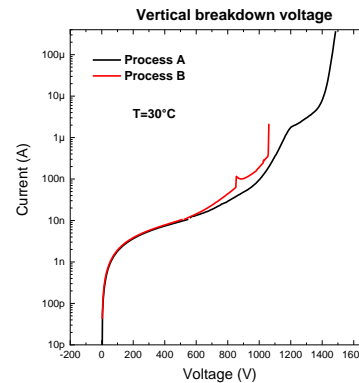
GaN high-electron-mobility transistors (HEMTs) on silicon (Si) substrate has been proved as excellent materials for power applications due to the large bandgap, high breakdown field strength, and high electron saturation velocity [1][2]. Recently significant efforts have been developed in order to find optimum GaN-on-silicon epitaxial structures enabling outstanding DC performances beyond 1 kV with low trapping effects [3][4]. Toward this end, in this work we demonstrate a vertical breakdown voltage above 1200 V based on superlattice buffer layers without generating additional trapping effects as compared to a more standard step-graded GaN-based epi-structure. Substrate ramp measurements are used to obtain the charge trapping effect into the buffer structure and the results are compared to a reference device at various temperature (up to  $T=150^{\circ}\text{C}$ )[5].

## Experimental

For this study, the GaN-on-silicon heterostructures are manufactured by EpiGaN targeting 1200 V power applications. The step-graded buffer structure has a  $5.5\ \mu\text{m}$  total thickness (**process B**) while the structure based on superlattices (SL) has a total thickness of  $5\ \mu\text{m}$  (**process A**). The breakdown voltage and the trapping effects in the buffer have been studied through a series of substrate bias ramp measurements. The analyses have been done also at different temperature in order to understand the different leakage current level.

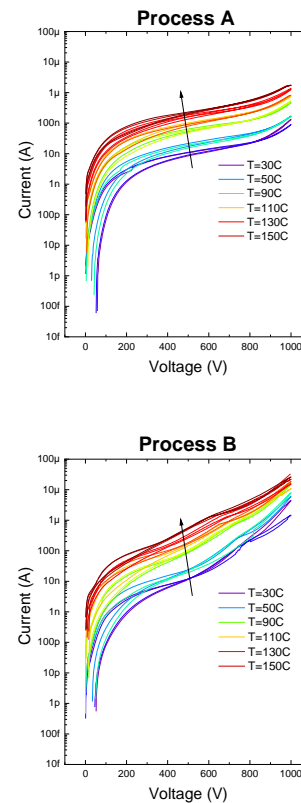
## Results and discussion

Vertical breakdown voltages measurements have been performed on both devices. A vertical breakdown of a 1300 V at  $1\ \mu\text{A}$  is reached for the structure with SL as compared to a 1000 V for the more standard structure (Fig. 1). Furthermore, it can be noticed that a low vertical leakage current is observed up to a temperature of  $150^{\circ}\text{C}$  for the SL heterostructure. The leakage current increase, up to a  $150^{\circ}\text{C}$ , is significantly lower than the reference heterostructure without SL. Fig. 2 shows the leakage current on process A, B at different temperature from  $30^{\circ}\text{C}$  to  $150^{\circ}\text{C}$ , in which the vertical leakage current increases with temperature.[6][7].



**Figure 1.** Vertical breakdown voltage at room temperature for heterostructure with (process A) and without (process B) SL.

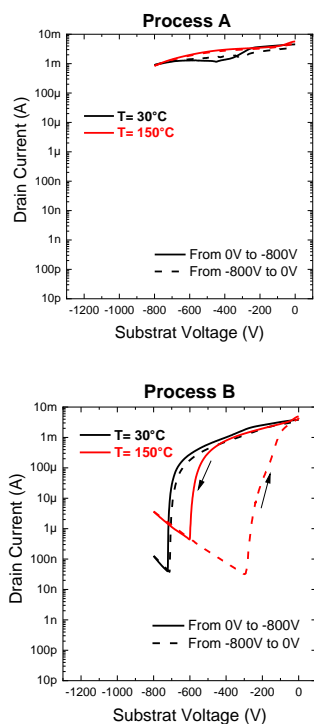
Substrate ramp analysis is a technique to get the buffer traps information in the off-state condition. In order to study the buffer trapping effects, substrate ramp measurements have been carried out on both devices by ramping the bulk from 0 V down to -800 V in the off-state condition.



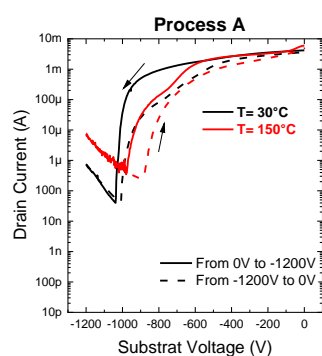
**Figure 2.** Vertical leakage current at different temperature for heterostructure with (process A) and without (process B) SL.

Fig. 3 reports the measurement at room and high temperature ( $T=150^{\circ}\text{C}$ ) for process A and B. The reference heterostructure without SL shows low trapping effect down to a  $-800\text{ V}$  with a strong trapping activation starting from  $-900\text{ V}$ . However, the optimized SL buffer uniformly delivers state-of-the-art low trapping effects all the way down to  $-1200\text{ V}$  as shown in Fig. 4.

Moreover, electrical characterizations have been realized on  $2\times 50\text{ }\mu\text{m}$  transistors with a gate length of  $2\text{ }\mu\text{m}$  for several gate-drain distances (GD) for both structures. DC characteristics ID-VD and ID-VG reveal a low leakage current and an excellent pinch-off behaviour reflecting the absence of parasitic punch-through effect or gate leakage current.



**Figure 3.** Substrate ramp measurement on process A and B at room and high temperature.



**Figure 4.** Substrate ramp measurement on process A at room temperature and high temperature, down to  $-1.2\text{ kV}$

## Conclusion

In conclusion, it has been shown that a heterostructure with superlattices (SL) shows no temperature dependency to a substrate ramp and a low trapping effect even at high temperature. The measured results indicate that a proper buffer optimization along with the insertion of SL clears a way to GaN-on-silicon lateral power transistors operating at  $1200\text{ V}$  with very low trapping effects.

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