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Characterization and Electrical Modeling including Trapping Effects of AlN/GaN HEMT 4x50 μ m on silicon substrate

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Abstract—This paper reports the full characterization and modeling of novel AlN/GaN HEMTs on silicon using a short gate length. This device has been optimized for high frequency analog circuits applications. The presented model includes DC and small-signal modeling steps taking into account the trapping effects. It contains a trap model inside the current source which allows to accurately predict gate-lag transient response and low frequency dispersion of the output admittance. The model is validated by comparing the 4 GHz load-pull measurement results with the simulation ones.

Index Terms—characterization, modeling, GaN, traps

I. INTRODUCTION

GaN-based devices enable to achieve excellent performances, particularly for high power and high frequency applications. In this context, a short gate length ($\leq 0.15\mu\text{m}$) AlN/GaN HEMT grown on silicon (Si) substrate has been developed, showing attractive performance. The main drawback associated with the silicon substrate is the high RF loss. The GaN/Si interface optimization has been performed on these devices which allows obtaining RF loss less than 0.5dB/mm until 100GHz for a 1 mm transmission line [1].

To represent the transistor for designing the PA, LNA and VCO, a large signal (LS) and high frequency non-linear model is mandatory. The drawback of GaN-based transistors is the presence of deep level states into the heterostructure, called traps. In order to accurately predict the device behavior, trapping effects and its associated modeling are necessary.

In this paper, DC, small signal, large signal and transient measurements have been performed on a 4x50 μm AlN/GaN transistor and compared with the simulation results obtained from our in-house developed large signal model using Keysight ADS software. After a short device description, the first part of this work is devoted to the device static modeling comparing I/V simulated and measured characteristics. In the second part, the small signal modeling based on low frequency (LF) and high frequency (HF) S-parameters measurements is described. In the third part, trapping effect characterizations and simulations are compared. In the last section of this paper, the LS model is validated by comparing load-pull measurements with simulation results.

II. DEVICE DESCRIPTION

The AlN/GaN/AlGaIn double heterostructure were grown by metal organic chemical vapor deposition (MOCVD) on a highly resistive 4 in. Si (111) substrate. The studied structures consisted of transition layers, and a 1.5- μm -thick Al_{0.08}Ga_{0.92}N buffer layer followed by a 150 nm GaN channel for the double heterostructure (DHFET). On top of the GaN channel layer, a 4.0 nm ultrathin AlN barrier layer and a 20-nm-thick in situ Si₃N₄ cap layer were deposited, as shown in Fig. 1 [1]. The main specificities are the high polarization AlN material as a barrier layer and the 20 nm thick in-situ SiN cap layer that enables both to withstand much higher electric field and to reduce the current collapse as compared to thinner cap layer. A high drain current can be exhibited while showing together with a low off-state leakage current in the $\mu\text{A}/\text{mm}$ range resulting in a high breakdown voltage while using a 120 nm gate length with a gate-drain distance of 1 μm .

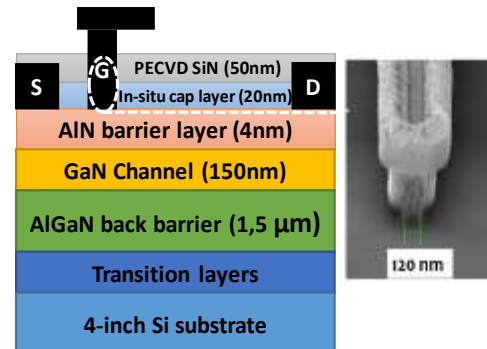


Fig. 1 Schematic cross section of the fabricated AlN/GaN-on-silicon transistors. The inset shows a SEM image of the gate electrode.

III. OUTPUT NETWORK MODELING

To better understand the device behavior, two types of DC characterization are performed. First, continuous I/V measurements have been carried out using the Keysight B1500A semiconductor parameter analyzer. This instrument is capable of measuring both gate and drain voltages and currents, and it also

computes the trans-conductance (gm). Secondly, pulsed-IV (P-IV) measurements (pulse period: 100us, duty cycle: 0.8%) have been carried out with a quiescent point ($V_{gs0}=0V$, $V_{ds0}=0V$) in order to obtain trapping effects free characteristics. Afterwards, two measurement configurations are used to highlight the gate lag ($V_{gs0}=-5V$, $V_{ds0}=0V$) and drain lag ($V_{gs0}=-5V$, $V_{ds0}=10V$) trapping effects. These two sets of measurements will be used to model the traps. Once the measurements have been performed, the current source chosen is an equation-based model which takes into account the gate-lag and drain-lag effects [2]. Current source modeling procedure starts by tuning the model output I/V network to match the measurements corresponding to the ideal case without trapping effects ($V_{gs0}=0V$, $V_{ds0}=0V$). This step allows us to determine the source (Rs) and drain (Rd) resistances thanks to the Ron P-IV measurements slope value. Rg is then estimated due to its influence on the small signal S-parameters.

A comparison between the P-IV measurements and the simulation results is presented in Fig. 2. The fictive load-line, which links the chosen bias points for the future designs, is drawn in black. The Cgs and Cgd non-linear capacitances are extracted along this load-line.

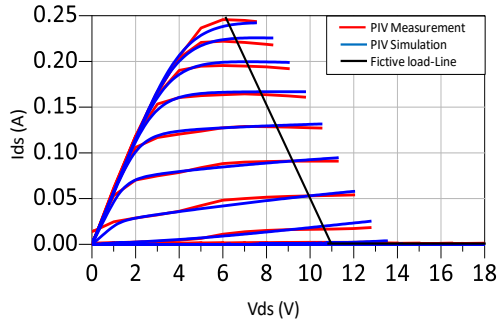


Fig. 2. Comparison between I/V measurements and simulations. Vds varies from 0V to 18V, 0.5V step. Vgs varies from -5V to 2V, 0.5V step.

IV. SMALL SIGNAL S-PARAMETERS MODELING

Two types of multi-bias S-parameters measurements have been performed. These measurements are repeated for every single bias point of the output I/V network presented in Figure 2. The first type is LF S-parameters measurements, performed using the Keysight E5061b VNA, which covers the 3Hz-3GHz band. The second type is the HF S-parameters measurements performed with the Wiltron 360B VNA which ranges from 40MHz up to 40 GHz.

The LF measurements allow the non-linear capacitances (Cgs, Cds, Cgd) extraction along a fictive load-line. They also enable the trapping effects characterization by studying the output admittance frequency dispersion. To compute the non-linear capacitances, LF S-parameters measurements are converted into Y-parameters using ADS software. Since capacitances are linked to the imaginary part of the admittance, we compute the capacitances values from the equations (1)-(3) for various gate

voltage points chosen on the fictive load-line drawn in Fig. 2 [3].

$$C_{gs} = \frac{\text{Im}(Y_{11}) + \text{Im}(Y_{12})}{2\pi f} \quad (1)$$

$$C_{gd} = \frac{-\text{Im}(Y_{12})}{2\pi f} \quad (2)$$

$$C_{ds} = \frac{\text{Im}(Y_{22}) + \text{Im}(Y_{12})}{2\pi f} \quad (3)$$

Knowing the capacitances values, we simply model the three capacitances with the same equation (4) and we adjust the parameters in order to match the simulation results with the measurements [3].

$$C = C_0 + \frac{C_1 + C_2}{2} [1 + \tanh(A * (V + V_m))] - \frac{C_2}{2} [1 + \tanh(B * (V + V_p))] + \frac{C_3}{2} [1 + \tanh(C * (V + V_n))] \quad (4)$$

This last expression has 10 parameters optimized for each non-linear capacitance. According to the capacitance which is modeled, the variable V stands for the command voltage of Cgs, Cgd and Cds, respectively Vgs, Vgd and Vds.

From now on, the intrinsic parameters are known. The remaining extrinsic parameters (Cpg, Cpd, Lg, Ld, Ls) are tuned to fit the HF S-parameters measurements for bias points within the fictive load-line, and also for the other bias points of the output I/V network. Finally, a comparison between model results and measurements is given in Fig. 3 for one bias point: Vgs = -1V, Vds = 10V. It shows the validity of the developed small signal model for a wide frequency range.

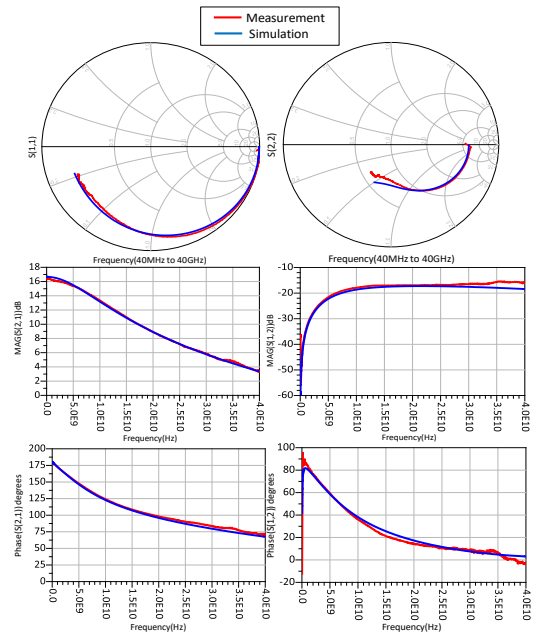


Fig. 3. Comparison between S-parameters measurements (red) and simulations (blue). (Bias point: Vgs=-1V/Vds=10V)

V. TRAPPING EFFECTS MODELING

✓ Low frequency S-parameters measurement

The low frequency S-parameters measurements in the frequency of 100 Hz to 100 MHz have been carried out using an Agilent E5061B network analyzer. The 4x50 μ m device S-parameters measurements have been performed for the bias conditions of VDS=10V and IDS= 115 mA (VGS=0V). The measured LF S-parameters are converted into their equivalent Y-parameters. Fig.4 shows the imaginary part of Y₂₂ parameter extracted using LF S-parameters measurements for T_{CHUCK} between 25°C and 125°C.

The measurement Y₂₂ parameter shows the presence of two traps in the device 'Trap1' and 'Trap2'. It is clear in Fig.4 that the peak value of Y₂₂ parameter for Trap 1 shift towards higher frequencies as the temperature increases, while Trap 2 does not show the frequency shift as the temperature increases, instead the peak amplitude increases with temperature.

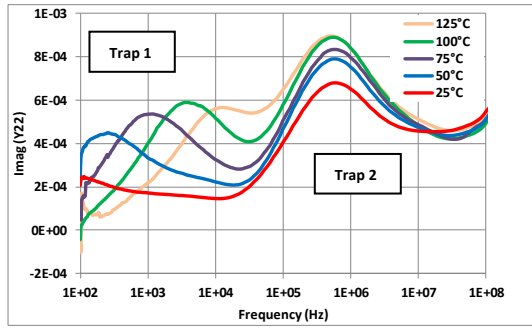


Fig. 4. Imaginary part of the measured Y₂₂ parameter vs. frequency for the T_{chuck} ranges between 25°C and 125°C.

The emission time constant (τ_n) is calculated at each measurement temperature using equation (5).

$$f_{peak} = f(\text{imag}Y_{22}) = \frac{1}{2\pi\tau_n} \quad (5)$$

Then by using Arrhenius equation, the plot of $\ln(\tau_n T^2)$ versus $1/kT$ yields the straight line, whose slope and intercept determine the apparent activation energy and cross section of the traps existing in the device.

Fig.5 shows the Arrhenius plot of two traps extracted using LF S-parameter measurements. we extracted an activation energy of 0.84eV for the first trap (Trap 1) and 0,06eV for the second trap (Trap 2).

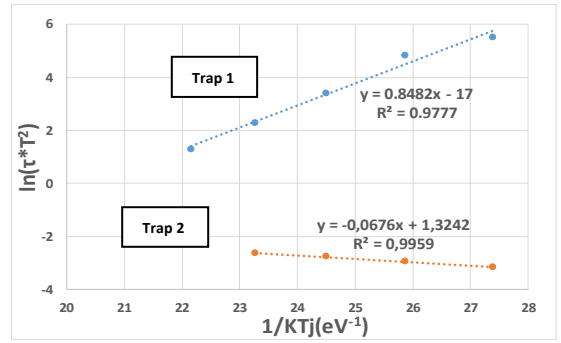


Fig. 5. Extracted Arrhenius plot using Y₂₂ parameter

In order to understand, to localize and identify dispersive effects occurring in GaN HEMT device, two-dimensional (2D) TCAD physics-based device simulations will be performed later.

Other S-parameters measurements have been performed for VDS (6V ,8V, 10V) and for VGS= 0V at different temperature. Fig. 6 and Fig.7 shows that the peak values of Imag(Y₂₂) for (Trap 1) shift towards high frequencies as VDS increases, showing that the emission rate increases not only with the temperature but also with the applied electric field. Trap2 shows that the emission rate increases only with the temperature and decrease with the applied electric field.

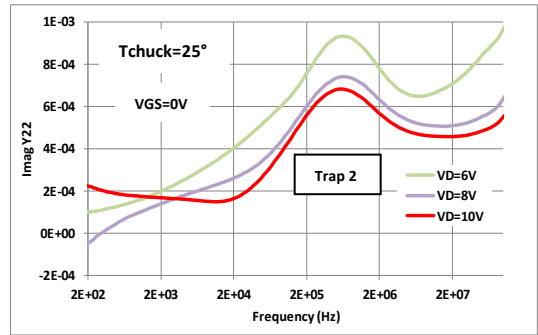


Fig. 6. Frequency don't shift for the peak of Imag[Y₂₂] for trap 2 at different VDS with a constant temperature of 25°C

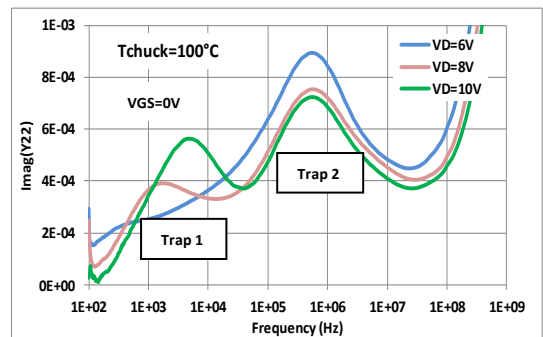


Fig. 7. Frequency shift for the peak of Imag [Y₂₂] for trap1 at different VDS with a constant temperature of 100°C

Fig.8 shows the imaginary part of Y_{22} versus frequency. It is evident from the characterization plot that trap is visible only for V_{gs} greater than $-0.5V$.

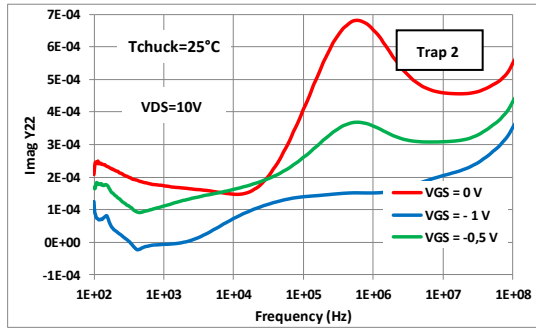


Fig. 8. Frequency don't shift for the peak of $\text{Imag}[Y_{22}]$ for trap 2 at $V_{DS}=10V$ and for different V_{GS} with a constant temperature of $25^\circ C$

✓ Trapping modeling for $25^\circ C$

The output admittance low frequency dispersion allows to identify the deep energy level effects [4]. The variables of the trap models, inside the current source, are adjusted in order to reproduce the Y_{22} imaginary part dispersion without impacting the DC and small signal modeling which has been already achieved. In Fig. 9, the measured and simulated imaginary parts of the output admittance are compared and are found to be in reasonable agreement.

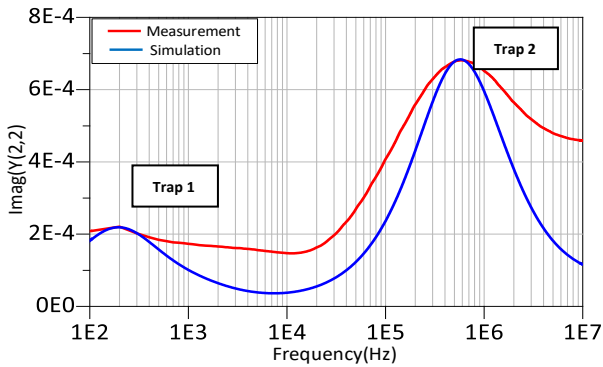


Fig. 9. Comparison between imaginary part of Y_{22} measurement at $25^\circ C$ (red) and simulation (blue). Bias point: $V_{gs} = 0V$, $V_{ds}=10V$.

VI. LS MODEL VALIDATION

The modeling work has been carried out both for DC and small signal conditions, including trapping effects. Finally, load-pull measurements are performed in order to validate the model in large signal operation. The measurement bench is composed of one RF arbitrary waveform generator MXG N5162B (9 kHz–6 GHz), one LSNA, two tuners and two couplers. One tuner is connected to the DUT input and used to vary the source impedance. The second tuner is wired on the DUT output in order to tune the load impedance at the fundamental frequency (f_0), also at the second harmonic ($2f_0$) and the third harmonic ($3f_0$). The couplers are added between the tuners and the DUT to capture the incident and reflected waves with the LSNA.

Load-pull measurements have been carried out at 4GHz with 50 ohm presented both on the source and on the load sides of the DUT. The bias point chosen is ($V_{gs}=-1V$, $V_{ds}=10V$), corresponding to a deep AB class operating mode. The input power ranges from -25 dBm to 9 dBm in order to push the device in non-linear compression region. In Fig. 10, a simulation and measurement comparison is shown at the same bias point. The comparison reveals a good agreement, confirming the validity of the developed model.

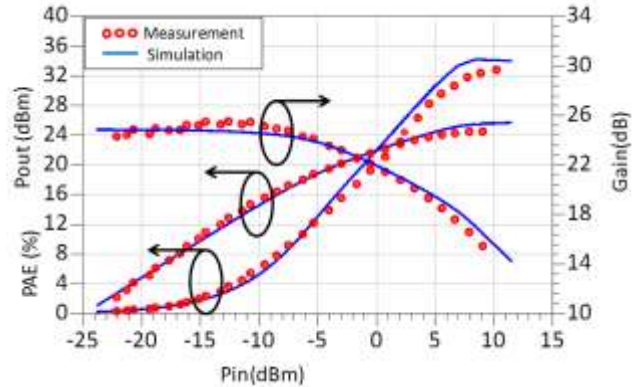


Fig. 10. Large signal model validation: comparison between load-pull measurements (symbols) and simulation (lines). (Bias point: $-1V/10V$)

VII. CONCLUSION

To conclude, a new large signal model has been developed for an emerging AlN/GaN HEMT technology. This model presents a good agreement for all the comparisons depicted: I_d/V_d characteristics, low frequency and high frequency S-parameters. The device current source model includes a comprehensive trap model which successfully simulates the low frequency output admittance dispersion and the gate lag transient response. The model has been validated under large signal conditions through 4 GHz load-pull measurements with approximately 32% of PAE for 50 Ohm load impedance.

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