Comparison of C-Doped AlN/GaN HEMTs and AlN/GaN/AlGaN Double Heterostructure for mmW Applications

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***Abstract*— We report on a comparison of the ultrathin (sub-10 nm barrier thickness) AlN/GaN heterostructure using two types of buffer layers for millimeter-wave applications: 1) carbon doped GaN high electron mobility transistors (HEMTs) and 2) double heterostructure field effect transistor (DHFET). It is observed that the carbon doped HEMT structure shows superior electrical characteristics, with a maximum drain current density I_d of 1.5 A/mm, an extrinsic transconductance G_m of 500 mS/mm and a maximum oscillation frequency f_{max} of 242 GHz while using a gate length of 120 nm. The C-doped structure delivering high frequency performance together with an excellent electron confinement under high bias enabled to achieve a state-of-the-art combination at 40 GHz of output power density (P_{OUT} = 7 W/mm) and power added efficiency (PAE) above 52% up to V_{DS} = 25V in pulsed mode.**

I. INTRODUCTION

With the development of wireless communication such as 5G or SATCOM, the need and requirements for millimeter-wave compact solid-state high power amplification has significantly increased. Achieving high power-added-efficiency and output-power-density combination in the millimeter-wave range represents currently one of the key goal for the GaN technology. Indeed, higher PAE not only saves electrical power usage but also can reduce the size and cost of high power amplifiers (HPAs), due to the lower amount of heat dissipated. For instance, in space applications, the traveling wave tube amplifiers (TWTA) are still widely used, because of the high PAE while delivering high P_{OUT}. Even though attractive efficiencies on GaN devices (well-beyond 40%) have been already demonstrated up to Ka band [1][2][3][4][5], rather limited PAE has been reported so far in the Q band (40 GHz) and above. For high frequency applications requiring short gate lengths, it has been shown that the double heterostructure using a thick AlGaN back barrier with 8% Aluminum (Al) content enabled to combine a high electron confinement with high frequency performance and low trapping effects [6]. It can be noticed that the record frequency performances achieved on devices fabricated by HRL laboratory employed an AlGaN back barrier [7] as well. However, AlGaN alloys have the drawback that they have much poorer thermal conductivity than the binary GaN or AlN alloys[8], which causes an increase in the peak channel temperature during operation. C-doped GaN buffers have been widely adopted in high voltage power switching applications[9], and have the advantage compared to Fe-doped GaN buffers of lower memory effects[10], lower risk of diffusion and the elimination of contamination risks when used in Si CMOS-based foundries..
In this paper, the two types of buffer layer structure, DHFET and C-doped HEMT are evaluated and compared using a 0.12 µm gate technology.

II. MATERIAL AND D EVICE PROCESSING

The AlN/GaN heterostructures were grown by metal organic chemical vapor deposition (MOCVD) on 4 in. SiC substrates. The HEMT structure consists of transition layers to GaN, a 1 µm-thick C-doped GaN buffer layer followed by an undoped GaN channel, a 4.0 nm ultrathin AlN barrier layer and a 10-nm-thick in situ Si_3N_4 cap layer (Fig. 2.1). The in situ SiN layer is used both as early passivation as well as to prevent strain relaxation [11][12][13]. In the second structure called DHFET, the 1-µm-thick C-doped GaN buffer layer is replaced with a 1 µm-thick $Al_{0.08}Ga_{0.92}N$ layer and a 150 nm GaN channel as shown in Fig. 2.1. Room-temperature Hall measurements showed high electron sheet concentrations of 1.8×10^{13} and 1.6×10^{13} cm^{-2} with an electron mobility about 1100 $cm^2V^{-1}s^{-1}$ in the HEMT and DHFET heterostructures, respectively.

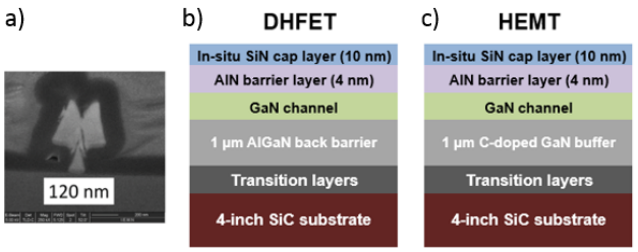


Fig. 2.1. : a) FIB view of the 0.12 µm T-gate and schematic cross section of b) DHFET and c) C-doped HEMT.

A Ti/Al/Ni/Au metal stack followed by a rapid thermal annealed has been used to form the ohmic contacts directly on top of the AlN barrier layer by etching the in situ Si_3N_4 layer. Device isolation was achieved by nitrogen implantation.

Ohmic contact resistance (R_c) extracted from linear transmission line model (TLM) structures was as low as 0.3 Ω.mm for both heterostructures. Then, a 0.12 µm Ni/Au T-gate length was defined by e-beam lithography (see Fig. 2.1). The SiN underneath the gate was fully removed by SF_6 plasma etching. The gate-source and gate-drain spacings were 0.3 and 2 µm, respectively, and the device width was 50 µm. Finally, 200 nm PECVD Si_3N_4 was deposited as final passivation.

III. DC AND SMALL SIGNAL CHARACTERIZATION

DC measurements have been performed with a Keysight A2902A static modular and source monitor. The Fig 3.1 shows the typical I-V characteristics of both structures. The gate source voltage was swept from -6V to +2V with a step of 0.5 V. For the DHFET, a maximum current drain density (I_{Dmax}) of 1.3 A/mm is observed at V_{DS} = 10V. For the HEMT, a higher I_{Dmax} of 1.5 A/mm is obtained under the same conditions reflecting the higher carrier concentration.

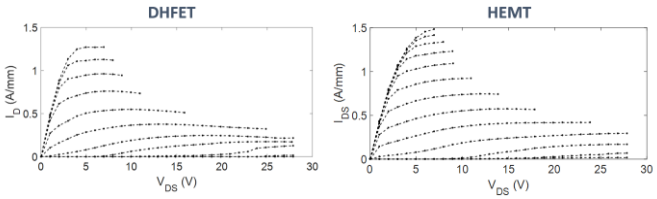


Fig. 3.1. : Output characteristics of DHFET and C-doped HEMT.

The transfer characteristics of both structures at V_{DS} = 6, 8 and 10 V are shown in Fig. 3.2. Excellent device pinch-off behavior are obtained in both cases with a low off-state leakage current well-below 10 µA/mm. This confirms that a good electron confinement can be also obtained without the use of an AlGaN back barrier, even when using short gate lengths. At the same time, a slightly higher extrinsic transconductance is observed for the HEMT structure with a G_m around 500 mS/mm at V_{DS}=10V against 470 mS/mm at V_{DS} =10V for the DHFET. At these respective biases, the cut-off frequency and maximum frequency oscillation are extracted from the scattering (S) parameters using Rhode and Schwarz ZVA67GHz. The DHFET yields a f_T = 56 GHz and f_{max} = 235 GHz while rather similar RF performances are achieved for the HEMT with f_T = 60 GHz and f_{max} = 242 GHz (see Fig. 3.3). It can be stressed that a high f_{max} / f_T ratio above 4 is observed, which is quite untypical. This is due to the favorable aspect ratio between the gate length and the gate to channel distance (ultrathin 4nm barrier), the high carrier concentration and the low parasitic gate capacitance.

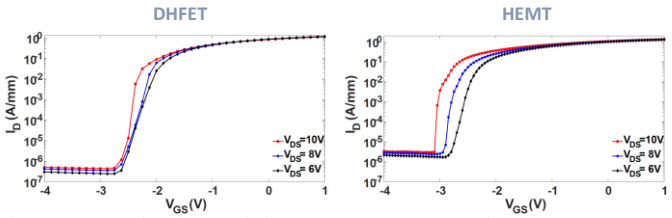
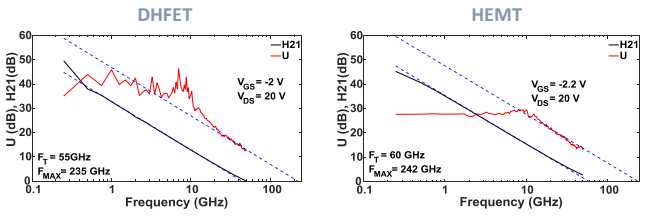


Fig. 3.2. : Transfer characteristics at V_{DS} = 6, 8, 10 V of DHFET and HEMT.



	F_t (GHz)			F_{max}(GHz)		
V_{ds} (V)	10	15	20	10	15	20
DHFET	65	60	55	148	195	235
C-doped HEMT	70	66	60	211	238	242

Fig. 3.3. : RF performance of the 0.12 µm of DHFET and C-doped HEMT.

IV. LARGE SIGNAL CHARACTERIZATION AT 40 GHZ

Large signal characterizations at 40 GHz have been carried out on both structures in pulsed mode (1 µs width and 1% duty cycle). It can be stressed that the same measurement conditions (deep AB class) have been used for the HEMTs and DHFETs. Fig 4.1 shows the pulsed power performance of a 0.12×50 µm² AlN/GaN HEMT at 40 GHz with V_{DS} = 15V, 20V, and 25 V. A saturated P_{OUT} (output power density) of 7 W/mm was achieved with a peak PAE of 52% associated to a linear power gain above 8 dB. Moreover, at V_{DS} = 10 V a peak PAE as high as 56% combined with an output power density of 1.6 W/mm has been reached.

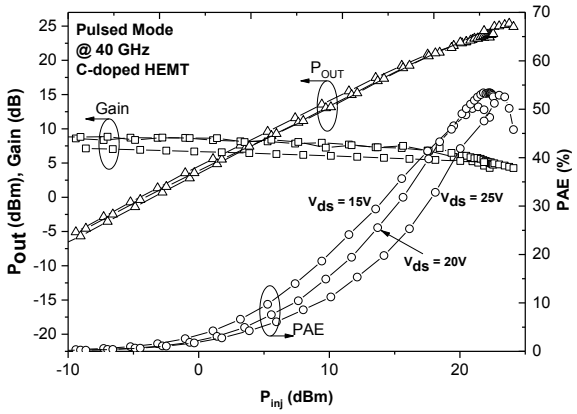


Fig. 4.1. : Pulsed power performance of a 0.12×50 µm² HEMT at 40 GHz with V_{DS} = 15, 20, 25V.

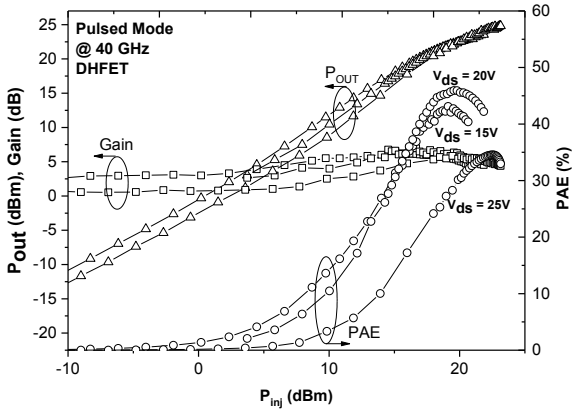


Fig. 4.2. : Pulsed power performance of a 0.12×50 µm² DHFET at 40 GHz with V_{DS} = 15, 20, 25V.

Similarly the pulsed power performance of a 0.12x50 the DHFET structure at 40 GHz can be seen in Fig. 4.2. The output power density evolves linearly as a function of the drain bias (see Fig 4.3) with no sign of saturation even at V_{DS} = 25V for both structure reflecting the high material quality and associated processing. It is worth noting that the C-doped structure shows the ability to deliver a PAE above 50% up to V_{DS} = 25V. For the DHFET, the PAE shows an increasing evolution up to V_{DS} = 20V. At V_{DS} = 15V, a PAE of 43% is obtained while a PAE of 46% associated to an output power density of 5.1 W/mm at V_{DS} = 20V. Nevertheless, at V_{DS} = 25V a degradation of performance is observed with a PAE decreasing to 35%. The significant drop of the PAE at V_{DS} = 25V can be explain by the fact that, despite the pulsed mode, the 1µs pulse width is still too large to avoid the self-heating at such a high voltage within the DHFET structure.

Consequently, the performance enhancement is attributed to the better thermal dissipation within the C-doped GaN HEMTs as compared the DHFETs. It can be noticed that no device degradation is observed in both cases as seen for instance from the absence of gate leakage current increase subsequent to the number of pulsed power sweeps up to V_{DS} = 25 V.

As can be seen from the benchmark in Fig. 4.4, the achieved PAE / P_{OUT} combination at 40 GHz compares favorably to the state-of-the-art.

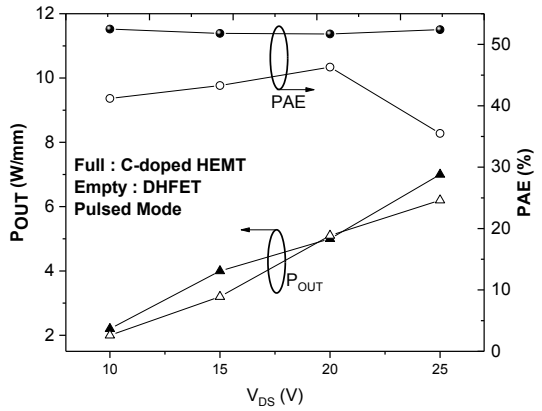


Fig. 4.3. : Pulsed output power density (triangle) and PAE (circle) versus V_{DS} at 40 GHz.

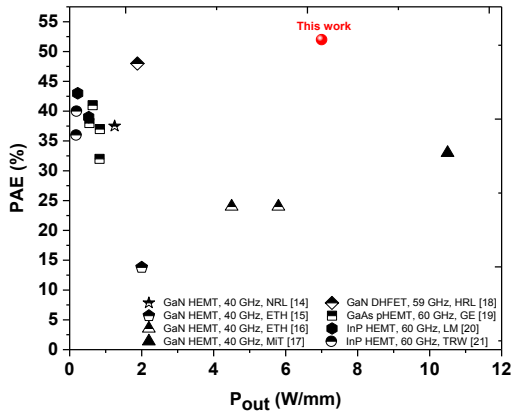


Fig. 4.4. : Benchmark of the output RF power density vs PAE for Q and V band[14][15][16][17][18][19] [20][21].

V. CONCLUSION

This work shows that a careful architecture of buffer layers should be employed in order to perform high performance millimeter-wave GaN devices. The use of higher bias operation ($V_{DS} \geq$ 20 V) will be possible while using short gate length only if the thermal resistance induced by the buffer layers is reduced. In particular, it is shown that a thick AlGaN back barrier (DHFET structure) results in a huge drop of PAE at V_{DS} = 25V despite the pulsed mode. With an enhanced thermal dissipation as compared to the DHFET, the C-doped structure delivers much higher performances illustrated by a state-of-the-art combination of PAE (> 50%) and an output power density of 7 W/mm at 40 GHz and V_{DS} = 25V.

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