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## GaN-on-silicon high-electron-mobility transistor technology with ultra-low leakage up to 3000 V using local substrate removal and AlN ultra-wide bandgap

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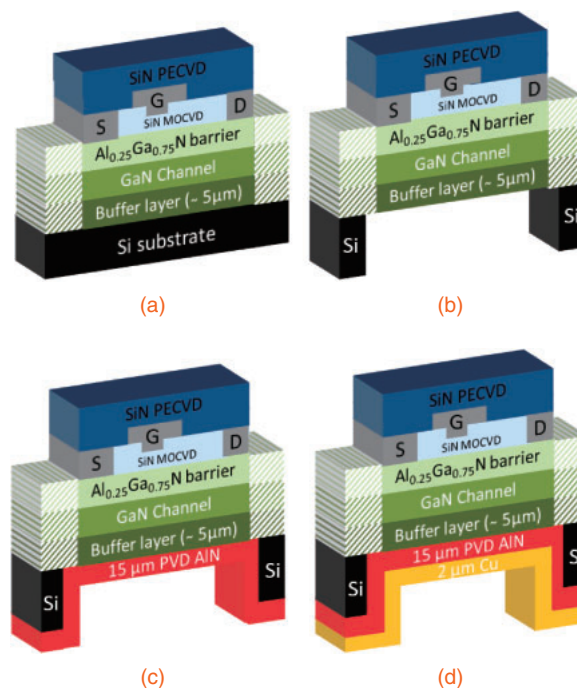
We report on extremely low off-state leakage current in AlGaN/GaN-on-silicon metal–insulator–semiconductor high-electron-mobility transistors (MISHEMTs) up to a high blocking voltage. Remarkably low off-state gate and drain leakage currents below  $1 \mu\text{A}/\text{mm}$  up to 3 kV have been achieved owing to the use of a thick in situ SiN gate dielectric under the gate, and a local Si substrate removal technique combined with a cost effective 15- $\mu\text{m}$ -thick AlN dielectric layer followed by a Cu deposition. This result establishes a manufacturable state-of-the-art high-voltage GaN-on-silicon power transistors while maintaining a low specific on-resistance of approximately  $10 \text{ m}\Omega\text{-cm}^2$ . © 2018 The Japan Society of Applied Physics

For future efficient and low-cost power electronics, GaN high-electron-mobility transistors (HEMTs) on silicon (Si) substrate are highly promising owing to their superior intrinsic properties such as large bandgap, high breakdown field strength, and high electron saturation velocity.<sup>1–9</sup> However, GaN-on-Si transistors suffer from poor critical electrical field strength of the Si substrate together with a parasitic conduction at the buffer/substrate interface leading to device breakdown.<sup>10–12</sup> Therefore, the highest reported three-terminal breakdown voltage ( $V_{\text{BD}}$ ) values for GaN-on-Si HEMTs defined at an off-state leakage current of  $1 \mu\text{A}/\text{mm}$  are still below 1.5 kV,<sup>13</sup> which is basically limited by the Si substrate and the associated material quality.<sup>14–21</sup>

To suppress the parasitic conduction phenomenon, a local Si substrate removal (LSR) was proposed in 2010.<sup>22,23</sup> The Si substrate removal around the drain electrode enabled the electrical isolation of the gate and source from the drain across the buffer layer/Si interface, leading to an enhanced blocking voltage of the GaN-on-Si HEMT above 2 kV.<sup>24</sup> Using this approach, our group reported GaN-based transistors with a significantly improved blocking voltage of 3 kV,<sup>25</sup> but still with a high leakage current that is not compatible with high-power applications.

In this paper, we report for the first time GaN-on-Si metal–insulator–semiconductor HEMTs (MISHEMTs) with LSR under the entire device followed by a backside deposition of the ultra-wide bandgap AlN material. The use of an in situ SiN gate dielectric under the gate and the LSR technique combined with 15- $\mu\text{m}$ -thick AlN layer enabled the state-of-the-art GaN-based HEMTs with remarkably low off-state leakage current ( $<1 \mu\text{A}/\text{mm}$ ) up to 3 kV.

The AlGaN/GaN/AlGaN double heterostructures were grown using metalorganic chemical vapor deposition (MOCVD) on a 6-in. Si(111) substrate. The HEMT structure consists of an AlN nucleation layer followed by AlGaN-graded transition layers and an  $\text{Al}_{0.08}\text{Ga}_{0.92}\text{N}$  buffer layer. The 5  $\mu\text{m}$  total buffer thickness was followed by a 150-nm GaN channel, a 20-nm  $\text{Al}_{0.25}\text{Ga}_{0.75}\text{N}$  barrier layer and a 50-nm in situ  $\text{Si}_3\text{N}_4$  cap layer [Fig. 1(a)]. Hall effect measurements revealed an electron sheet concentration of  $8.9 \times 10^{12} \text{ cm}^{-2}$  with a mobility of  $2190 \text{ cm}^2\text{-V}^{-1}\text{-s}^{-1}$  and a sheet resistance  $R_{\text{SH}} = 319 \Omega/\square$  at room temperature with a high uniformity of less than 4% across the wafer. Ohmic contacts were formed directly on top of the AlGaN barrier by alloying the Ti/Al/Ni/Au stack at 875 °C using rapid thermal annealing. Device isolation was achieved by  $\text{N}_2$  implantation. The metal–



**Fig. 1.** Schematic cross-section of AlGaN/GaN MISHEMT after the (a) front side process, (b) LSR technique, (c) 15- $\mu\text{m}$ -thick PVD AlN deposition, and (d) 2- $\mu\text{m}$  Cu deposition on the backside.

insulator–semiconductor (MIS) gate structure was employed by depositing the Ni/Au metal stack on the in situ  $\text{Si}_3\text{N}_4$  cap layer (30-nm-thick SiN left under the gate) without any additional field plate. A 200-nm-thick SiN film was deposited using plasma-enhanced chemical vapor deposition (PECVD) as extra passivation. Once the front-side processing was completed, the Si substrate was locally etched up to the AlN nucleation layer around the entire device (50  $\mu\text{m}$  away from the sidewalls), as shown in Fig. 1(b). It is noteworthy that our mask design consists of devices with and without LSR patterns, which eliminates any processing or epi variations during the device characterization [Fig. 2(a)]. Figure 2(b) depicts a backside view of a crack-free  $20 \times 500 \mu\text{m}^2$  GaN-based MISHEMT after the LSR technique.

Subsequently, a 15- $\mu\text{m}$ -thick AlN was deposited on the backside by physical vapor deposition (PVD) at 300 °C by Kyma Technologies. Figure 3(a) reveals the cross-sectional scanning electron microscopy (SEM) image of the 15- $\mu\text{m}$ -thick conformal AlN film. To evaluate the corresponding

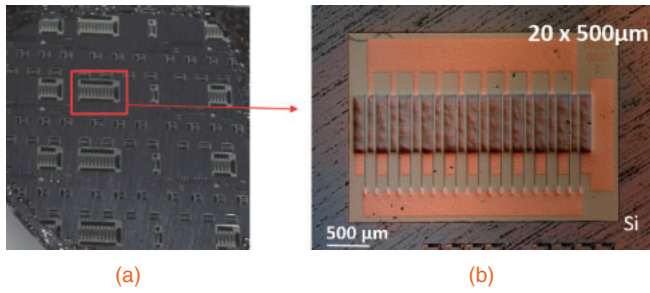


Fig. 2. Optical backside image of (a) the wafer with and without LSR removal patterns, (b)  $20 \times 500 \mu\text{m}^2$  GaN-based MISHEMT after LSR.

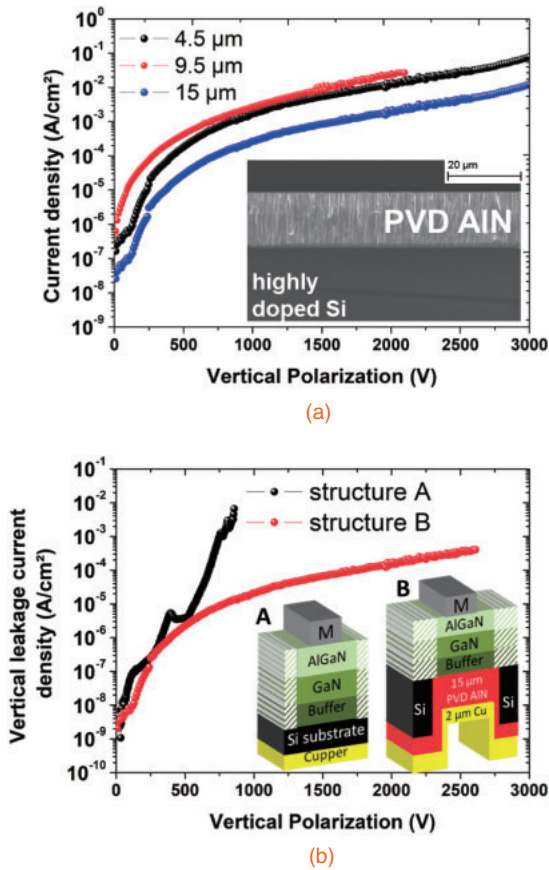
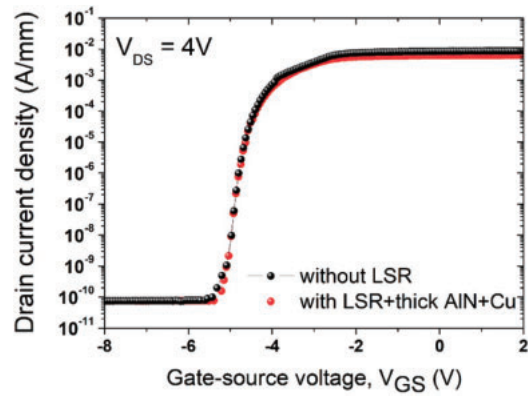
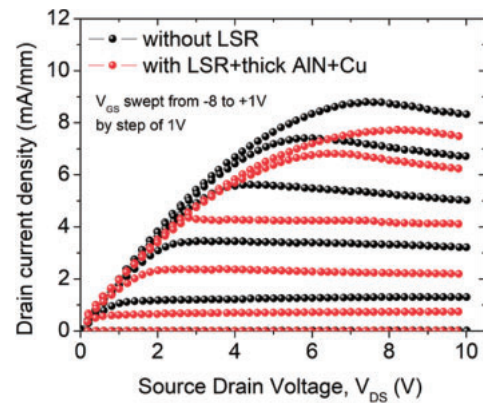


Fig. 3. Vertical leakage characteristics of (a) AlN layers deposited under the same conditions as a function of thickness on highly doped Si, and (b) AlGaIn/GaN epitaxial structures A and B, without and with LSR/backside AlN deposition, respectively. Inset: Cross-sectional SEM image of 15- $\mu\text{m}$ -thick AlN film.

breakdown voltage characteristics, several thicknesses have been deposited on a highly doped Si. The PVD AlN film delivered a high breakdown field above 4 MV/cm despite the low temperature deposition, and offers a cost-effective manufacturing technology scalable up to 8 inches, considering that the LSR approach is also applicable in large-diameter wafers. In addition, Fig. 3(b) shows the vertical leakage current measurements conducted on isolated transmission line method (TLM) patterns on structures A and B. Structures A and B correspond to the AlGaIn/GaN epitaxial designs without and with LSR/backside AlN deposition, respectively. The removal of the Si substrate combined with the backside deposition of a 15- $\mu\text{m}$ -thick AlN layer enabled a remarkable increase in the vertical breakdown from 850 V to



(a)



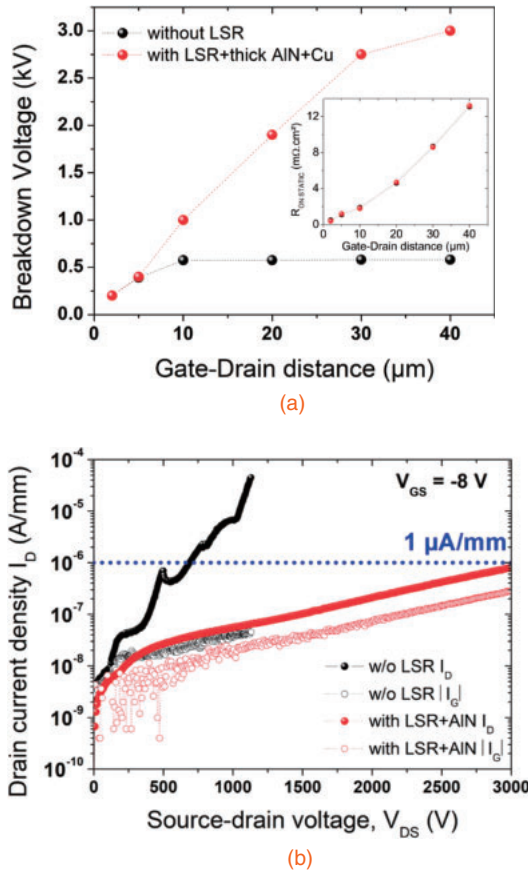
(b)

Fig. 4. (a) DC transfer and (b)  $I_D$ - $V_D$  characteristics of GaN-based MISHEMTs with  $L_{GD}$  of  $40 \mu\text{m}$  with and without LSR/backside AlN and Cu deposition.

2.6 kV, confirming the suppression of substrate conduction and the effectiveness of the dielectric film.

Electrical characterizations were carried out on devices with gate width/length =  $50 \mu\text{m}/2 \mu\text{m}$  and a gate-to-drain spacing ( $L_{GD}$ ) that varied from 2 to  $40 \mu\text{m}$  with and without LSR/backside AlN and Cu deposition on the same wafer. The DC transfer and  $I_D$ - $V_D$  characteristics of the AlGaIn/GaN MISHEMTs with an  $L_{GD}$  of  $40 \mu\text{m}$  are shown in Fig. 4. The maximum current density at  $V_{GS} = +1 \text{V}$  decreased by approximately 30% from 8.8 to 6.3 mA/mm after the Si substrate removal under the active region due to self-heating. The origin of the self-heating subsequent to substrate removal is the degradation of the thermal dissipation in air, resulting in an increase in the channel temperature, which decreases the electron mobility and thus causes a reduction in the drain current. Indeed, the devices with LSR have been recently reported to have lower thermal conductivities than those without LSR by the Raman thermometry technique.<sup>26)</sup> However, a significant recovery of the maximum current density (approximately 85%), with respect to the devices without LSR, occurs after the highly thermally conductive Cu deposition, which in turn enables the strong reduction in self-heating [Fig. 4(b)]. The static specific on-resistance ( $R_{ON-STATIC}$ ) values were extracted to be 13.1 and 13.2  $\text{m}\Omega/\text{cm}^2$  for devices with  $L_{GD} = 40 \mu\text{m}$ , without and with LSR/thick AlN and Cu, respectively. The active area of the devices with  $L_{GD} = 40 \mu\text{m}$  was calculated to be  $2.6 \times 10^{-5} \text{cm}^2$  by considering a  $5 \mu\text{m}$  transfer length for each ohmic contact (i.e., source and drain).

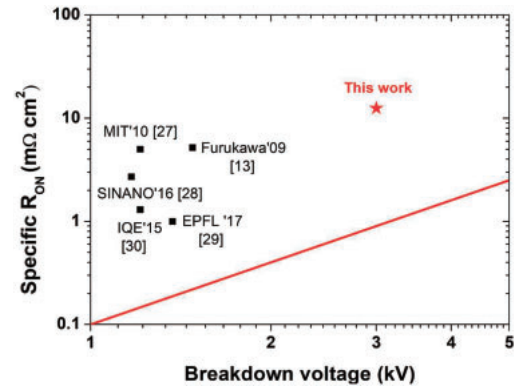




**Fig. 5.** (a) Evolution of  $L_{GD}$ -dependent device breakdown and specific on-resistance (inset) of AlGaIn/GaN HEMTs with and without LSR/thick AlN/Cu by defining blocking voltage at  $I_D = 1 \mu\text{A/mm}$ , and (b) off-state leakage current characteristics of AlGaIn/GaN MISHEMTs with and without LSR/thick AlN deposition.

Three-terminal  $V_{BD}$  measurements were conducted on various transistor designs from 2 to  $40 \mu\text{m}$  at  $V_{GS} = -8 \text{ V}$  with a floating substrate using a Fluorinert solution.  $V_{BD}$  was defined as the drain-source voltage ( $V_{DS}$ ) at which the drain current density ( $I_D$ ) reaches  $1 \mu\text{A/mm}$ . The specific on-resistances and breakdown voltages without and with LSR/thick AlN and Cu for each design are represented in Fig. 5(a). For devices without LSR,  $V_{BD}$  saturated at approximately 600 V for  $L_{GD}$  larger than  $10 \mu\text{m}$  resulting from the parasitic substrate conduction between the metal contacts and the Si substrate, regardless of the device geometry. The device breakdown occurs at the AlN/Si interface because of the lower breakdown field of Si compared to the III-nitride layers ( $E_{\text{AlN}} = 11.7 \text{ MV/cm}$  and  $E_{\text{Si}} = 0.3 \text{ MV/cm}$ ).<sup>10,11</sup> On the other hand, for devices with LSR/thick AlN and Cu, the substrate leakage contribution is suppressed and  $V_{BD}$  further increased with the gate-to-drain distance while still delivering low specific on-resistances.

The three-terminal off-state leakage characteristics of the AlGaIn/GaN MISHEMTs with and without LSR/thick AlN and Cu are plotted as a function of  $V_{DS}$  for the largest design, i.e.,  $L_{GD} = 40 \mu\text{m}$  in Fig. 5(b). The devices without LSR demonstrated an exponential increase in the leakage current at low  $V_{DS}$  bias reaching the  $1 \mu\text{A/mm}$  limit at approximately 600 V owing to the parasitic conduction through the buffer/Si substrate. For devices with LSR/thick AlN and Cu, the drain leakage current density was reduced by approximately two



**Fig. 6.** Benchmark of GaN-on-Si HEMTs with blocking voltage defined at an off-state leakage current of  $1 \mu\text{A/mm}$ .

orders of magnitude from 600 V to 3 kV, confirming the suppression of the substrate's conductive-path contribution. It is noteworthy that the off-state gate leakage ( $I_G$ ) currents of both AlGaIn/GaN MISHEMT designs, with and without LSR are below  $1 \mu\text{A/mm}$  until the device breaks down owing to the gate dielectric under the gate. Therefore, despite common perception, the drain leakage current flowing through the buffer layers is not especially due to the bulk defects/traps but is more confined at the AlN nucleation layer/Si substrate interface.

Figure 6 shows a benchmark of the GaN-on-Si HEMTs blocking voltage defined at an off-state leakage current of  $1 \mu\text{A/mm}$ .<sup>27-30</sup> The translated specific  $R_{ON}$  of  $13 \text{ m}\Omega\text{-cm}^2$  combined with a blocking breakdown voltage of 3 kV, for devices with  $L_{GD} = 40 \mu\text{m}$  sets the state-of-the-art device. These results pave the way for higher-voltage-operation GaN-on-Si power devices.

We demonstrated for the first time GaN-on-Si MISHEMTs with local Si substrate removal under the entire device followed by a low-cost backside deposition of a thick ultra-wide bandgap AlN film. Using an MIS gate structure and the LSR technique combined with a  $15\text{-}\mu\text{m}$ -thick AlN layer resulted in state-of-the-art GaN-based HEMTs with remarkably low off-state leakage current ( $<1 \mu\text{A/mm}$ ) beyond 3 kV. The comparison of these devices without LSR proves that the drain leakage current flows at the AlN nucleation layer/Si substrate interface. Furthermore, the significant recovery of the maximum current density after the backside Cu deposition enabled the reduction in self-heating. This work shows that this emerging type of devices could be useful for cost-effective applications requiring breakdown voltages above 3 kV.

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