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## **► To cite this version:**

Mouhannad Dbeiss, Yvan Avenas. Power Semiconductor Ageing Test Bench Dedicated to Photovoltaic Applications. IEEE Transactions on Industry Applications, 2019, 55 (3), pp.3003–3010. <10.1109/TIA.2019.2897681>. <hal-02350907>

**HAL Id: hal-02350907**

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Submitted on 17 May 2021

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# Power semiconductor ageing test bench dedicated to photovoltaic applications

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**Abstract**—This paper presents a new concept of semiconductor ageing test benches dedicated to photovoltaic inverters. The ageing profile is obtained by analyzing mission profiles of the current and the ambient temperature, extracted over several years from different photovoltaic plants. Accordingly, the ageing test is done by applying power cycling under variable ambient temperature, using power semiconductors in a Pulse Width Modulation inverter and under nominal conditions. The measurement and estimation of power losses and thermal models are then used to choose the ageing profile parameters adapted to the experimental setup. Finally, the preliminary experimental results of the accelerated ageing tests are presented in the case of silicon carbide MOSFETs power semiconductors. These results show a remarkable increase in the gate to source threshold voltage, the leakage currents and the drain to source on resistance.

**Keywords**—Power cycling; Photovoltaic inverter; Silicon carbide MOSFETs; Semiconductor failure indicators;

## I. INTRODUCTION

Silicon Carbide (SiC) semiconductor devices are being increasingly used in power electronic applications, mainly because of their high switching speed, which improves the overall efficiency and/or the compactness of the inverters. On the other hand, in photovoltaic systems the DC/AC inverters have the highest failure rate, and the anticipation of its breakdowns is still difficult [1]. Thus, in order to study their main failure modes in laboratories, it is crucial to propose methods allowing for an acceleration of the ageing of the inverter devices. In this context, accelerated ageing of power modules is carried out under aggravated conditions of current (power cycling) or temperature (thermal cycling) to speed up the natural ageing process. It is used to help determining in a laboratory, the long-term effects of expected levels of stress within a shorter period of time. Unfortunately, by applying the accelerated ageing, mechanisms of failures that do not occur in the real application could be observed, while inversely other mechanisms that usually occur could be not recreated [2]. Thermal cycling consists on passively cycling the devices between two extreme temperatures, and hence inducing large variations in the whole module temperature. It should be noted that during thermal cycling the whole module has approximatively the same temperature. Power cycling consists

in applying a series of current pulses, usually resulting in large variations of the junction temperature of semiconductor devices [3]-[4]. In other words, it is an active cycling, resulting in large temperature gradients inside the module. On the other hand, power cycling using the opposition method (also called back-to-back configuration) consists in cycling the power semiconductors in a single-phase PWM inverter, under nominal conditions. It is a power cycling method that induces more realistic electrical stresses on the power devices, compared with classical power cycling. The devices are fed with a regulated switched sinusoidal current with an adjustable frequency [5]. For power semiconductor devices, the operating conditions are very close to those existing in a real inverter [6]-[7]. The accelerated ageing methods mentioned above are widely used, but do not necessarily represent always the real application [8].

This paper presents a new concept of ageing test benches dedicated to photovoltaic inverters, by considering the mission profiles of the current and ambient temperature, extracted from photovoltaic plants over several years, as presented in Fig. 1. The photovoltaic data analysis leads to create accelerated ageing profiles of photovoltaic inverters RMS output current and ambient temperature. These profiles are then introduced into a power losses estimation model, coupled with a thermal model to estimate the correspondent junction temperature of the semiconductor devices, considering the electro-thermal coupling of temperature-dependent electrical parameters [3]. Then, the estimated junction temperature profiles of the semiconductors, corresponding to the accelerated ageing current profile, are used to determine the ageing profile parameters, after applying the required refinements, such as the current ageing profile's maximum value  $I_{MAX}$ , the truncation current  $I_{LIMIT}$ , the pulses durations  $T_{on}$  and  $T_{off}$ , as well as the ambient temperature's minimum and maximum values  $T_{a_{min}}$  and  $T_{a_{max}}$  respectively (cf section II).

Finally, the obtained ageing profile is applied during the new accelerated ageing test, where active and passive cycling are simultaneously done, under switching nominal conditions and pulse width modulation (PWM) operating mode. The accelerated ageing is stopped periodically in order to apply the diagnostics of the semiconductor devices, using the *Keysight B1506A* Analyzer. The purpose is to identify the potential indicators of ageing/failure of SiC MOSFET devices used in photovoltaic DC/AC inverters. This method that aims to regenerate closer constraints to those of the photovoltaic application will be depicted in the following sections, as well as some preliminary results of the accelerated ageing tests.

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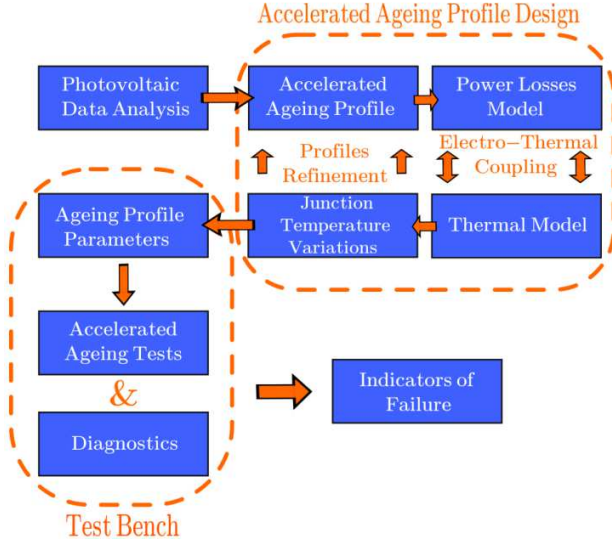


Fig. 1. Synoptic of the full study

## II. BUILDING ACCELERATED AGEING PHOTOVOLTAIC PROFILES

Older power cycling methods concentrate on packaging damages, where in every power cycling test, different degradation mechanisms occur simultaneously. Thus, depending on the power cycling method, one of these ageing processes will be more accelerated than the others. That is why it is important to apply the tests in conditions which are as close as possible to the real application.

### A. Analysis of photovoltaics' mission profiles

The aim of this study - fully depicted in [9] - is to create an accelerated ageing method, generating thermo-mechanical stresses in the semiconductors, considering the photovoltaic application. Thus, mission profiles of inverters' RMS output current and ambient temperature are extracted from multiple photovoltaic power plants located in the south of France, over several years. Due to similarities within the data, one mission profile over a single year serves as an example in this paper.

The profiles of the current and ambient temperature can show clear sky days as in Fig. 2.a or cloudy days as in Fig. 2.b. By analyzing the current profiles, several characteristics can be identified, such as the shape of the current, the slope of the current variations, the diffuse radiation, the delays between the current variations, and the ambient temperature, etc. It should be noted that the values of certain parameters may depend on the power plant's location and size. An analysis is thus required for each case.

#### 1) The shape of the current

As it can be noticed in Fig. 2.a, the shape of the RMS output current of the DC/AC inverter during the sunshine is theoretically sinusoidal. This profile depends on several parameters, such as the geographical area, the orientation of the

photovoltaic panels and many others [10]. The number of sunshine hours depends on the season as well as on the geographical zone, while no current is produced by the PV panels during the night

#### 2) The diffuse current

The minimum value that the current can reach is proportional to the diffuse solar radiation. This latter - illustrated over one day in Fig. 3 - represents the radiation that reaches the PV panels during the passage of clouds. The current produced during the passage of clouds at a given time is close to 10% of the total current that the PV panels produced directly before the passage of the clouds [11]. In other words, the amplitude of the current variation during the passage of clouds  $\Delta I$  is close to 90% of the current  $I_{clear}$ , produced before the passage of clouds.

#### 3) The slope of the current variations

During traditional power cycling tests, the variations of the current are abrupt, which may accelerate the damaging of the module, potentially in a non-representative way, since the thermo-mechanical stress may be dependent of it. In order to build a profile that accelerates the ageing of the power modules of the DC/AC photovoltaic inverter, slight current variations are neglected. Thus, only the current variations higher than  $\Delta I_{min}$  leading to  $\Delta T_j \geq 30 K$  were retained, where the value of 30 K is arbitrary selected. The value of  $\Delta I_{min}$  can be determined using a thermal model. Fig. 4 illustrates the extraction of current's considerable variations over several days represented with a red line.

Considering the available data, the maximum slope of these sudden variations is estimated to be:

$$\frac{\Delta I}{\Delta t} = 0.15 \cdot I_{MAX} \text{ (A/s)} \quad (1)$$

where  $I_{MAX}$  is the maximum RMS current reached during one year. Actually, this slope depends on wind speed and hence varies from a season to another, and depends also on the size of the photovoltaic power plant and its location.

#### 4) Delays between the current variations

As mentioned previously, only the delays between the current variations higher than  $\Delta I_{min}$  are therefore considered. The cumulative histogram illustrated in Fig. 5 represents the percentage of occurrences of the delays between these big variations, in other words the delays between two consecutive passages of clouds inducing high temperature swings. It can be seen that more than 50% of the delays are lower than 200s.

#### 5) Ambient Temperature

Ambient temperature has a sinusoidal shape during the day (without considering the night), as represented in Fig. 6, with its extreme values dependent on the geographical zone. It is noticeable that during the day, the temperature variations can be higher than 20°C.

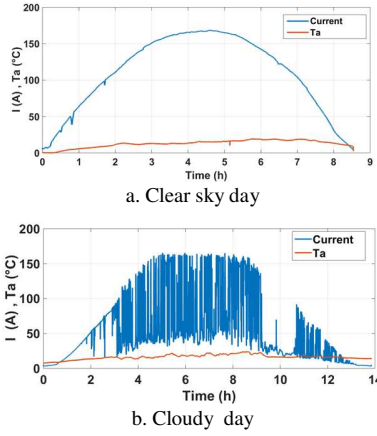


Fig. 2. Typical current and ambient temperature profiles over one day

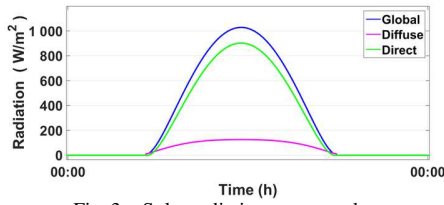


Fig. 3. Solar radiation over one day

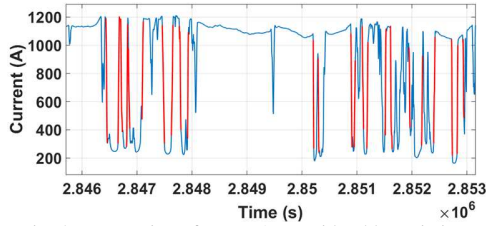


Fig. 4. Extraction of current's considerable variations

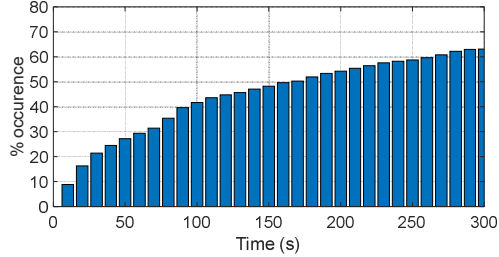


Fig. 5. Cumulative histogram of occurrences (in percentage) of the delays between two consecutive big variations of the current

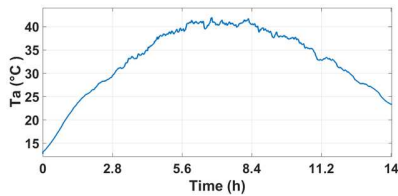
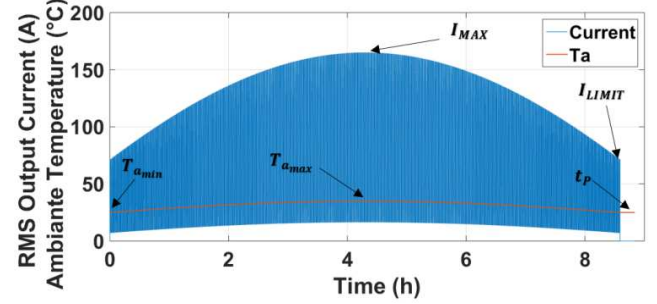


Fig. 6. Ambient temperature profile over one day

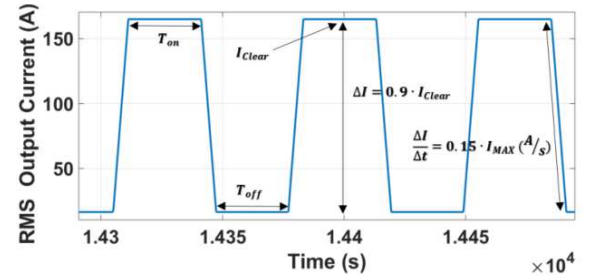
## B. Building the accelerated ageing profile

In order to build accelerated ageing profiles, current and ambient temperature mission profiles extracted from photovoltaic plants for several years were analyzed. The statistical analysis of the photovoltaic mission profiles leads to the photovoltaic profile presented in Fig. 7.a. This profile simulates one day (without considering the night). Like in real application, the global profile of the RMS output current has a sinusoidal shape, where the minimum current value at a given time is nearly 10% of the current's value, before the occurring variation (Fig. 7.b). Hence, the current variation at a given time can be expressed as  $\Delta I = 0.9 \cdot I_{Clear}$ , where  $I_{Clear}$  represents the RMS current's value before the current drop (corresponding to a clear sky). In Fig. 7.b, the slope  $\Delta I / \Delta t = 0.15 \cdot I_{MAX}$  (A/s), while  $T_{on}$  and  $T_{off}$  represent the delays between the variations.  $I_{MAX}$  represents the peak value of the RMS current.

On the other hand, it can be noticed that a truncation is applied at the two extreme sides of the profile, so that the value of the current starts at  $I_{LIMIT}$  instead of 0, to prevent the creation of  $\Delta T_j < 30$  K (by introducing  $\Delta I \geq \Delta I_{min}$ ).



a. Ageing profile simulating one day of real application



b. Zoom on several current variations

Fig. 7. Accelerated ageing profiles of the current and the ambient temperature

As it can be seen in Fig. 7.a, the ambient temperature  $T_a$  has a sinusoidal shape, varying between  $T_{a_{min}}$  and  $T_{a_{max}}$ .

The current profile is sequentially applied during the power cycling using the opposition method, by switching the semiconductors of the inverter using the PWM. A pause of  $t_p = 15$  minutes is made between two consecutive profiles to allow for the relaxation of the viscoelastic constraints in the power module [12]-[13]. It should be noted that the methodology suggests applying the same profile along the accelerated ageing test, without considering the increase of the thermal resistance. Actually, in the photovoltaic application this latter increases

gradually due to the natural ageing of the modules and accelerates the ageing process.

As presented in Fig. 1, once the accelerated ageing profile is defined, it is then introduced into power losses and thermal models. Next, a cycle counting algorithm is appointed to extract the cycles from the junction temperature profiles  $T_j$ , as well as the temperature swings  $\Delta T_j$  of each extracted cycle, and the corresponding mean temperature of each temperature swing  $T_{jM}$ . Then, the ageing profiles parameters are determined according to the desired maximum junction temperature  $T_{jMAX}$ .

### III. EXPERIMENTAL SETUP

In order to conduct this study, a two-level DC/AC single-phase inverter was designed, implementing SiC MOSFET power modules APTMC120AM16D3AG (1200V-136A phase-leg power modules without antiparallel diodes). The inverter uses a water-cooled heat sink and 4x420  $\mu$ F DC-link capacitors ( $C_{bus}$ ) and 2x1  $\mu$ F decoupling capacitors ( $C_{dec}$ ), with a DC bus voltage  $E = 750$ V. The equivalent electrical circuit of the inverter is presented in Fig. 8.

The opposition method was implemented using LabVIEW; one FPGA core of a PXI system (National Instruments) drives the MOSFETs as well as the DC-link power source, and controls the coolant fluid temperature. Two pre-driver electronic boards were designed to adapt the output signals of the PXI, since the used drivers PT62SCMD12 (Cree) accept only differential input signals. Moreover, two LEM current transformers HAS 100-S were used for the closed loop control of the load current, where the load is a 130  $\mu$ H inductor. Fig. 9 shows the inverter prototype, whereas Fig. 10 represents the global accelerated ageing test bench.

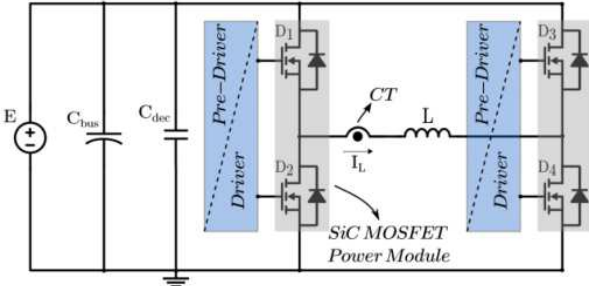


Fig. 8. Equivalent electrical circuit of the inverter

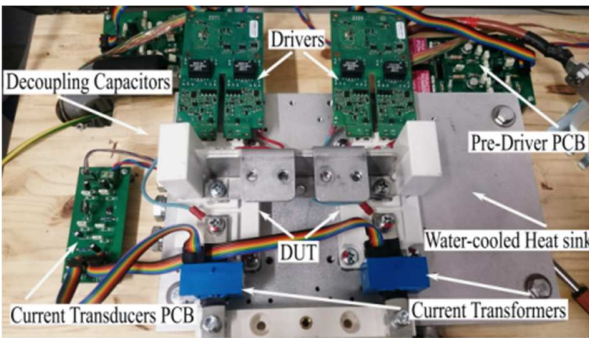


Fig. 9. Inside of the inverter

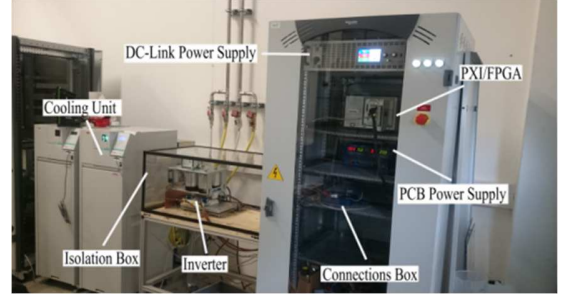


Fig. 10. Global test bench

### IV. DETERMINATION OF AGEING PROFILE PARAMETERS

#### A. Objective

Once the accelerated ageing profile presented in Fig. 7 is designed, and before starting the ageing tests campaign, the parameters of this profile should be determined in order to obtain the desired junction temperature of each semiconductor. These parameters are the current ageing profile's maximum value  $I_{MAX}$ , the truncation current  $I_{LIMIT}$ , the pulses durations  $T_{on}$  and  $T_{off}$ , as well as the ambient temperature's minimum and maximum values  $T_{amin}$  and  $T_{amax}$  respectively. In order to obtain these parameters, the current and the ambient temperature profiles are introduced into power losses and thermal models, as it will be described in the following sections.

#### B. Losses estimation [4]-[14]-[15]

In order to estimate the conduction losses of the MOSFET, the Drain-Source on-state resistance  $R_{DSon}$  is extracted from datasheet, given as a function of the current level and the MOSFET junction temperature. Similarly, the conduction power losses of the MOSFET's intrinsic body diode can be obtained by extracting the value of its threshold voltage  $E_0$  and its dynamic resistance  $R_D$  from datasheet. However, the values of these parameters were verified with the B1506A analyzer (Keysight).

The MOSFET switching power losses can be estimated by multiplying the switching energy losses  $E_{on}$  and  $E_{off}$  by the switching frequency  $f_{sw}$ , and similarly for the diodes using reverse recovery losses  $E_{rec}$ . Usually, these energy losses are given in the datasheet, however  $E_{rec}$  is not provided for this power module. Despite this, the reverse recovery energy of the MOSFET's body diode was found to be low in several recent studies [16-18]. Hence in order to verify this theory and obtain more accurate values of  $E_{on}$  and  $E_{off}$ , the double pulse test was applied. In fact, the switching processes are affected by the parasitic connection inductances. They induce transient overvoltages and may cause oscillations due to the circuit and transistor capacitances [4], thus it is more accurate to directly measure the switching losses in the inverter that will be used during the accelerated ageing test.

The tests were applied for the following load current values  $I_{Load} = 10$ A, 30A, 45A, 60A, 90A and 120A, and for two junction temperatures  $T_j = 25$  °C and 100 °C. These latter are estimated by measuring at thermal equilibrium the water-cooled heat sink's temperature directly under the dies using



thermocouples. It is therefore considered that the junction temperature increase during the tests is low, which was verified by using manufacturer data (thermal impedance curve). Fig. 11 represents the turn-on, the turn-off and the recovery energy losses ( $E_{on}$ ,  $E_{off}$  and  $E_{rec}$  respectively) as a function of the load's current, all for  $T_j = 25^\circ\text{C}$  and  $100^\circ\text{C}$ . It can be seen that  $E_{rec}$  is largely lower than the other switching energies and seems to confirm the results proposed in [16-18].

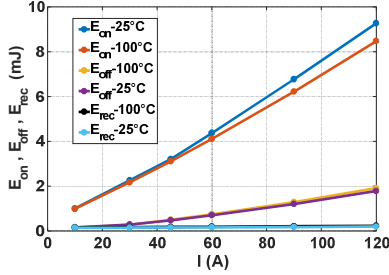


Fig. 11. Turn-on, turn-off and recovery energy losses respectively as a function of the load current, all for  $T_j = 25^\circ\text{C}$  and  $100^\circ\text{C}$

### C. Thermal model identification

The thermal model uses Foster networks since the fitting of the measured thermal impedance curves is easier with this equivalent circuit type, rather than with Cauer networks. Its equivalent thermal impedance can be expressed as follows:

$$Z_{th}(t) = \sum_{i=1}^{i=N} R_{thi} \cdot (1 - e^{-\frac{t}{\tau_i}}) \quad (2)$$

where  $R_{thi}$  is one elementary thermal resistance of the model,  $\tau_i$  one elementary time constant ( $\tau_i = R_{thi} \cdot C_{thi}$ ), while  $N$  is the number of  $R$ - $C$  cells in the model. In order to consider the thermal coupling between the semiconductor devices, the junction temperature of the different devices can be estimated, using the following matrix:

$$\begin{pmatrix} T_{j1} \\ T_{j2} \\ T_{j3} \\ T_{j4} \end{pmatrix} = \begin{pmatrix} Z_{11} & Z_{21} & Z_{31} & Z_{41} \\ Z_{12} & Z_{22} & Z_{32} & Z_{42} \\ Z_{13} & Z_{23} & Z_{33} & Z_{43} \\ Z_{14} & Z_{24} & Z_{34} & Z_{44} \end{pmatrix} \cdot \begin{pmatrix} P_1 \\ P_2 \\ P_3 \\ P_4 \end{pmatrix} + T_A \cdot \begin{pmatrix} 1 \\ 1 \\ 1 \\ 1 \end{pmatrix} \quad (3)$$

However, a series combination between Foster networks of the power module and the cooling unit, using the values of  $R$ - $C$  cells provided in the datasheets, will lead to non-negligible errors in  $T_j$  estimation [19]. Thus, a thermal model of high precision can only be achieved by a direct measurement of the Junction-Ambient self-heating thermal impedances, as well as a measurement of all the mutual thermal coupling impedances existing between the semiconductor devices.

The thermal impedances measurement was done using a Thermo-Sensitive Electrical Parameter (TSEP) [3]-[20]. The chosen TSEP was the forward voltage under low current of the

MOSFET's intrinsic body diode  $V_f$ , while blocking the MOSFETs' gates with high precision voltage sources of  $-2\text{V}$  [21].

The results showed that the mutual thermal coupling impedances between the semiconductor devices inside the same power module cannot be neglected, thus it is crucial to consider the thermal coupling between the semiconductors, in order to accurately build its thermal model. Finally all the thermal impedances were fitted with the Least Squares Methods, as presented in Fig. 12, where  $Z_{thii}$  represents the Junction-Ambient self-heating thermal impedance of the device  $D_i$ , whereas  $Z_{thji}$  represents the mutual thermal coupling impedance between devices  $D_j$  and  $D_i$ .

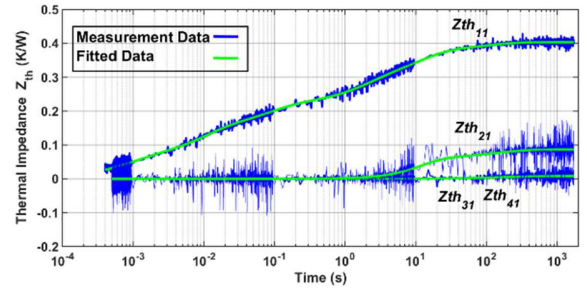


Fig. 12. Fitting the thermal impedances of MOSFET  $D_i$  (see Fig. 8)

### D. Junction temperature estimation

A power losses model was built with *Matlab* in order to estimate both the conduction and the switching losses of the semiconductor devices [4]-[14]. Having current profiles with high number of samples, only the average losses within a fundamental period  $T_{out} = 20\text{ms}$  were calculated [15]. The power losses model is presented in details in [14], in the case of a two-level PWM DC/AC inverter. The resulting losses are then introduced into a thermal model to estimate the correspondent junction temperature of the semiconductor devices. The power losses and the thermal models are coupled together in order to take into account the dependence of  $R_{DSon}$ ,  $E_0$ ,  $R_D$ ,  $E_{on}$ ,  $E_{off}$  and  $E_{rec}$  on the junction temperature.

Having accelerated ageing profiles with more than 1.5 million samples each and a complex thermal model of 16 thermal impedances, the junction temperature estimation of each device becomes very time-consuming. Hence, in order to reduce the calculation time, six  $T_j$  calculation methods using equivalent combined circuits of Foster networks were implemented and compared in terms of execution time and the ability to consider the electro-thermal coupling. These methods are: time-domain estimation [22], fast Fourier transform FFT [23], FFT with overlap-add method [24], breaking down mission profile into single pulses [20], and finally an analytical solution [25]. These methods provided the same output results, which allowed to validate them. As a conclusion, the analytical solution presents the highest performance in term of execution time (only several seconds), mostly with very long mission profiles ( $>10^6$  time samples) and complicated systems with

multiple power modules (64 convolution products), where the thermal coupling effect between the modules is considered.

The measured impedances are then implemented in the thermal model of the SiC MOSFET DC/AC inverter, and the junction temperature corresponding to the ageing profile can be thus estimated using (3). Finally, the ageing profile parameters presented in Fig. 7 were then determined as presented in TABLE I after several refinements, correspondingly to the desired maximum junction temperature  $T_{j\_MAX}$  that should be approximately equal to 125 °C (since the employed MOSFETs withstand a maximum junction temperature of 150 °C). Fig. 13 demonstrates a highlight on the resulting estimated junction temperature profiles of all the devices, when  $\Delta T_j$  is maximum.

TABLE I. AGEING PROFILE PARAMETERS

Parameter	$I_{MAX}$	$I_{LIMIT}$	$T_{on}$	$T_{off}$	$T_{amin}$	$T_{amax}$	$t_p$
Value	90A	60A	30s	30s	10°C	40°C	15min

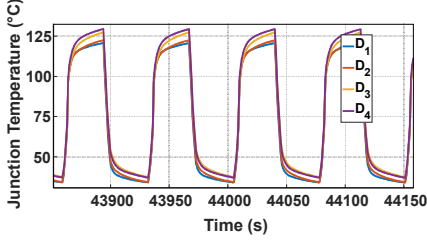


Fig. 13. Highlight on the resulting estimated junction temperature profile for all the devices

## V. ACCELERATED AGEING TESTS' RESULTS

The accelerated ageing is stopped periodically to apply the diagnostics of the semiconductor devices after disconnecting them, using the *Keysight B1506A* analyzer, while fixing the DUT temperature using a *Thermo Stream*, as represented in Fig. 14. This is a complicated and time-consuming process and can be automated in the future. However, the purpose is to monitor the maximum number of electrical parameters, in order to determine the ones that could be considered as indicators of ageing/failure of SiC MOSFET power modules, used in DC/AC photovoltaic inverters. Hence, the monitored electrical parameters are: the gate leakage current  $I_{GS}$ , the drain to source on resistance  $R_{DSon}$ , the gate to source threshold voltage  $V_{GSth}$ , the drain leakage current  $I_{DSS}$ , the drain to source on voltage  $V_{DSon}$ , the body diode forward voltage  $V_{SD}$ , the input capacitance  $C_{iss}$ , the output capacitance  $C_{oss}$  and the reverse transfer capacitance  $C_{rss}$ . It should be noted that a carbon sheet is used as thermal interface between the water-cooled heat sink and the MOSFETs, which are fixed with a constant tightening torque of 5 N.m, in order to prevent any change in the thermal behavior of the system, while disconnecting the MOSFETs.

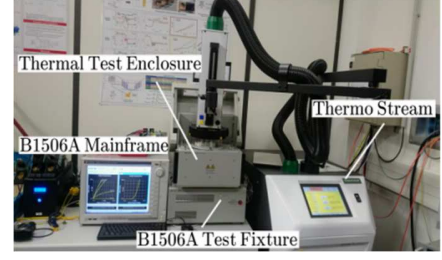


Fig. 14. Monitoring the electrical parameters using the *B1506A* Analyser with the *Thermo Stream*

The tests lasted for 864 h, until the gate of MOSFET  $D_4$  became uncontrollable by the driver, and  $R_{DSon}$ 's derivation of MOSFET  $D_3$  exceeded the threshold value of 20%. The evolution of the monitored parameters measured at  $T_j = 25$  °C is represented in the following figures as a function of time.

Fig. 15 represents the evolution of the gate-source threshold voltage  $V_{GSth}$  of the MOSFETs as a function of cycling time.  $V_{GSth}$  increases gradually by approximately 6.5%, 5%, 9% and 9.5% respectively in the case of  $D_1$ ,  $D_2$ ,  $D_3$  and  $D_4$ . Usually, the gate threshold voltage  $V_{GSth}$  is considered as indicator of gate oxide based failures, due to interfacial charge trapped in the case of SiC-based devices at and near the SiC-SiO<sub>2</sub> inversion channel-gate insulator interface [26]. A derivation of 20% in gate threshold voltage is considered as failure criterion in [27]. This can lead to significant degradation in the device's reliability and performance by shifting the threshold voltage and substantially reducing the effective channel mobility, due to coulombic scattering of the free carriers which are themselves reduced by charge trapping.

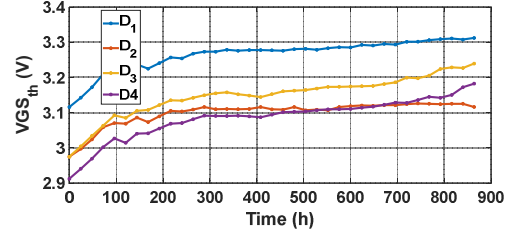


Fig. 15. Evolution of  $V_{GSth}$  as a function of cycling time

Similarly Fig. 16 represents the evolution of the gate leakage currents  $I_{GS}$  of the MOSFETs as a function of cycling time. It can be clearly seen that in the case of  $D_4$  it increases sharply due to gate's oxide failure.

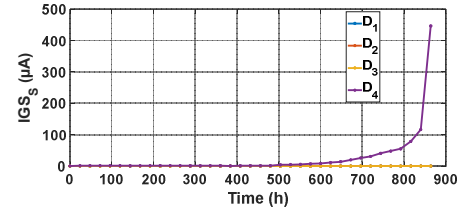


Fig. 16. Evolution of  $I_{GS}$  as a function of cycling time

Fig. 17 represents the evolution of the drain leakage current  $I_{DSs}$  as a function of cycling time. This parameter decreases a tiny bit gradually during 264 h for all MOSFETs, then increases abruptly of approximately 300%, 63%, 240% and 73% for  $D_1$ ,  $D_2$ ,  $D_3$  and  $D_4$  respectively. Then, it continues to increase gradually to reach at the end of the test approximately 800%, 100%, 1800% and 600% in the case of  $D_1$ ,  $D_2$ ,  $D_3$  and  $D_4$  respectively. A damage of a single cell in the MOSFET would lead to an increase in the drain leakage current, while the carriers can leak between source and drain terminals of a MOS (subthreshold conduction) [28].

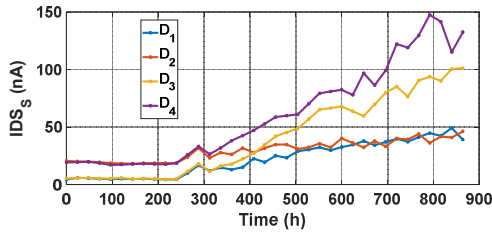


Fig. 17. Evolution of  $I_{DSs}$  as a function of cycling time

Similarly, Fig. 18 represents the evolution of the MOSFETs drain-source on-state resistance  $R_{DSon}$  as a function of cycling time. This parameter increases gradually to reach approximately 15%, 17%, 22% and 7% for  $D_1$ ,  $D_2$ ,  $D_3$  and  $D_4$  respectively. Accordingly, the value of  $R_{DSon}$  in the case of MOSFET  $D_3$  crosses the commonly used threshold value, corresponding to an increase of 20% above the initial value. The increase of this parameter can be considered as indicator of the wire bonding lift off, a reconstruction of the metallization surface [3]-[29], a decrease in device's thermal performances, and/or a degradation of the die given that  $V_{GSth}$  has also increased. It should be noted that  $V_{SD}$  showed close evolution as that of  $R_{DSon}$ , being not represented here.

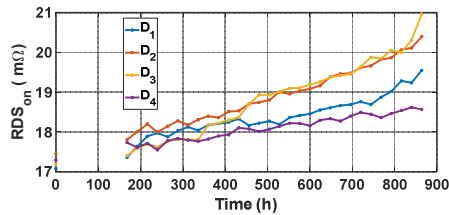


Fig. 18. Evolution of  $R_{DSon}$  as a function of cycling time

Table. II summarized the results obtained, exhibiting the minimum and maximum variations of the electrical parameters, as well as their corresponding threshold values.

TABLE II. VARIATIONS OF THE ELECTRICAL PARAMETERS AND THEIR CORRESPONDING THRESHOLD VALUES

Electrical parameter	Variation (%)		Threshold
	Minimum	Maximum	
Gate leakage current $I_{GSs}$	75 %	51570 %	+ 100% above the upper limit

Gate leakage current $I_{GSs(-)}$	-2.5 %	-12.5 %	+ 100% above the upper limit
Gate to source threshold voltage $V_{GSth}$	4.74 %	9.28 %	$\pm$ 20% of the limits
Drain leakage current $I_{DSs}$	125.8 %	1800 %	+ 100% above the upper limit
Drain to source on resistance $R_{DSon}$	7.37 %	22.01 %	+ 20% of start value
Input capacitance $C_{iss}$	-0.28 %	-0.62 %	---
Output capacitance $C_{oss}$	0.16 %	0.78 %	---
Reverse transfer capacitance $C_{rss}$	0.31 %	2.67 %	---

## VI. CONCLUSIONS AND PERSPECTIVES

As already presented in [30], this paper depicts a new concept of ageing test bench dedicated to photovoltaic inverters, where the accelerated ageing test reproduces a typical profile of the photovoltaic inverters RMS output current. The current profile was obtained by analyzing the mission profiles of the current and the ambient temperature, extracted over several years from different photovoltaic plants [9]. The profile was then introduced into a power losses estimation model, coupled with a thermal model to estimate the correspondent junction temperature of the semiconductor devices, in order to determine the profile parameters. Finally, the obtained ageing profile was applied during the accelerated ageing test, where active and passive cycling were simultaneously done, under switching nominal conditions and pulse width modulation (PWM) operating mode. The accelerated ageing was stopped periodically, in order to apply the diagnostics of the semiconductor devices, using the *Keysight B1506A* Analyzer. According to the results obtained,  $R_{DSon}$ ,  $I_{DSs}$ ,  $I_{GSs}$  and  $V_{GSth}$  showed the most remarkable variations during the accelerated ageing tests.

Actually, the main purpose of this study was to apply the tests in a real test bench, in order to check their feasibility, duration and complexity, as well as to find potential indicators of failure corresponding to this type of tests. Thus, being new, the accelerated ageing tests presented in this chapter were applied for a preliminary check. Hence, a campaign of tests has to be executed in the future on the same device type as well as on others to check if similar results could be obtained.

These tests have demonstrated comparable duration to that of a classical power cycling, while they are expected to show more representative results, leading to reduce the favoring of certain failure modes to the detriment of others. Therefore, in the future, it would be of high interest to apply classical power cycling to the same devices to compare the obtained indicators variations and failure mechanisms. Thermal parameters such as thermal resistance should also be measured during the cycling time. This work has also to be pursued by further investigation of failure mechanisms analysis with different



techniques as scanning acoustic microscopy or scanning electron microscopy.

#### ACKNOWLEDGMENT

Authors would like to thank ANR agency (MEMPHIS ANR-13-PRGE-0005-01 PROGELEC project and State Program Investment for the Future ANR-10-ITE-0003) for financial support brought for these researches.

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