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Halide perovskite high-k field-effect transistors with dynamically reconfigurable ambipolarity

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Despite the remarkable optoelectronic properties of halide perovskites, achieving reproducible field effect transistor (FET) action in polycrystalline films at room temperature has been challenging and represents a fundamental bottleneck for understanding electronic charge transport in these materials. In this work, we report halide perovskite-based FET operation at room temperature with negligible hysteresis. Extensive measurements and device modeling reveal that incorporating high-k dielectrics enables modulation of the channel conductance. Furthermore, continuous bias cycling or resting allows dynamical reconfiguration of the FETs between p-type behavior and ambipolar FET with balanced electron and hole transport and an ON/OFF ratio up to 10^4 and negligible degradation in transport characteristics over 100 cycles. These results elucidate the path for achieving gate modulation in perovskite thin-films and provide a platform to understand the interplay between the perovskite structure, and external

stimuli such as photons, fields and functional substrates, which will lead to novel and emergent properties.

The field effect transistor (FET) is a fundamental component for realizing modern digital integrated circuits. It is also often utilized as a platform to evaluate lateral charge transport and (opto-)electronic transport properties in isotropic materials and for the investigation of new emergent properties by electrostatically doping the material, which are otherwise not easily accessible. Halide (or organic-inorganic) perovskites (HaP) have emerged as solution-processed semiconductors with outstanding properties for optoelectronics including low effective mass, high carrier mobility-lifetime product, weak exciton binding energy at room temperature, unusually high defect tolerance, and low trap density.^{1–12} These characteristics have raised widespread interest in their exploration for optoelectronic devices, such as solar cells leading to high power conversion efficiency values exceeding 24%,^{13–16} radiation detectors (Gamma and X-rays) and optically pumped lasers.^{7,17–22} Despite such unprecedented progress, several riddles remain to be solved including fundamental details of charge transport mechanisms in halide perovskite thin-films.^{10,23} Additionally, recent discoveries have highlighted the important role of external stimuli such as electromagnetic radiation and electric field on the structural dynamics,^{11,23,24} which in turn strongly impacts the disorder and charge transport in hybrid perovskites. The dynamic nature of the material also provides opportunities to understand and unravel new physical phenomena that couple charge transport, structural dynamics, electric field and light. FETs are an excellent platform for the elucidation of new physical properties such as electric-field induced Rashba splitting and for the realization of novel perovskite devices, spin transistors and in general gate-induced doping of the soft perovskite lattice.

While there has been some pioneering previous works on using 2D HaP as an active material for FETs^{25,26}, there exist limited reports on 3D HaP-based FETs and attest to the

challenges of building a FET that operates at room temperature (RT). Recent work on 3D HaP FETs is summarized below. Chin et al.²⁷ reported methyl ammonium lead triiodide (MAPbI₃) hybrid perovskite-based FETs that had to be operated at low temperature to overcome screening of carriers due to ionic impurities, which otherwise prevented FET operation at RT. Other reports on perovskite FETs have revealed a processing dependent n- or p-type doping of perovskites thus making it difficult to probe the intrinsic properties and charge transport.^{23,28} Moreover, halide perovskite-based FETs have also been reported to exhibit significant hysteresis in the current-voltage transfer characteristics during device operation, with rapid degradation, which can strongly compromise their transport properties.^{27–30} Zeidell et al shows that FETs with mobilities approaching 10 cm²/V-sec can be obtained by using a solvent vapor approach to passivate the grain boundaries in Methyl ammonium lead iodide (MAPbI₃) based HaP FETs. More recently, Yusoff et al, demonstrated ambipolar FETs using triple cation 3D perovskites, although the origin of ambipolarity was not described. Ambipolar FET behavior was also observed by Amassian and co-workers³¹, in FET devices made with few microns thick MAPbI₃/Br₃ single crystals. However, the observation of ambipolarity for a large band-gap semiconductor (perovskite bandgap is larger than 1.55 eV) with symmetric source and drain gold contacts is surprising for the choice of dielectrics (PMMA and SiO₂) as the applied gate field is not large enough to tune the Fermi energy across the large band-gap and thereby switch from p- to n-type conduction. Moreover, in the work by Yusoff et al, the output characteristics appear to be anomalous as they show a square-law drain current scaling with gate overdrive (typical of long channel FETs) for the p-type curves and, at the same time, a linear scaling (typical of short channel FETs) for the n-type. Such scaling typically spans different generations of FETs technologies and there is no discussion on the physical origin of the PFET and NFET behavior. All of these recent reports on demonstrating a working 3D halide perovskite FET use a wide range of device designs and configurations, which further motivates the investigation of

3D HaP based FET studies to understand the working mechanism. Furthermore, the near intrinsic doping density^{4,6,32}($\sim 10^{16}/\text{cm}^3$) should facilitate either p-type or n-type transport with the appropriate choice of metal contacts and therefore energy band alignment with respect to the valence or the conduction band. However, in most cases, interface traps pin the Fermi-level and prevent the effective modulation of the conductance by means of a capacitively coupled gate electrode. Therefore, the ability to modulate the conductance in halide perovskites using an FET geometry remains challenge depending on a carefully designed architecture. Moreover, there has been no report on using high-K dielectrics such as hafnium oxide (HfO_2) or silicon nitride (Si_3N_4), for HaP FETs. Such a study is important for both the elucidation of the charge transport properties in complex perovskite device architectures and to enable the discovery of novel and emergent physical phenomena, which may lead to multifunctional devices.

In this paper, we report halide perovskite-based FETs with good gate modulation at room temperature without the need of preconditioning steps such as light soaking. We demonstrate reproducible electrostatic gating with p-type modulation of the channel conductance with negligible hysteresis. Furthermore, a novel aspect of the FETs is that after continuous bias cycling, the as fabricated p-type devices progressively transform into ambipolar FETs, where the perovskite Fermi energy can be successfully modulated by the gate voltage allowing the balanced transport of both electrons and holes with greater than four orders of magnitude gate modulation in the channel conductance. Analysis with different dielectrics such SiO_2 , Si_3N_4 and HfO_2 reveals that the fundamental challenge for the demonstration of perovskite-based FETs operation at RT is the screening of the gate electric field by ionic vacancies. Density functional theory simulations show that the $\text{MAPbI}_3/\text{HfO}_2$ interface corresponds to the ideal band alignment configuration for a gate/channel interface in a FET device. Through device characterization coupled with quantitative device modeling, we show that such effects can be overcome by combining high-quality perovskite thin films with high-

K dielectrics, thus allowing for the complete inversion of the channel. Our results elucidate the demonstration of hybrid perovskite-based FETs, enabled by the presence of high-K dielectrics and pave the path towards the understanding of transport mechanisms in hybrid perovskites-based FETs as a platform.

Results

Perovskite-based FET operation at room temperature. The FETs were fabricated using the architecture illustrated in Fig. 1a where the main conduction channel is composed of methylammonium lead iodide (MAPbI₃) organic-inorganic (hybrid) perovskite. Briefly, we used the previously developed hot-casting method^{5,33,34} to grow large grain-sized crystalline thin-films (400 nm thick) on top of a heavily doped Si wafer with a 30-nm thick layer of hafnium oxide film (HfO₂, dielectric constant ~23, experimental details are given in the Supplementary Note 1) and pre-evaporated gold contact electrodes. The characteristics of the FETs measured in the dark at room temperature and all measurements are performed using a DC bias and are reported in Fig. 1b-e. The gate voltage (V_G or gate bias) dependent drain current (I_D) shows field effect modulation with p-type behavior (Fig. 1b-d), i.e. the FET turns ON only for negative V_G in the operating range of gate bias without failure of the device.

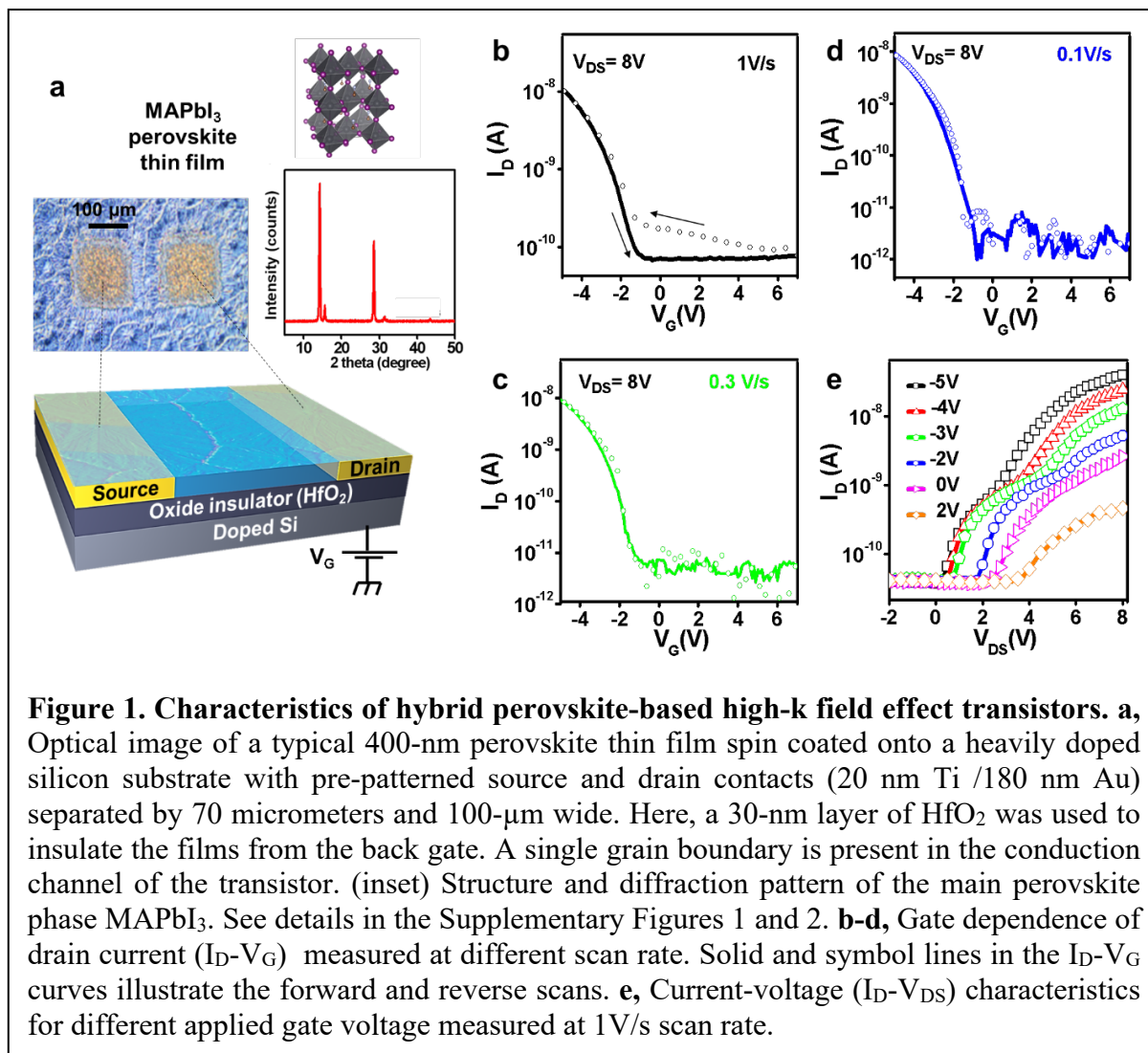


Figure 1. Characteristics of hybrid perovskite-based high-k field effect transistors. a, Optical image of a typical 400-nm perovskite thin film spin coated onto a heavily doped silicon substrate with pre-patterned source and drain contacts (20 nm Ti /180 nm Au) separated by 70 micrometers and 100-μm wide. Here, a 30-nm layer of HfO₂ was used to insulate the films from the back gate. A single grain boundary is present in the conduction channel of the transistor. (inset) Structure and diffraction pattern of the main perovskite phase MAPbI₃. See details in the Supplementary Figures 1 and 2. **b-d,** Gate dependence of drain current (I_D - V_G) measured at different scan rate. Solid and symbol lines in the I_D - V_G curves illustrate the forward and reverse scans. **e,** Current-voltage (I_D - V_{DS}) characteristics for different applied gate voltage measured at 1V/s scan rate.

To confirm that our devices are truly hysteresis-free we measured the FET device performances as a function of V_G scan speed and observed that the forward and reverse gate bias scan overlap with one another (Fig. 1b-d). The gate leakage current was dynamically monitored during the measurements and remained two orders of magnitude or more below the current when the channel is ON under the normal operating conditions, with an average value of about 30 pA (Supplementary Figure 1). The lack of hysteresis observed here for the large-grain thin films is consistent with previous results demonstrating that reducing the number of grain boundaries (here we have only one, Fig. 1a) results in a reduction of ionic transient motions and hysteresis effects.^{5,35} We verified the detrimental effect of grain boundaries by first, studying the perovskite FET as a function of channel length (Supplementary Figure 2)

which has a strong impact on the device performances. This is mainly due to the dimension of the channel length being strongly correlated to the number of grain boundaries across the channel, which results in higher charge decay rate inside the perovskite channel and thus lower device performances.

Second, we used a planar p-i-n junction architecture to measure the spatial distribution of the photocurrent and electroluminescence in the perovskite thin films (Supplementary Figure 3). We observe a dramatic reduction of both the photocurrent and electroluminescence at the grain boundaries as compared to inside the grain which can only be explained by defect-induced charge losses at boundaries, under the reasonable assumption that grains and grain boundaries have similar optical absorption.⁴ Recent studies have also reported that ionic motion which is believed to be at the origin of part of hysteresis in perovskite solar cells, is enhanced at grain boundaries.^{36,37} These results demonstrate that the presence of a single grain boundary in the conduction channel of our perovskite FET devices is advantageous to minimize hysteresis effects and to achieve gate field effect at room temperature.

We attributed our ability to obtain reproducible thin-film perovskite FET devices operating at room temperature not only to the reduction of the number of grain boundaries in the conduction channel to one as discussed above, but also to the use of a high dielectric constant material (HfO_2 dielectric constant ϵ is 23.5) as oxide insulator in our metal-oxide-FET architecture. Indeed, FETs using low dielectric constant materials such as SiO_2 ($\epsilon \sim 3.9$) or Si_3N_4 ($\epsilon \sim 7.5$) constantly yield devices with lower performances and larger hysteresis (Supplementary Figure 4 and Table 1). We observe both a smaller gate modulation of the current and a n-type FET characteristic for devices made with SiO_2 or Si_3N_4 suggesting that the technique used to deposit gate insulator may play an important role in terms of interface defects leading to a defect-induced carrier transport (details on the preparation of the FETs are given in Supplementary Table 5 to 8).

Table 1. Performances of MAPbI₃ perovskite FETs using different oxide layers. The I_D-V_G characteristics are plotted in the Supplementary Figure 4. ϵ is the oxide layer dielectric constant and EOT stands for the equivalent oxide thicknesses indicating the equivalent SiO₂ layer needed to produce the same effect as the high-k oxide materials.

Oxide layer	ϵ	EOT (nm)	Conductance (nA/V)	ON/OFF ratio	Threshold field (V/cm)	Hysteresis area (a.u.)
SiO ₂	7.5	100	0.02	$\sim 10^2$ (n-type)	3	1
Si ₃ N ₄	3.9	52	0.05	10^2 - 10^3 (n-type)	1	0.4
HfO ₂	23.5	5	4.90	10^2 - 10^4 (p-type)	0.5	0.1

Next, the current-voltage characteristics (I_D-V_{DS}) as a function of applied gate bias was measured (Fig. 1e) exhibiting a typical exponential response³⁸, which is indicative of a Schottky barrier in our FET. Consistent with the p-type behavior observed from the I_D-V_G characteristics described above (Fig. 1b), I_D increases from 0.4 nA to 40 nA for gate bias varying between 2V to -5V. Surprisingly, we observe a decrease of the turn-on voltage from about 3V to 0V while reducing the applied gate bias from 2V to -5V. This behavior indicates that the gate bias is able to modify the built-in voltage via electrostatic modulation of the doping of the perovskite layer. Specifically, the gate bias in the perovskite FETs can fully deplete the conduction channel by reducing and almost suppressing the charge doping at the barriers between the contacts and perovskite. In order to understand the results described in Fig. 1 we performed extensive modeling using first principles calculations and device modeling, which are described in Fig. 2 and Fig. 3 respectively.

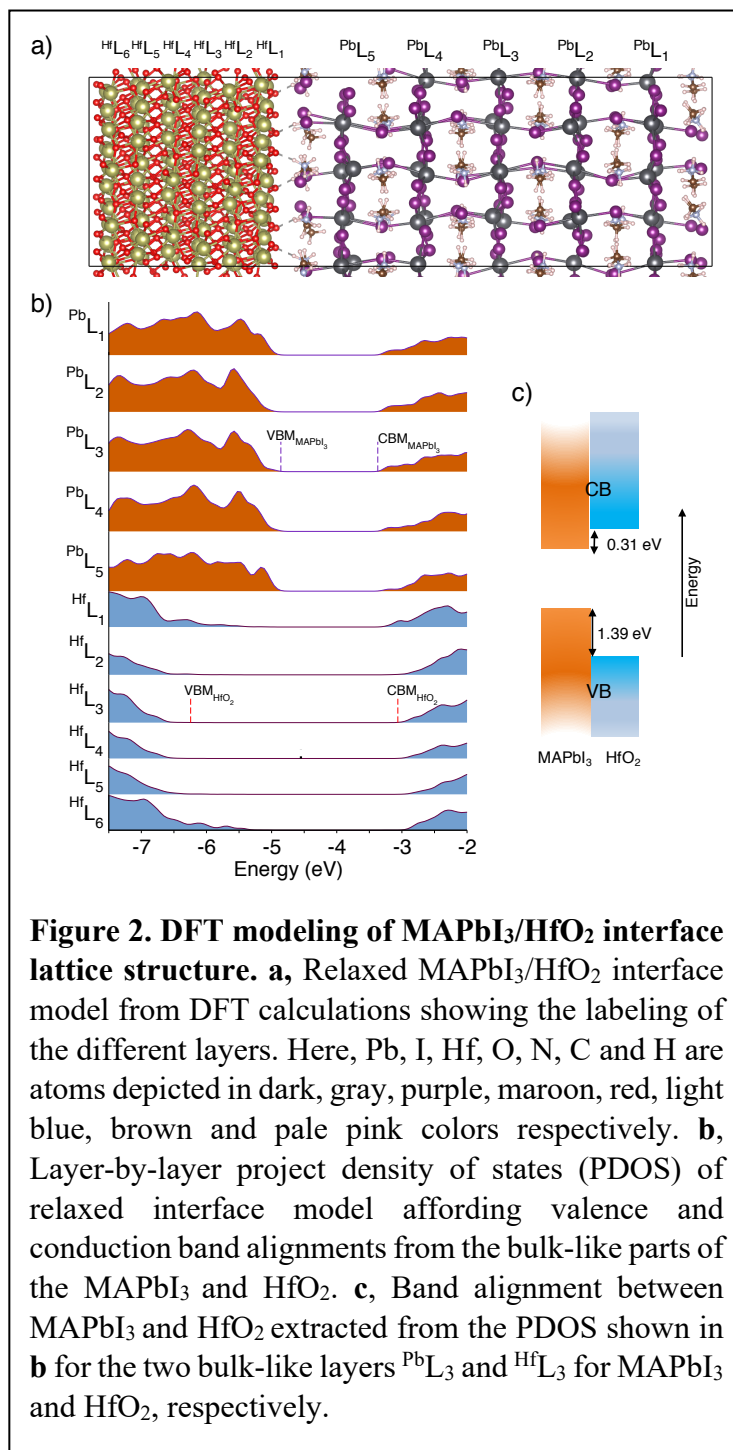
DFT calculations illustrating MAPbI₃/HfO₂ interface

A high-performance gate oxide in a FET device presents a very low-leakage current (*vide supra*), which requires high energy barriers for both holes and electrons across the gate/channel interface. These barriers are generally referred to as the valence band offset (VBO) and the conduction band offset (CBO) for holes and electron, respectively. Hence, to compute these band offsets and thus gain a more fundamental understanding on the performance of the high-k dielectric as the gate oxide, we built a MAPbI₃/HfO₂ interface model and studied its

properties using first-principles based modeling. The detailed procedure of the model construction along with the adopted computational approach are described in the supplementary material (Supplementary note 3). Fig. 2a shows the relaxed structure of the interface system with I atoms pointing to those of Hf at the interface region. Regarding the electronic structure of the system, the band edge states are formed by Pb-I states of MAPbI₃ while those of HfO₂ are either lower in energy at the valence band or higher at the conduction band (Supplementary Figure 6)). From layer by layer resolved projected density of states (PDOS) shown in Fig. 2b, we calculated the band offsets between MAPbI₃ and HfO₂. Here, VBO (CBO) is defined as the difference between VBM_{HfO2} (CBM_{HfO2}) and VBM_{MAPbI3} (CBM_{MAPbI3}) from their bulk-like layers³⁹, which are emulated in Fig. 2a by the two bulk-like layers ^{Pb}L₃ and ^{Hf}L₃ for MAPbI₃ and HfO₂, respectively. We calculated a VBO of 1.39 eV and a CBO 0.31 as summarized in the band diagram of Fig. 2c. Interestingly, the latter corresponds to the ideal band alignment configuration for a gate/channel interface in a FET device and this is consistent with the improved FET characteristics measured with MAPbI₃/HfO₂ interface. The calculated CBO presents a lower barrier as compared to VBO, which may hint to a possible electron tunneling across MAPbI₃/HfO₂. We stress, however, that our DFT calculations underestimate the calculated band gaps. The computations of proper many-body band gap corrections for both bulk materials and for the MAPbI₃/HfO₂ superlattice (over 900 atoms) is computationally unaffordable. Hence, our calculated band offsets only yield a qualitative prediction, which

highlight the suitability and performance of using HfO₂ as a gate dielectric in MAPbI₃ based FET devices.

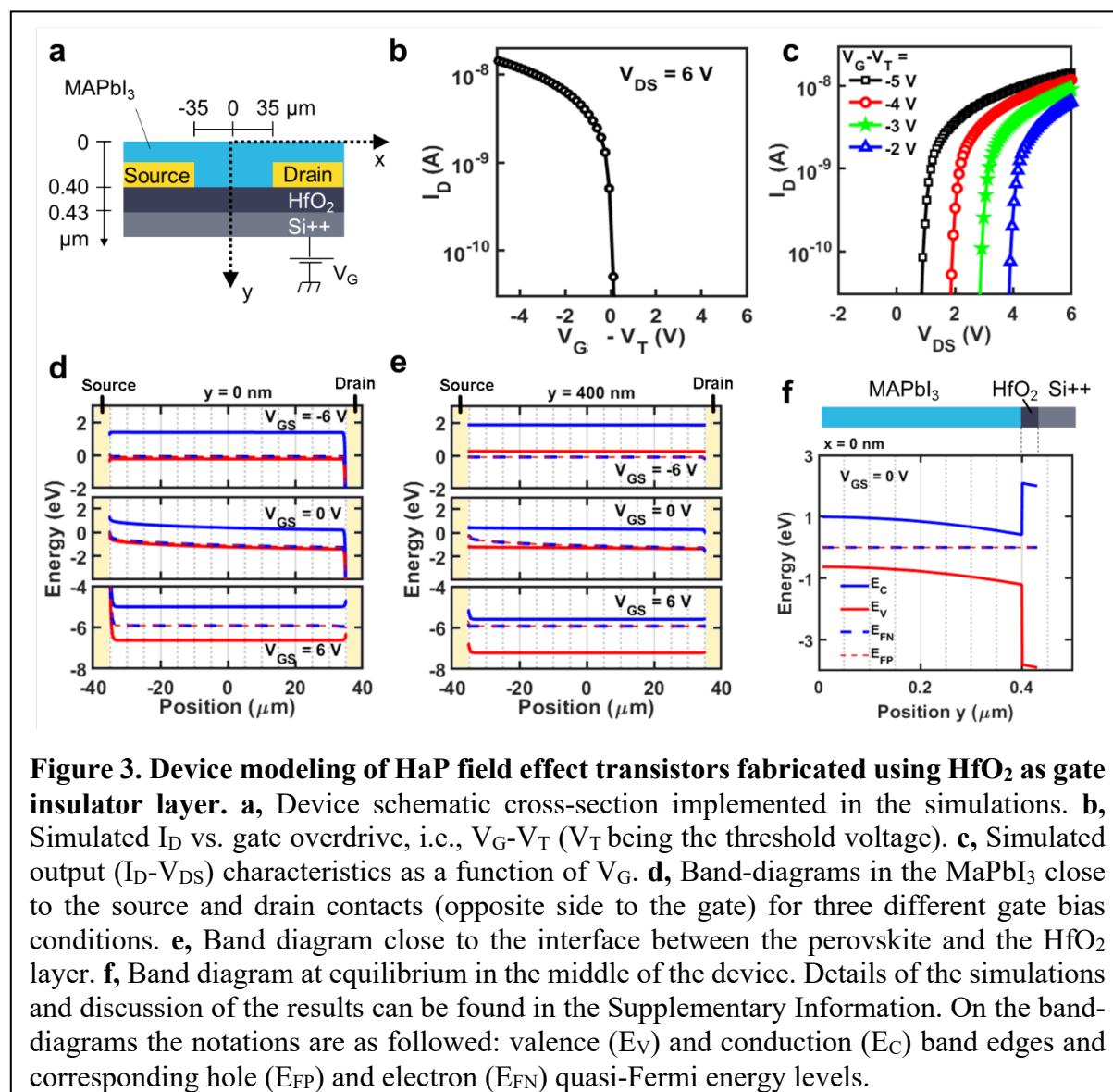
FET device modelling. In order to validate the observed p-type FET behavior with Au as the source-drain electrode and further understand the underlying mechanisms of the perovskite FETs, we simulated the transfer characteristics (I_D - V_G) and analyzed the band diagrams of perovskite-based FETs using HfO₂ as gate dielectric (Fig. 3). Briefly, the numerical simulations involved the self-consistent finite element modeling of electron and hole transport in the two-dimensional device geometry, with appropriate potential barriers for the gate oxide



as well as source drain contacts (see details of the numerical simulations in Supplementary Note 2 and Supplementary Table 1 to 4). A single set of parameters allowed to predictably reproduce the I-V characteristics for a variety of device geometry (film thickness, source/drain separation, etc.), operating conditions (e.g. gate and drain voltages), different types of gate dielectrics

(HfO_2 , Si_3N_4 , and so on). The analysis suggests that the key features of these transistors can be understood at the same level of sophistication as of Silicon MOSFETs.

The device structure implemented in the simulator is schematically represented in Fig. 3a where the model device dimensions are also indicated (see also Supplementary Table 2). Fig. 3b shows the I_D - V_G transfer characteristic for the device with a constant drain bias V_{DS} set to 6 V. The simulations predict a dominant hole current in the channel with device performance comparable to the experimental ones illustrated in Fig. 1b. The I_D - V_{DS} output characteristics for the device with four different gate bias V_G is illustrated in Fig. 3c. The output characteristics



are in agreement with the previous transfer characteristics (Fig. 1e), predicting no considerable change in the device behavior because the gate bias are all well below threshold.

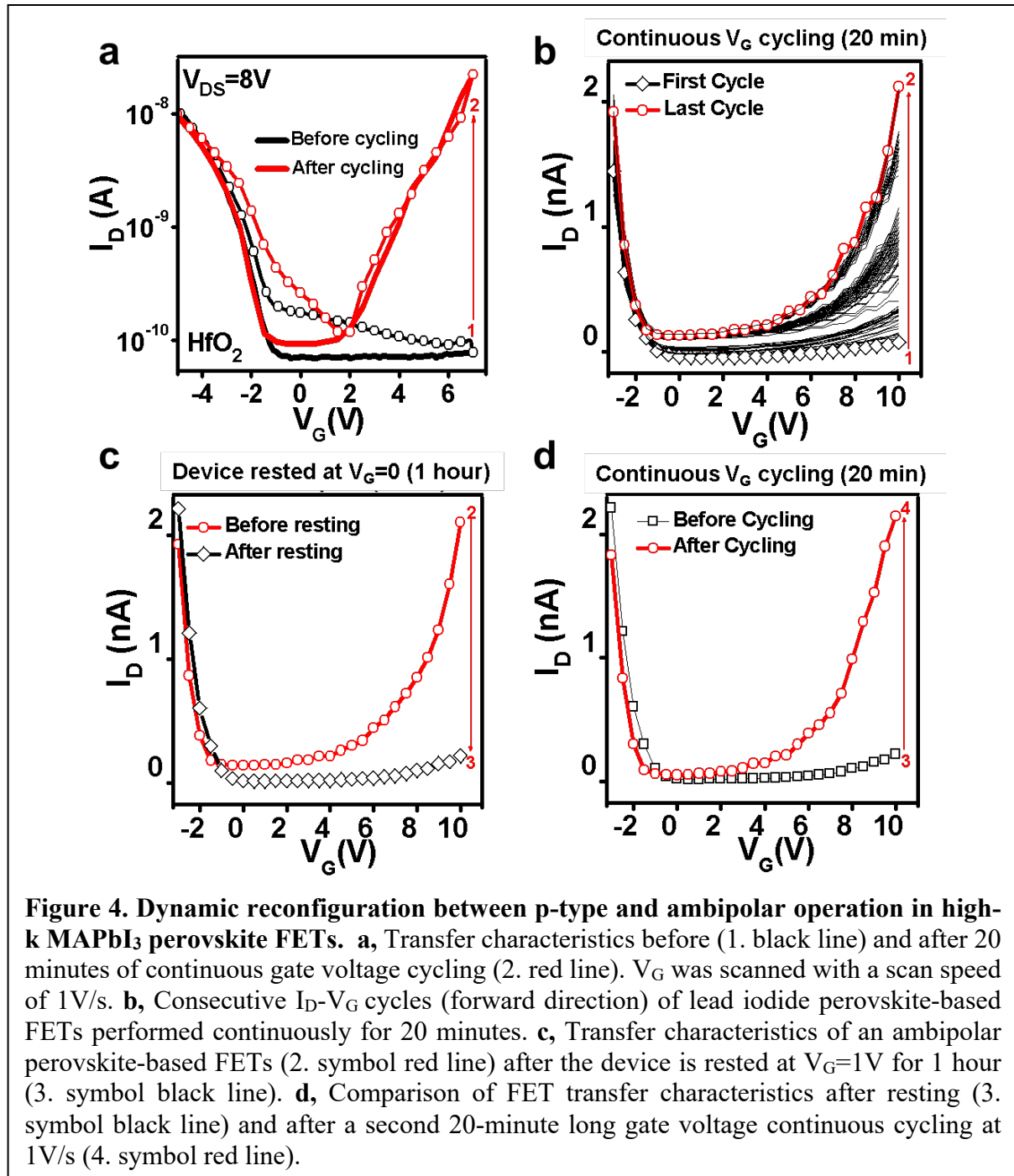
To better understand the previous results, we analyzed the spatial distributions of the valence and conduction band edges as well as of the corresponding hole and electron quasi-Fermi energy levels (Fig. 3d-f). Figure 3d and 3e depict for three gate voltages the band diagrams along the source-drain direction at, respectively, the top and the bottom of the FET channel. We observe that the hole quasi-Fermi level is below or very close to the valence band edge at V_G set to -6 V and 0 V. Conversely, when V_G is set to 6 V, the hole quasi-Fermi level is well above the valence band thereby impeding the flow of holes in the channel. Although in this latter case the electron quasi-Fermi level is close to the conduction band edge, there is a relative high Schottky barrier (about 0.6 eV) at the source contact which precludes the flow of electrons in the channel even at high positive gate bias. Fig. 3f sketches the corresponding band diagram normal to the source-drain direction in the middle of the channel (vertical dashed line in inset schematics of Fig. 3f), crossing both the perovskite and oxide dielectric layers. We observe a decrease of the energy of the valence and conduction band edges by about 0.6 eV across the perovskite layer starting from the free surface. At the interface between the perovskite and oxide layers we observe large barriers for both electrons and holes that prevents leakage, assuming an idealized situation with no ionic vacancies in the perovskite material at this interface (see discussion below). Given the relatively thin perovskite layer (400 nm), the gate can fully deplete the semiconductor (as shown in Fig. 3f, for $V_{GS} = V_{DS} = 0$ V), as confirmed by the low free hole density ($\sim 10^7$ cm⁻³) compared to the doping (10^{16} cm⁻³).

Our device simulations demonstrate that a high- κ dielectric oxide layer such as HfO₂ is required to obtain perovskite-based FETs with a strong gate dependence for p-type carriers at room temperature, confirming the experimental results. We hypothesize that the key to obtain such operational FETs using polycrystalline perovskite thin-films is to reduce the screening of

the gate electric-field by charged ionic vacancies located supposedly at the interface between the perovskite and oxide dielectric which would otherwise hinder the complete inversion of the channel.

Dynamically reconfigurable perovskite FETs (experiment). We experimentally tested the stability and reliability of the gate field effect in the perovskite FETs (HfO₂ as oxide insulator) described in Fig. 1 by measuring the evolution of the I_D-V_G characteristics over several consecutive cycling of the gate bias (Fig. 4). We observed that cycling the gate voltage several times from negative to positive and back to negative at a scan speed of 1V/s resulted in a dramatic enhancement in the gate modulation for the n-type carriers. This operation resulted after 20 minutes in a transient I_D-V_G characteristic typical of ambipolar FETs with a negligible hysteresis and a comparable gate modulation for both the n- and p-type carriers (Fig. 4a). As illustrated in Fig. 4b, this transient effect provides control via the number of gate bias cycle over the modulation of the n-type carriers, i.e. the ON current and ON/OFF ratio. Interestingly, by resting the FET devices at zero gate bias for about 1 hour the original (before gate bias cycling) p-type behavior is recovered (Fig. 4c). After that, performing the gate bias cycling operation reproduced the progressive increase of the n-type gate modulation to reach after several minutes the same ambipolar behavior as the first cycling operation (Fig. 4d). This unique and reversible reconfigurable behavior of FET operation via gate sweeping has not been reported in perovskite based FETs and could potentially be used for short-term, reconfigurable logic circuits, where the signals are dynamically reprogrammed^{36–38}.

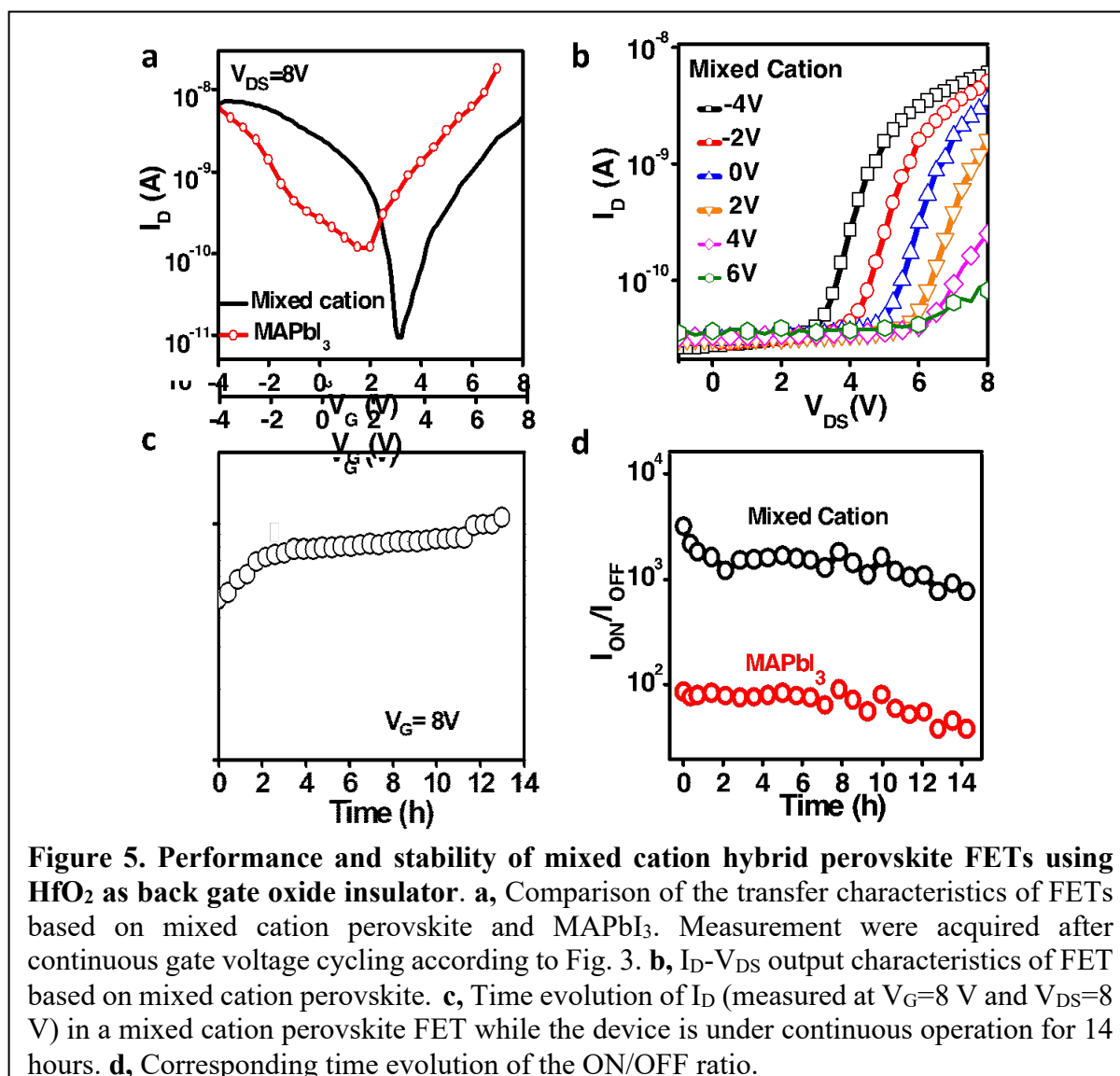
The remarkable reproducibility of this transient behavior suggests that it takes its origin in a dynamical effect in hybrid perovskites which can be activated by carrier doping in the dark. We hypothesize that the transformation from a p-type FET to an ambipolar FET after continuous gate voltage cycling results from local redistribution of the ions within the channels with gate bias cycling, which leads to the creation of stacks of n-type and p-type doped regions



in the channel of the perovskite FETs. This is analogous to work by Dodabalapur et al.⁴³ which demonstrated a polarity tunable ambipolar FET by fabricating a channel with stacked p and n doped layers (achieved by using polymer and C₆₀). Another possibility involves changes in the energy diagram of the perovskite layer that modifies the contribution of n-type carriers during gate bias modulation. In the simulations, we have qualitatively reproduced the ambipolar behavior by considering possible electron tunneling from the source/drain contacts (see

Supplementary Fig. 6). While the exact mechanism for the observed ambipolarity is not clear, our simulations suggest that the redistribution of the electric field due to ion movement could enhance the field close to the contact and enhance the tunneling current from the source/drain contacts.

Finally based on the understanding gained through our measurements (Fig. 1-4), we proceed to demonstrate a high-performance FET operating at RT by replacing the MAPbI₃ with the recently discovered mixed cation perovskites, which exhibits higher intrinsic electronic



conductivity.^{11,14,44} We used a composition of FA_{0.5} MA_{0.25} Cs_{0.25} PbI₃ (details for the materials preparation and characteristics are given in Supplementary Note 1 and Supplementary Figure 5) as the active channel in FETs using HfO₂ as the gate insulator with the same device geometry

as illustrated in Fig. 1a. The corresponding I_D - V_{DS} and I_D - V_G characteristics are shown in Fig. 5a and 5b, where the measurement were performed after gate bias cycling under the same conditions as in Fig. 4. In comparison with the MAPbI₃, the ON/OFF ratio is nearly one order of magnitude higher ($\sim 10^3$) in the mixed cation due to a significant reduction of the OFF current to about 10 pA. We also note an improvement in the mobility and subthreshold swing in the mixed cation-based FETs as compared to their MAPbI₃ counterparts. We note that the overall mobility is still on the lower end of what has been reported and we believe that this is probably related to the presence of traps at the interface of HfO₂/HaP. The I_D - V_{DS} characteristics at different applied gate bias yield a typical diode behavior but with gate field dependent threshold voltage, analogous to MAPbI₃ based devices. We attribute the improvement of performances to the better film quality of the mixed cation perovskites as compared to MAPbI₃ (Supplementary Information Figure 5) and a reduction of the diode barriers.

We also evaluated the reliability of both MAPbI₃ and FA_{0.5}MA_{0.25}CS_{0.25}PbI₃ based perovskite FETs by scanning I_D - V_G characteristics continuously over 14 hours. Fig. 5c and 5d show the time evolution of, respectively, the drain current at a fixed gate voltage ($V_G = 8V$) and the ON/OFF current ratio, for both the MAPbI₃ and the mixed cation perovskite FETs. The results show that both types of FETs exhibit stable current output over 14 hours with little degradation in the ON current and ON/OFF ration (factor of 4). These results are the first to address the long-standing problem of reliability and stability of hybrid perovskite-based FETs operating at room temperature.

In summary, we report the first demonstration of a perovskite thin-film FET with strong gate dependence at room temperature and negligible hysteresis and good durability during the device operation. Moreover, we show that persistent electrical cycling of the gate voltage leads to a FET, which can be dynamically reconfigured between p-type and ambipolar operation states. This behavior opens new opportunities for hybrid perovskite FETs towards applications

in reprogrammable electronics including for example short and mid-term memory devices. These devices exhibit a high (10^4) ON/OFF ratios and a charge carrier mobility of $10^{-3}\text{cm}^2/\text{V}\cdot\text{s}$. Further improvements in the device figures of merit are expected to arise from improvements in the contacts and mitigating charge carrier scattering at the gate oxide/perovskite interface. These results pave the path for using perovskite-based FETs as a platform for the understanding and realization of new and emergent device concepts and for the elucidation of several predicted mechanisms that couple charge, lattice, electric field and light.

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Authors contributions: A.D.M, conceived the idea, designed experiments, analyzed the data and co-wrote the manuscript along with J.-C.B and M.A.A. N. D.C, K. F and F. L, performed FET device fabrication. H.B performed photocurrent and electroluminescence under the supervision of J.-C.B. N. Z performed device modeling simulations and analyzed simulation data with M.A.A, who conceived the device modeling and supervised the device modeling. R. R and L.L.B analyzed the data and supervised the project along with A.D.M. J.E and M.G.K discussed the results and provided inputs on the choice of material compositions along with H.T, W.N, and S.T. B.W.A helped in optimizing experiments and helped with analysis of the data. All authors have read the manuscript.

Authors N. D.C and N. Z contributed equally to the work and will serve as joint first co-authors.

Additional Information

Data availability: The data that support the findings of this study are available from the corresponding authors upon reasonable request.

Competing interests: The authors declare no competing interests.

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Supplementary Materials

Halide perovskite high-k field-effect transistors with dynamically reconfigurable ambipolarity

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Supplementary Note 1

Materials

Methylammonium iodide (MAI), lead iodide (PbI₂), formamidinium iodide (FAI), cesium iodide (CsI), dimethylsulfoxide (DMSO), dimethylformamide (DMF), Methylammonium chloride (MAcI) were all purchased from Sigma Aldrich.

Perovskite precursor

Lead iodide perovskite solution was mix of PbI₂ and MAI (1:1) in anhydrous DMSO and DMF (1:1) solvent. The prepared solution was stirred for at least 48 hours at 70 °C before using.

Mixed Cation perovskite solution was mix of PbI₂, FAI, MAcI, and CsI (1: 0.5:0.25:0.25) in anhydrous DMSO and DMF solvent (1:1). The prepared solution was stirred for at least 24 hours at 70 °C before using.

Optical microscope measurement

The optical microscope images of perovskite films were collected using an optical bright-field microscope (Model: Olympus BX51M) with 5X and 10X focal lengths under Olympus U-DICR prism at room temperature.

FET fabrication

Field effect transistors used in this study were performed following bottom-gate bottom-contact structure as illustrated in Fig.1a of the main text. Heavily n-doped Si wafer with 100nm thick thermally silicon dioxide layer (SiO₂, $\epsilon_r \sim 3.9$) / 100 nm thick silicon nitride (Si₃N₄, $\epsilon_r \sim 7.5$) deposited by PECVD (plasma-enhanced chemical vapor deposition) and 30nm Hafnium oxide (HfO₂, $\epsilon_r \sim 23.4$) deposited by ALD (atomic layer deposition) were used as substrates in this work.

The substrates were cleaned by three times of sonication in acetone and isopropyl alcohol for 10 min respectively and subsequently dried under nitrogen air flow followed by baking on hot-plate in air for 20 min. Subsequently, electrodes of 20 nm titanium and 180 nm-thick gold (100um x 100um) were deposited by electron beam deposition using a shadow mask to define a channel area of W=100um and L=70um. Subsequently, the patterned-substrates were exposed to oxygen-plasma cleaning treatment for 6 minutes to improve the wetting of the surface and obtain uniform perovskite layers; otherwise perovskite solution does not stick on the silicon substrates after its deposition. Then, the perovskite thin-films were deposited by using the previously develop hot –casting method to grow high quality perovskite films (See Supplementary Fig. 1-2).

For this approach we used a hot (70°C) perovskite precursor ink (MAI: PbI₂ (1:1),) casted onto a preheated and spinning (180 °C) substrates (rotation time 30 seconds). After perovskite spin coating (thickness ~ 400nm), the substrates were placed on the hot plate at 100°C for 10 minutes to fully convert the perovskite precursor into the CH₃NH₃PbI₃ perovskite films.

FETs characterization

After perovskite deposition, the devices were immediately loaded into a ST500-1-4CXKEL-TR vacuum probe station to proceed with the electrical measurements. These measurements were carried out at high vacuum (10⁻⁷ torr level) by using a turbo molecular pump before the characterization. The characteristics of perovskites field effect transistors were analyzed by using YOKOGAWA 7562 Digital Multimeters along with a current amplifier (Yokogawa 7561 multimeter).

Supplementary Note 2

Charged carrier transport was modeled adopting the drift-diffusion formalism (see Supplementary Tab. 1 for the equations set). With this approach Poisson equation and continuity equations are solved self-consistently to obtain the electrostatic potential and the carriers' concentration. Numerical simulations are carried out with a commercial software¹.

Poisson Equation	$\nabla \cdot (\varepsilon \nabla \psi) = -q(p - n + N_D - N_A)$
Continuity Equation.	$\mp \nabla J_{n,p} = q(G_{n,p} - R_{n,p})$
Drift-Diffusion Equations	$J_n = \mu_n n (-\nabla \psi) + D_n \nabla n$ $J_p = \mu_p p (-\nabla \psi) - D_p \nabla p$
Recombination Equation	$R_{n,p} = \frac{np - n_i^2}{\tau_n(p + p_1) + \tau_p(n + n_1)}$

Supplementary Table 1. Equations for Carrier Transport used for the device simulations.

The device structure implemented in the simulator is schematically represented in Fig. 2 of the main text, with indication of the device dimensions. The geometrical parameters and device dimensions adopted in the simulations are collected in Supplementary Tab. 2.

Symbol	Description	Parameter value
L_G	Gate Length	70 μm
W_G	Gate Width	100 μm
t_{ox}	Gate Oxide Thickness	30 nm (EOT \sim 5 nm)
t_{chan}	Semiconductor Channel Thickness	400 nm

Supplementary Table 2. Geometrical Dimensions adopted in the device simulations.

Supplementary Tab. 3 collects the MaPbI_3 electrical parameters; Supplementary Tab. 4 includes other relevant parameters used in the simulations. Schottky barriers are considered at the boundaries of the MAPbI_3 layer with the gold source and drain contacts. SHR recombination (with lifetime found from literature²) in the perovskite semiconductor layer is also taken into account. We consider HfO_2 as the gate oxide layer ($\epsilon_r \sim 23.5$).

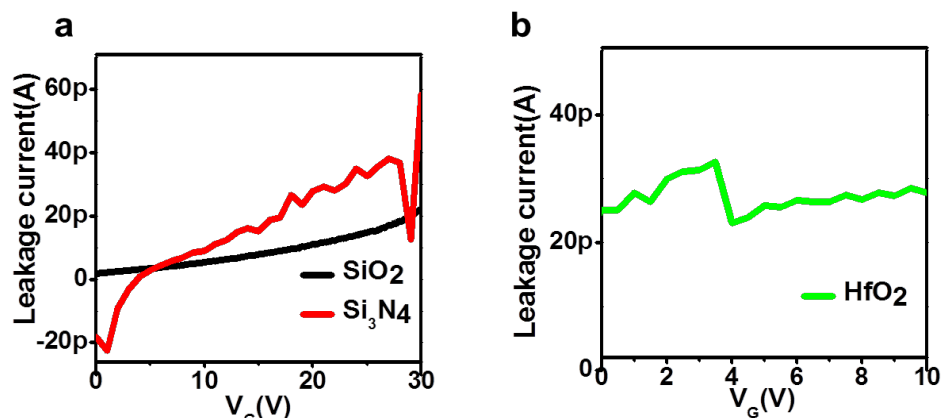
Symbol	Description	Parameter value
E_G	Band Gap	1.62 eV
χ	Electron Affinity	3.73 eV
ϵ_r	Relative Dielectric Constant	25
N_C	Effective Density of States in the Conduction Band	$6.98 \times 10^{18} \text{ cm}^{-3}$
N_C	Effective Density of States in the Valence Band	$2.49 \times 10^{18} \text{ cm}^{-3}$
n_i	Intrinsic Carrier Concentration	$1.03 \times 10^5 \text{ cm}^{-3}$
N_A	Doping Concentration (p-type)	$1.0 \times 10^{16} \text{ cm}^{-3}$
$\mu_{n,p}$	Carriers' Mobility	$0.4 \text{ cm}^2/\text{V.s}$
$\tau_{n,p}$	Carriers' Lifetime	10 ns

Supplementary Table 3. MaPbI_3 Parameters (Perovskite)^{2,3}.

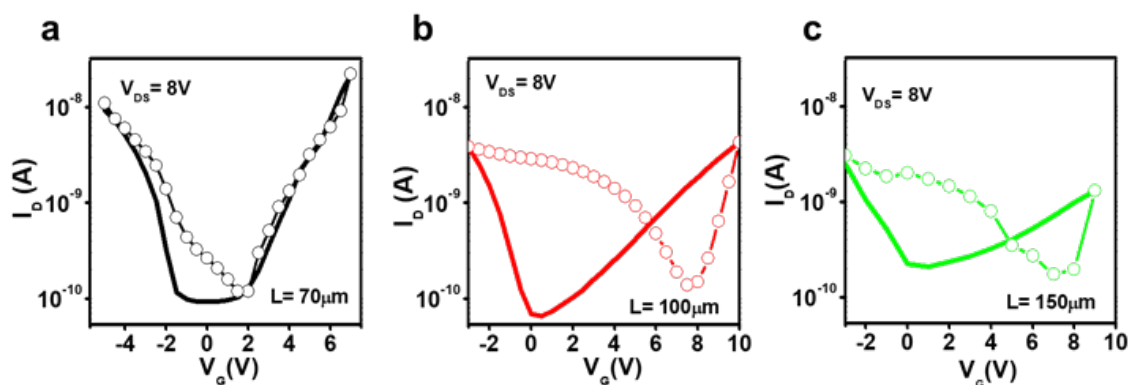
Symbol	Description	Parameter value
ϵ_r	Relative Dielectric Constant (HfO_2)	23.5
Φ_G	Gate Contact Work-Function	4.05 eV (Silicon)
$\Phi_{S,D}$	Source, Drain Contacts Work-Function	5 eV (Gold)

Supplementary Table 4. Other Relevant Simulation Parameters.

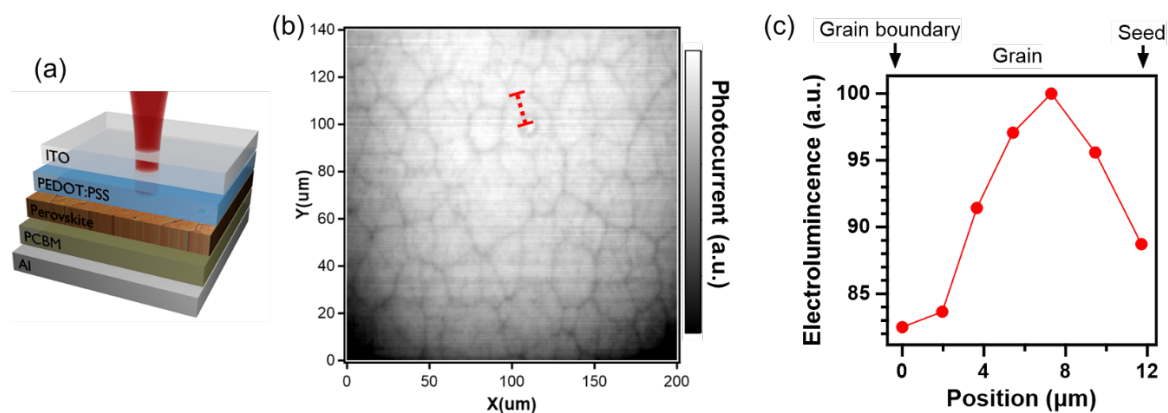
Supplementary Figures



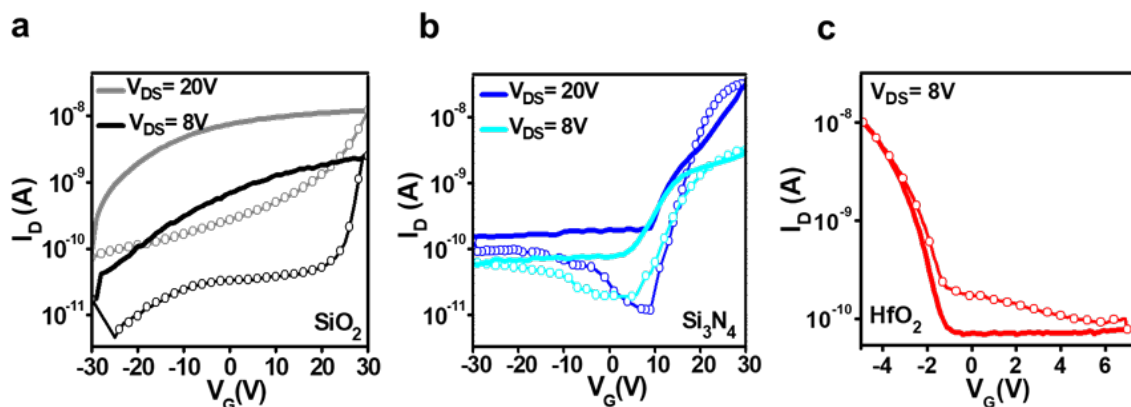
Supplementary Figure 1. Leakage current (I_g - V_g) in perovskite-based field effect transistor using SiO_2 , Si_3N_4 and HfO_2 as insulators.



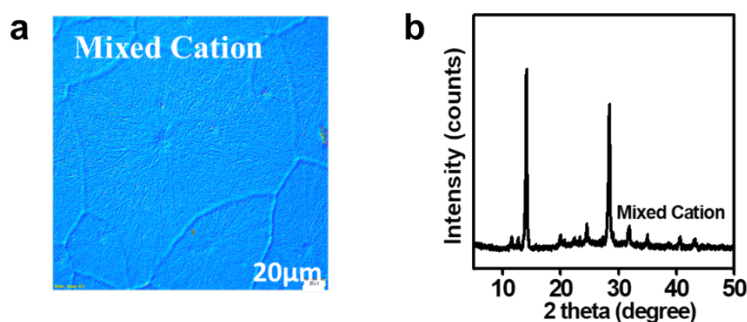
Supplementary Figure 2. Transfer characteristics of MAPbI₃ perovskite FETs with different channel length. The devices were operated in the ambipolar regime after continuous gate cycling during 1 hour, which allows us to probe channel length dependence of both electron and hole transport. Solid and dotted lines in the I_D - V_G curves illustrate the forward and reverse scans for channel length a) $70 \mu\text{m}$, b) $100 \mu\text{m}$, and c) $150 \mu\text{m}$, all with channel width $100 \mu\text{m}$.



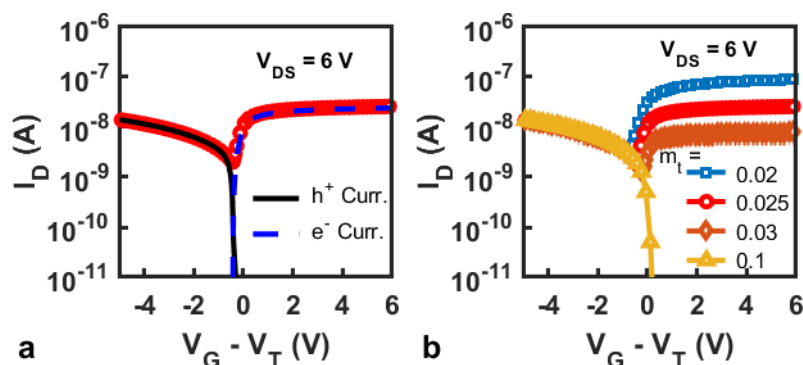
Supplementary Figure 3. Surface photocurrent intensity (b) and electroluminescence intensity (c) of the MAPbI₃ thin films demonstrating the detrimental role of grain boundaries to charge transport. A planar solar-cell architecture (a) was used for these measurements. The electroluminescence intensity profile in (b) correspond to the dashed red line in (a).



Supplementary Figure 4. MAPbI₃ perovskite FETs using different dielectric as insulators. Dielectric constant-dependent transfer characteristics of a perovskite field effect transistor using (a) SiO₂, (b) Si₃N₄ and (c) HfO₂. Voltages are scanned in both the forward (lines) and reverse (symbols) directions.



Supplementary Figure 5. Characteristics of the mixed cation perovskite FA_{0.5}MA_{0.25}Cs_{0.25}PbI₃. **a**, Optical micrographs illustrating the microstructure for MAPbI₃ and Mixed Cation perovskite thin films deposited on HfO₂ using hot-casting method. **b**, X-ray diffraction pattern of the thin films on glass substrates deposited using the hot casting technique.



Supplementary Figure 6. Simulations of ambipolar I_D - V_G characteristics. **a**, Electron current flows for $V_G - V_T > 0$ V when the tunneling at the source/drain contacts is active. **b**, Varying the electron tunneling mass (i.e., the tunneling probability) varies the current flow in the device.

PEROVSKITE PRECURSOR INK		
Solvent	DMF	× No operational devices
	DMSO	<i>Low coverage perovskite thin films on the dielectric</i>
	Mixture DMSO:DMF at a molar ratio of 1:1	✓ Operational devices <i>Good coverage and high-quality perovskite films on the dielectric layer</i>
Precursors	MAI:PbCl ₂ at a molar ratio of 1:1	× No operational devices
	PbI ₂ :FAI:MAI:CsI at a molar ratio of 1:0.7:0.25:0.05	<i>Bad quality and bad adhesion of perovskite films on the dielectric layer</i>
	MAI:PbI ₂ at a molar ratio of 1:1	✓ Operational devices
	PbI ₂ :FAI:MAI:CsI at a molar ratio of 1:0.5:0.25:0.25	<i>High quality perovskite films on the insulator layer</i>

Supplementary Table 5. Iterations performed in this work related to the perovskite precursor ink to obtain reproducible perovskite-based field effect transistors operational at room temperature.

PEROVSKITE DEPOSITION		
Perovskite thickness (d)	< 400nm	× No operational devices Need to dilute the solution to obtain thinner layer which leads to a decrease on the film quality.
	400 nm	✓ Operational devices <i>Good coverage and high-quality perovskite films on the dielectric layer</i>
Pre-treatment	No treatment	× No operational devices No adherence of perovskite on the dielectric
	O ₂ plasma	✓ Operational devices <i>Good perovskite adherence on the dielectric</i>

Supplementary Table 6. Iterations performed in this work related to the perovskite deposition to obtain reproducible perovskite-based FETs operational at room temperature.

Leakage problem	Without any protection	× No operational devices
	Protection on the borders of the substrate by using an organic insulator	Leakage too high due to current paths on the edge of the silicon wafer.
	Protection on the edge of the substrates by using kapton tape	✓ Operational devices
Insulator	SiO ₂ (100-300nm) obtained by thermal growth/ PECVD	Huge hysteresis Weak gate modulation
	Si ₃ N ₄ (100-300nm) deposited by PECVD	Small hysteresis Weak gate modulation
	HfO ₂	✓ Operational devices

Supplementary Table 7. Iterations performed in this work related to the gate dielectric to obtain reproducible perovskite-based FETs operational at room temperature.

Channel dimensions	Square mask (100um*100um)	L < 70 μm W = 100 μm	× No operational devices No adherence of perovskite on small channel lengths.
		150 μm > L > 70 μm W = 100 μm	✓ Operational devices

Supplementary Table 8. Iterations performed in this work related to the device geometry to obtain reproducible perovskite-based FETs operational at room temperature.

Supplementary Note 3

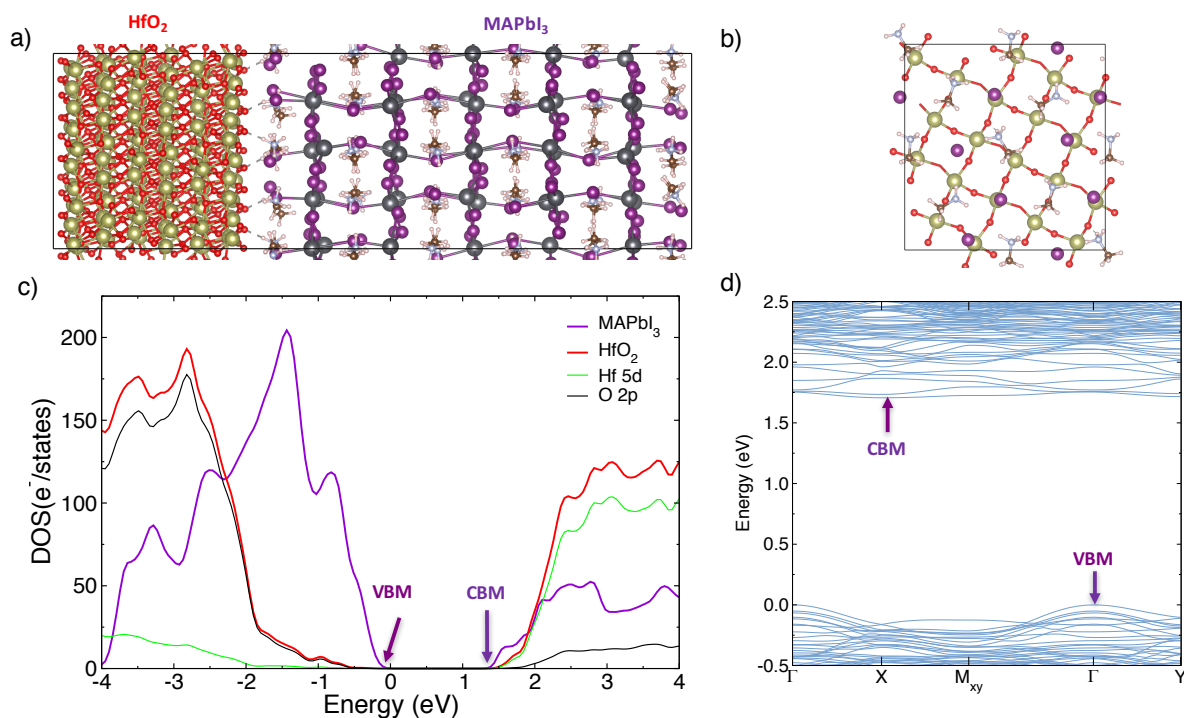
First principles study of the MAPbI₃/HfO₂ interface

The interface construction is based on the orthorhombic crystal structure of MAPbI₃ where the MA (methyl ammonium) molecules have well-defined positions within the inorganic Pnma lattice. Using the (001) surface of monoclinic HfO₂ rotated to about 90°, the MAPbI₃ (010) surface affords appropriate lattice matching for a MAPbI₃/HfO₂ interface (Supplementary Table 9).

	a (Å)		b (Å)		c (Å)		β	
	exp.	calc.	exp.	calc.	exp.	calc.	exp.	calc.
HfO ₂	5.12 ⁵	5.09	5.18 ⁵	5.22	5.29 ⁵	5.21	99.22 ⁵	99.05
MAPbI ₃	8.84 ⁶	8.74	12.58 ⁶	12.58	8.56 ⁶	8.40		
		a _{interf} (Å)		b _{interf} (Å)				
		16.13		16.46				
Lateral mismatch wrt. relaxed HfO ₂ (%)		4.1%		6.3%				

Supplementary Table 9. Lattice constants of bulk HfO₂, MAPbI₃ and the heterostructure MAPbI₃/HfO₂ interface model. For the heterostructure, the lattice constants of MAPbI₃ are rotated such that b becomes c that is: $abc \rightarrow cab$. We note that the interface being constructed along c, the lattice mismatch along c for the heterostructure is irrelevant.

Since MAPbI₃ is deposited on top HfO₂, we used the latter as the substrate. Therefore, we lattice matched the parameters of MAI-terminated MAPbI₃ to those of HfO₂. This is reasonable as HfO₂ is much stiffer than MAPbI₃ from the comparison of their Young moduli. Therefore, we obtained the following lattice mismatch: 4.1% along **a** and 6.3% along **b**. These values are relatively acceptable given the differences in their crystallographic structures. The constructed interface model contained 912 atoms and was allowed to relax along the stacking **c** direction while the lateral in-plane parameters (**a** and **b**) were kept constant as obtained from bulk HfO₂ full relaxation (Supplementary Figure 6a). The interface relaxed such that I atoms point to those of Hf at the interface region, which is chemically consistent since Iodine is an anion that points to Hf which is a cation (Supplementary Figure 6b). The projected density of states of Supplementary Figure 6c shows the contribution of MAPbI₃ and HfO₂. From this, one can see that the band gap edge states are MAPbI₃ states with HfO₂ presenting barriers for both holes and electrons coming from MAPbI₃. Finally, the band structure of the interface is shown in Supplementary Figure 6d. The band gap appears to be indirect due to band folding from Γ to X at the conduction band as a result of MAPbI₃ cell doubling during the course of the interface construction.



Supplementary Figure 6. Structural and electronic properties of MAPbI₃/HfO₂ interface model. **a**, Relaxed MAPbI₃/HfO₂ interface model from DFT calculations showing the labeling of the different layers. Here Pb, I, Hf, O, N, C and H atoms are depicted in dark, gray, purple, maroon, red, light blue, brown and pale pink colors, respectively. **b**, Interface configuration after relaxation with I atoms mostly pointing to Hf. **c**, Projected density of states of the interface system showing the contributions of MAPbI₃, HfO₂, Hf 5d and O 2p states. **d**, Band structure of the interface system.

First principles simulations method

The calculations were performed within the Density Functional Theory (DFT)⁶⁻⁷ as implemented in SIESTA package⁸ with a basis set of finite-range of numerical atomic orbitals. We used the van der Waals density functional with C09 exchange⁹ to describe the exchange-correlation term. This functional has proven to provide superior description of experimental lattice constants similar to those obtained with optimized GGA based PBEsol functional in solids¹⁰. Norm-conserving Troullier-Martins pseudopotentials were used for each atomic species to account for the core electrons.¹¹ 1s¹, 2s²2p², 2s²2p³, 5s²5p⁵, 5d¹⁰6s²6p², 2s²2p⁴ and 6s²5d² were used as valence electrons for H, C, N, I, Pb, O and Hf respectively. Polarized Double-Zeta (DZP) basis set with an energy shift of 200 meV were used for the calculations. For the real space mesh grids, energy cutoffs of 200 and at least 400 Rydberg were respectively used for MAPbI₃ bulk and systems including HfO₂ (bulk HfO₂ and interface with HfO₂).

References

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