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Design of a fully digital controller for a shunt three-phase active filter using VHDL-AMS language

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Area of research: Electronics systems

Abstract – In this paper, authors detail a Top-down design methodology for Power Electronic fully digital controller based on a Field Programmable Gate Array (FPGA). This design flow uses the VHDL-AMS language. The case of a shunt three-phase active filter is studied. An optimised architecture is designed and each step is detailed. Each block of the architecture is modelled in the VHDL at several levels of abstraction, from real data format to specific binary format. To achieve closed loop simulation, analogue and power elements are modelled in the VHDL-AMS. The whole closed loop system is successfully validated at various levels of abstraction of the digital control, using the *ADVanceMS* Computer Aided Design tools. An experimental validation of the proposed architecture, implemented on the target *Xilinx Virtex-II 2V4000bf95* FPGA is discussed.

Keywords: shunt active filter, fully digital controller, VHDL-AMS, architecture optimisation

I. INTRODUCTION

Before designing a Field Programmable Gate Array (FPGA) or ASIC (Application Specific Integrated Circuit) prototype of a fully digital controller for a Power Electronics system, a closed loop simulation and verification of the whole system are necessary in order to check its functionality and thus well the functionality of the future digital integrated circuit.

In the past three decades, hardware description languages (HDLs) have been widely used to model and simulate systems belonging to various engineering fields. For a long time, all these fields have been completely separated, each scientific community with its own design methodology and tools.

With the advent of nanotechnologies, the complexity of systems containing several fields such as MOEMS (Micro Opto ElectroMechanical Systems) becomes increasingly important. The development of a design environment for multidisciplinary systems, allowing a simulation of different physical domains is needed. The scientific engineering community IEEE proposed in 1999 the extension of an existing standard, IEEE 1076.1-1999, so called Very high speed integrated circuits Hardware Description Language – Analogue Mixed Signal (VHDL-AMS) [1], [2]. The VHDL-AMS is the hardware description language whose syntax and semantics [3] allow at the same time rapid and flexible way for modelling of a complex multidisciplinary system [4]. A mixed HDL functional verification and validation of a complex multidisciplinary system at various levels of abstraction are now available [5], recently used in power electronics research area [6].

As far as Power Electronic applications are concerned, similar design approaches for fully digital control could be considered [7, 8, 9, 10]. High-level analysis of a multidisciplinary system, functional validation at any design step, top-down design approach, simulation at various levels of abstraction and final physical design are the necessary tasks that need to be carried out to design well and optimise the digital controller till its final physical implementation.

In this paper, the authors detail a Top-Down methodology based on the VHDL-AMS description language and show improvements using this approach in designing of a fully digital controller. More precisely, this methodology is applied to the design of the digital controller for a shunt three-phase active filter. The Design flow is detailed in Section II. Then, the control strategy of the shunt three-phase active filter, using the method of instantaneous active and reactive powers, is described in Section III. In order to validate step-by-step our methodology, this case study is used.

II. VHDL-AMS BASED DESIGN METHODOLOGY

II.1. Design approach

The growing complexity of the multidisciplinary systems such as power electronic applications imposes to the designers a certain number of rules that must be respected at any design step. Today, the designers are mostly confronted with major challenges such as:

- High-level formal executable modelling method from the specifications;
- Error detection in the earliest stages of the design;
- Digital integrated circuits (FPGA or ASIC) functioning at the first programming or use;
- Project management to satisfy increasing time-to-market requirements;
- Design reusability.

To integrate all these constraints, the design methodology will play an increasing role in the success of FPGA-based industrial control systems, more particularly for power electronics applications [11, 12]. For a fully digital control design, Computer Aided Design (CAD) tools make possible to design circuits in a practically automatic way. Starting from a high level description of the function with a digital HDL, we use suited software to achieve necessary tasks (logical synthesis, simulation, optimisation and placement-routing) up to the final digital circuit design. These design techniques saw their effectiveness growing with the maturity of hardware description languages dedicated to digital design, such as Verilog or VHDL. We will reconsider later in this section the very important aspect of a digital or mixed HDL in the proposed methodology..

To model and simulate a complex multidisciplinary system such as power electronics application, the designer can use several modelling approaches depending on the final goal. High-level simulation results could be easily achieved using high-level tools such as Matlab-Simulink, which allows modelling of all parts of the target system. However, this high level modelling solution does not allow designing of a final fully digital design., i.e. this approach can only be used for checking and validating of the functionality of the entire system at the high level of abstraction. More recently, CAD tools such as DSPBuilder or SystemGenerator were associated to Matlab/Simulink tools. They allow effectively designing of a fully digital control. Specifically, the method proposed in [9] simulates the converter power stage using Virtual Test Bed and controls it using the actual converter digital controller, with an FPGA control system interfaced through the PCI bus of the host computer. However,

these tools generate automatically the VHDL code and thus no architecture optimization is possible [9, 10]. In our approach, by using existing methodology [13], we developed an improved VHDL-AMS-based design flow for an optimised digital control design of a power electronics application. In the proposed methodology, the fully digital controller can be validated in closed loop simulation, in a unique mixed design environment, from the high level to the final synthesizable description.

II.2. VHDL-AMS based Top-Down design approach

Power electronic systems are composed of several parts. To model the whole power system, the designer must mainly hold account of the sensors, power and analogue components. To ensure predictability of the final fully digital control, the design approach must allow the simulation of the complete power system. Thus, system can be evaluated quickly and eventual errors can be corrected more easily and cost effectively.

Top-down conception allowed us to design the digital control from specifications to final implementation details. Moreover, the use of the VHDL-AMS throughout the design provides a system validation at any level of abstraction and makes the digital design independent of the target technology. We propose to use a design methodology presented in Figure 1.

In the first stage, the designer either uses existing libraries with the VHDL-AMS models of components or creates its own new behavioural VHDL-AMS models to describe the analogue and power environment and the high-level behaviour of the digital controller. These high level models are firstly validated by mixed simulation using real data format.

Then, the designer draws his attention to the algorithm implementation, i .e. he studies an optimised architecture for the digital controller. This step is mostly dedicated for optimization of calculations in the algorithm and it determines approximately the number of digital operators which will be used for the algorithm implementation. This step is especially critical with regard to the silicon area of the final digital prototype. The studied architecture is validated at high level by mixed simulation using real data format and reusing analogue and power high level models previously described.

Then, before designing the final synthesizable VHDL model of the digital controller, the designer must take care of its digital implementation. To synthesize a digital design, the data format must be a specific binary data format. Consequently, the designer selects the number of bits necessary to compute constants and values appearing in the algorithm flow. The size of the decimal part should not decrease control performances and should be chosen and optimised according to this criterion.

In the phase dedicated to the final synthesizable VHDL model design, the designer modifies the VHDL models that were already written and describes them at Register Transfer Level (RTL). Some structural descriptions can be easily and quickly tested by

reusing VHDL functions or Intellectual Properties (IP) previously validated to reduce silicon area and to improve algorithmic treatment time.

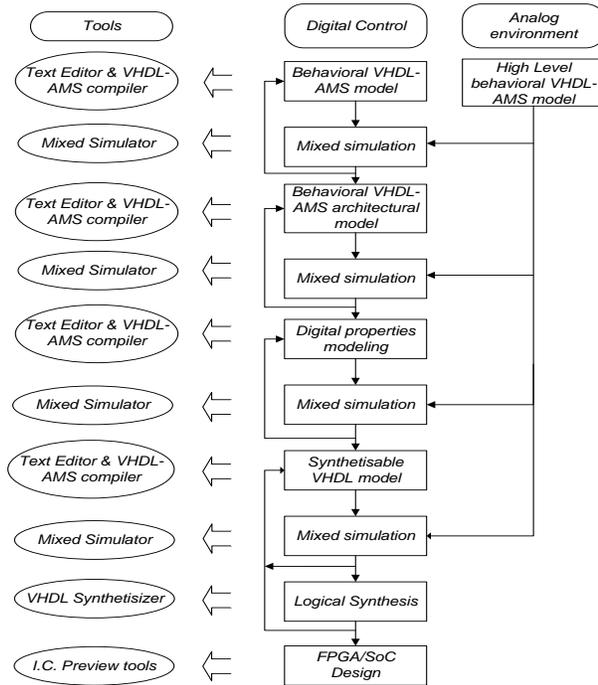


Fig. 1. Design flow.

At each step, the model of the digital control is functionally validated by mixed simulation. The VHDL-AMS-based simulation is a key element in this methodology design flow and is detailed in the next section.

The final stage of this conception flow is the physical design. Synthesis, placement and routing are carried out using a synthesis tool. The final objective of this work could be both to design an ASIC with the same RTL description or to prototype an FPGA and validate it experimentally [14], [15].

II.3. Mixed simulation environment

Design of a digital controller can be improved using mixed simulation. Indeed, analogue models characterizing real time features of the system which are described with ordinary differential and algebraic equations can be simulated in a unique mixed environment in order to study the digital model of the controller in closed-loop. Hence, a mixed simulation environment based on ADVanceMS Computer Aided Design tools and on VHDL-AMS language is used.

To model the digital parts of the system, we used the VHDL language. The high-level behavioural analogue and power models are designed in the VHDL-AMS language. The mixed simulation environment for the shunt three-phase active filter studied in next section, is presented in Figure 2. This environment is composed of several parts: the *Power Block* VHDL-AMS models (power rectifier, inverter and passive components), the *interface block* VHDL-AMS models, the electrical sensors and Analogue-Digital Converters (ADC) VHDL-AMS models and the *control block* VHDL model for the digital control.

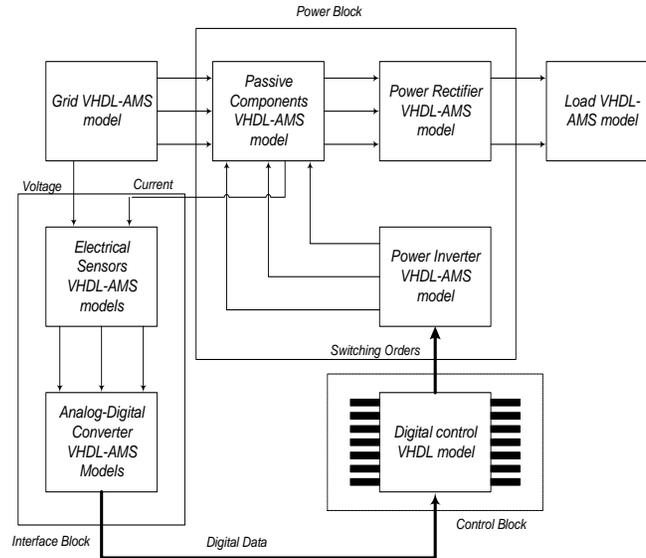


Fig. 2 . Mixed simulation environment.

The mixed simulation environment presented in Figure 2 demonstrates the simple and fast way to simulate and functionally validate any digital controller for power control. Indeed, this method can be used and extended to any other multidisciplinary field of applications.

III. BEHAVIORAL ANALYSIS AND MODELING OF A DIGITAL CONTROLLER FOR A SHUNT THREE PHASE POWER ACTIVE FILTER

III.1. Active filter principle and control

An example of a fully digital controller design is described step by step in next sections. The studied power application, namely a shunt three-phase active power filter is chosen. Current harmonics produced by non-linear loads are prevalent in today's power systems. These harmonics interfere with sensitive electronics equipment and cause unnecessary losses. Active power filters

are proposed as a means of removing current harmonics. The studied three-phase active filter is achieved by a three-leg Insulated Gate Bipolar Transistor inverter (IGBT), an energy storage voltage source (capacitor C_{dc}) and three inductances L_f as shown in Figure 3. The IGBT switching is defined in order to generate in the real time load harmonics currents [16]. The capacitor's value defines filter current dynamic and it is selected according to allowed voltage ripple during operating cycle of active filter. The non-linear load is a three-phase rectifier feeding a (R, L) load.

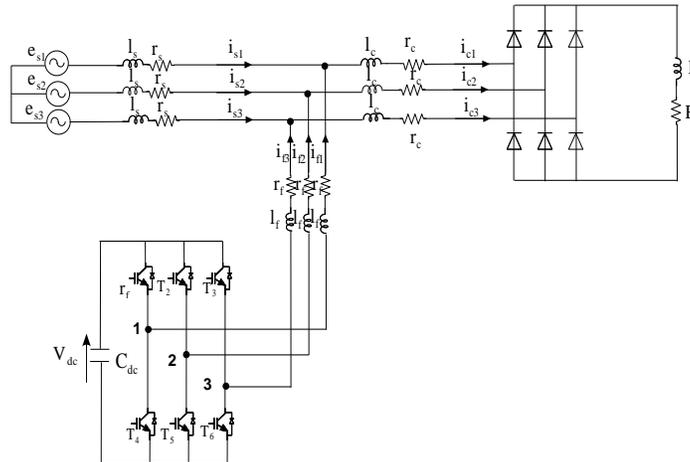


Fig. 3. Active filter principle.

The control principle of the active power filter consists in calculating the filter reference currents from the measured values of the grid voltages and load currents [16], as depicted in Figure 4.

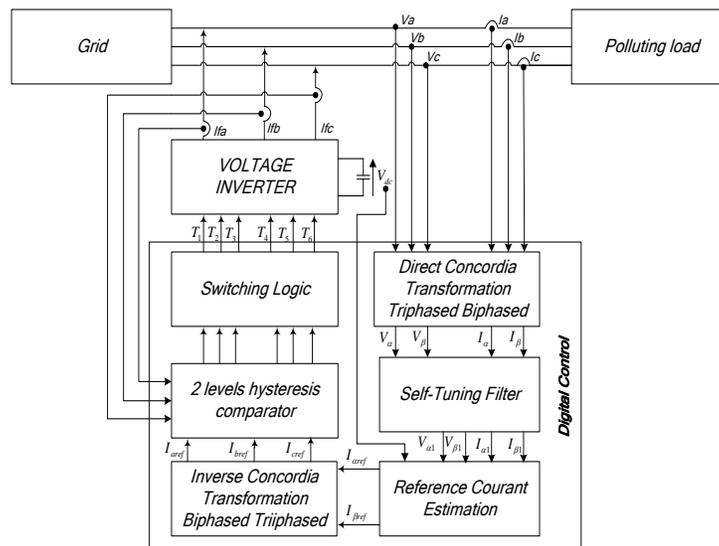


Fig. 4. Control principle.

The voltages and current components (V_α, V_β) and (I_α, I_β) on perpendicular (α, β) axis are computed from measured values (V_a, V_b, V_c) and (I_a, I_b, I_c) by the direct Concordia Transformation:

$$V_\alpha = \sqrt{\frac{2}{3}} \left(V_a - \frac{1}{2} V_b - \frac{1}{2} V_c \right) \quad (1)$$

$$V_\beta = \sqrt{\frac{2}{3}} \left(\frac{\sqrt{3}}{2} V_b - \frac{\sqrt{3}}{2} V_c \right) \quad (2)$$

$$I_\alpha = \sqrt{\frac{2}{3}} \left(I_a - \frac{1}{2} I_b - \frac{1}{2} I_c \right) \quad (3)$$

$$I_\beta = \sqrt{\frac{2}{3}} \left(\frac{\sqrt{3}}{2} I_b - \frac{\sqrt{3}}{2} I_c \right) \quad (4)$$

The self-tuning filter presented in Figure 3, which function is to extract the fundamental from the input signal [10], has the following transfer function:

$$H(s) = K \frac{(s + K) + j\omega_c}{(s + K)^2 + \omega_c^2} \quad (5)$$

where the parameters K and ω_c are respectively the gain and the central frequency of the filter.

After extraction, the voltage and current components are used to compute the active filter reference currents. This function is achieved using instantaneous active and reactive powers method developed by Akagi [17], which is described with the following equations:

$$\begin{bmatrix} I_{\alpha ref} \\ I_{\beta ref} \end{bmatrix} = \frac{1}{v_\alpha^2 + v_\beta^2} \left\{ \begin{bmatrix} V_\alpha & -V_\beta \\ V_\beta & V_\alpha \end{bmatrix} \left\{ \begin{bmatrix} \bar{p} \\ \bar{q} \end{bmatrix} + \begin{bmatrix} \hat{p} \\ \hat{q} \end{bmatrix} \right\} \right\} \quad (6)$$

where the parameters (\bar{p}, \bar{q}) and (\hat{p}, \hat{q}) are respectively the fundamental and alternative instantaneous power components.

Finally, the reference currents generated by the controller are the results of the inverse Concordia transformation block:

$$I_{a ref} = \sqrt{\frac{2}{3}} I_{\alpha ref} \quad (7)$$

$$I_{bref} = \sqrt{\frac{2}{3}} \left(-\frac{1}{2} I_{cref} + \frac{\sqrt{3}}{2} I_{\beta ref} \right) \quad (8)$$

$$I_{cref} = \sqrt{\frac{2}{3}} \left(-\frac{1}{2} I_{cref} - \frac{\sqrt{3}}{2} I_{\beta ref} \right) \quad (9)$$

These reference currents are compared with the measured currents of the voltage inverter using a two levels hysteresis comparator. The comparator outputs define the switching orders of the voltage inverter.

III.2. High-level modelling, simulation and validation

The three-phase active filter system is modelled and validated using the VHDL-AMS description language. The digital control is modelled at a behavioural level of abstraction that allowed us to validate functionally its behaviour. The used data format at this stage is the real data format. We present in Figures 5, 6 and 7 some VHDL-AMS models of major analogue elements, here the inverter and current sensor models. The inverter model is based on an ideal switch model depicted in Figure 5. The high level behavioural model of the digital controller is presented in Figure 8; it is based on Ordinary Differential Equations and simultaneous statements [1]. The Total Harmonic Distortion (THD) of the grid currents is respectively equal to 24,9% and 2.4% before and after the filtering.

```

Library IEEE, disciplines;
Use disciplines.electromagnetic_system.all;
Use IEEE.Math_real.all;

Entity ideal_switch is
  Port (Signal Commande : in bit;
        Terminal a, b : electrical);
end entity ideal_switch;

Architecture equ of ideal_switch is
  Quantity V across I through a to b;
Begin
  if Commande = '1' use
    V = = 0.0;
  else
    I = = 0.0;
  end use;
end;

```

Fig. 5: VHDL-AMS model of an ideal switch.

```

Library work, Disciplines;
Use work.all;
Use disciplines.electromagnetic_system.all;

Entity inverter is
    generic ( U0 : real );
    Port (    signal Sa, Sb, Sc : in bit;
            Terminal P1, P2, P3 : electrical);
End entity inverter;

Architecture equ of inverter is
    Signal Sab, Sbb, Scb :bit;
    Terminal Vp0, gnd :electrical;
Begin
    source_U0 : Entity source(equ)
    generic map (U0 => U0)
        port map (Vp => Vp0 ,Vm => gnd);
    interrupteur_1 : Entity ideal_switch(equ)
        Port map (Sa, Vp0, P1);
    interrupteur_2 : Entity ideal_switch(equ)
        Port map (Sab, P1, gnd);
    interrupteur_3 : Entity ideal_switch(equ)
        Port map (Sb, Vp0, P2);
    interrupteur_4 : Entity ideal_switch(equ)
        Port map (Sbb, P2, gnd);
    interrupteur_5 : Entity ideal_switch(equ)
        Port map (Sc, Vp0, P3);
    interrupteur_6 : Entity ideal_switch(equ)
        Port map (Scb, P3, gnd);
    Sab <= not Sa;
    Sbb <= not Sb;
    Scb <= not Sc;
end architecture equ;

```

Fig. 6: VHDL-AMS structural model of the inverter.

```

Library disciplines;
Use disciplines.electromagnetic_system.all;
Entity sensor is
    Generic ( RED: real);
port (
    Terminal A :    electrical;
    Terminal B :    electrical;
    Quantity :      C_OUT: out real );
end;

Architecture arch_cc OF sensor is
    Quantity V_capteur1 across I_CAPTEUR1 through A to B;
Begin
    V_capteur1 == 0.0;
    c_out == I_CAPTEUR1/red;
end;

```

Fig. 7: VHDL-AMS model of an ideal current sensor.

III.3. High-level model of the architecture

In this section, we present and examine two architectures for the fully digital controller: the first one that we call “architecture 1” and which is directly imposed by the equations described in section III.1. The second one, called “architecture 2” is the result of an algorithm/architecture optimisation. Both architectures are firstly modelled using the real data format.

The “architecture 1” is naturally imposed by the equations (1) to (9). The data flow graph (DFG) of this architecture is presented in Figure 9. By using the VHDL-AMS mixed simulation environment validated in previous section, we validated the VHDL model of the “architecture1”.

```

library disciplines, ieee, work;
use disciplines.electromagnetic_system.all;
use ieee.math_real.all; use work.all;

entity control is
    generic(K, Kmv,Wc, Kc,Tc,C, zero, Vdc_ref : real);
port(
    quantity Va,Vb,Vc, Vdc_m, Ia,Ib,Ic : in real;
    quantity Ia_ref,Ib_ref,Ic_ref : out real);
end;

architecture arch_control of control is
    Valpha,Vbeta          :      real;
    quantity Ialpha,Ibeta :real;
    quantity Valpha_1,Vbeta_1 :real;
    quantity Ialpha_1,Ibeta_1 :real;
    quantity Ialpha_h,Ibeta_h :real;
    quantity p,q          :real;
    quantity p_1,p_2     :real;
    quantity Ialpha_ref,Ibeta_ref :real;
begin
    Valpha      ==      K*(Va - 0.5*Vb -0.5*Vc);
    Vbeta       ==      K*((sqrt(3.0)/2.0)*Vb -(sqrt(3.0)/2.0)*Vc);
    Ialpha      ==      K*(Ia - 0.5*Ib -0.5*Ic);
    Ibeta       ==      K*((sqrt(3.0)/2.0)*Ib -(sqrt(3.0)/2.0)*Ic);
    Valpha_1'dot ==      K*(Valpha - Valpha_1) - Wc*Vbeta_1;
    Vbeta_1'dot ==      K*(Vbeta - Vbeta_1) + Wc*Valpha_1;
    Ialpha_1'dot ==      K*(Ialpha - Ialpha_1) - Wc*Ibeta_1;
    Ibeta_1'dot ==      K*(Ibeta - Ibeta_1) + Wc*Ialpha_1;
    Ialpha_h    ==      Ialpha - Ialpha_1 ;
    Ibeta_h     ==      Ibeta - Ibeta_1 ;
    p           ==      Valpha_1*Ialpha_h + Vbeta_1*Ibeta_h;
    q           ==      Valpha_1*Ibeta_h + Vbeta_1*Ialpha_h;
    reg_ten_1:entity reg_ten(arch_reg_ten)
        generic map(Kc,Tc,C,zero,Vdc_ref) port map(Vdc_m,p_2);
    p_1 == p+p_2;
    Ialpha_ref == (1.0/(Valpha_1*Valpha_1 + Vbeta_1*Vbeta_1
        + 0.001))* (Valpha_1*p_1+ Vbeta_1*q);
    Ibeta_ref == (1.0/(Valpha_1*Valpha_1 + Vbeta_1*Vbeta_1
        +0.001))* (Valpha_1*q + Vbeta_1*p_1);
    Ia_ref == K*Ialpha_ref;
    Ib_ref == K*((-1.0/2.0)*Ialpha_ref + (sqrt(3.0)/2.0)*Ibeta_ref);
    Ic_ref == K*((-1.0/2.0)*Ialpha_ref -(sqrt(3.0)/2.0)*Ibeta_ref);
End arch_control;

```

Fig. 8 : VHDL-AMS model of the digital controller.

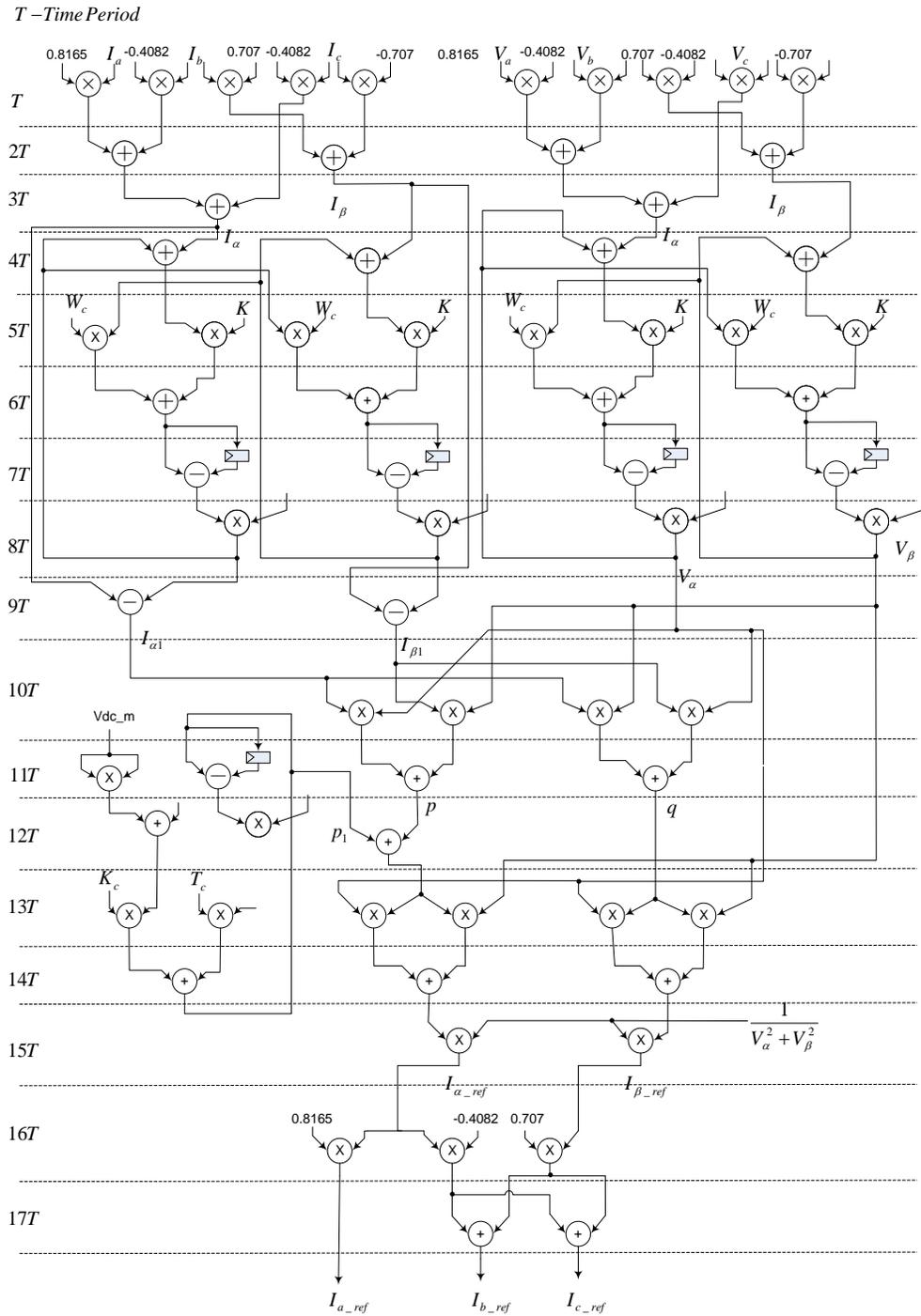


Fig. 9: Data flow graph for "architecture 1"

However, the number of operators for the "architecture 1" is too high and not optimised. We proposed the "architecture 2" based on two multipliers and two adders. The "architecture 2" includes multiplexers and registers necessary for storing of intermediate results. To handle all necessary operations, a Finite State Machine (FSM) based on 21 states is designed. The Data Flow graph of

this optimised architecture is presented in Figure 10. We modelled this architecture using the VHDL language and simulated it successfully in the mixed simulation environment previously described.

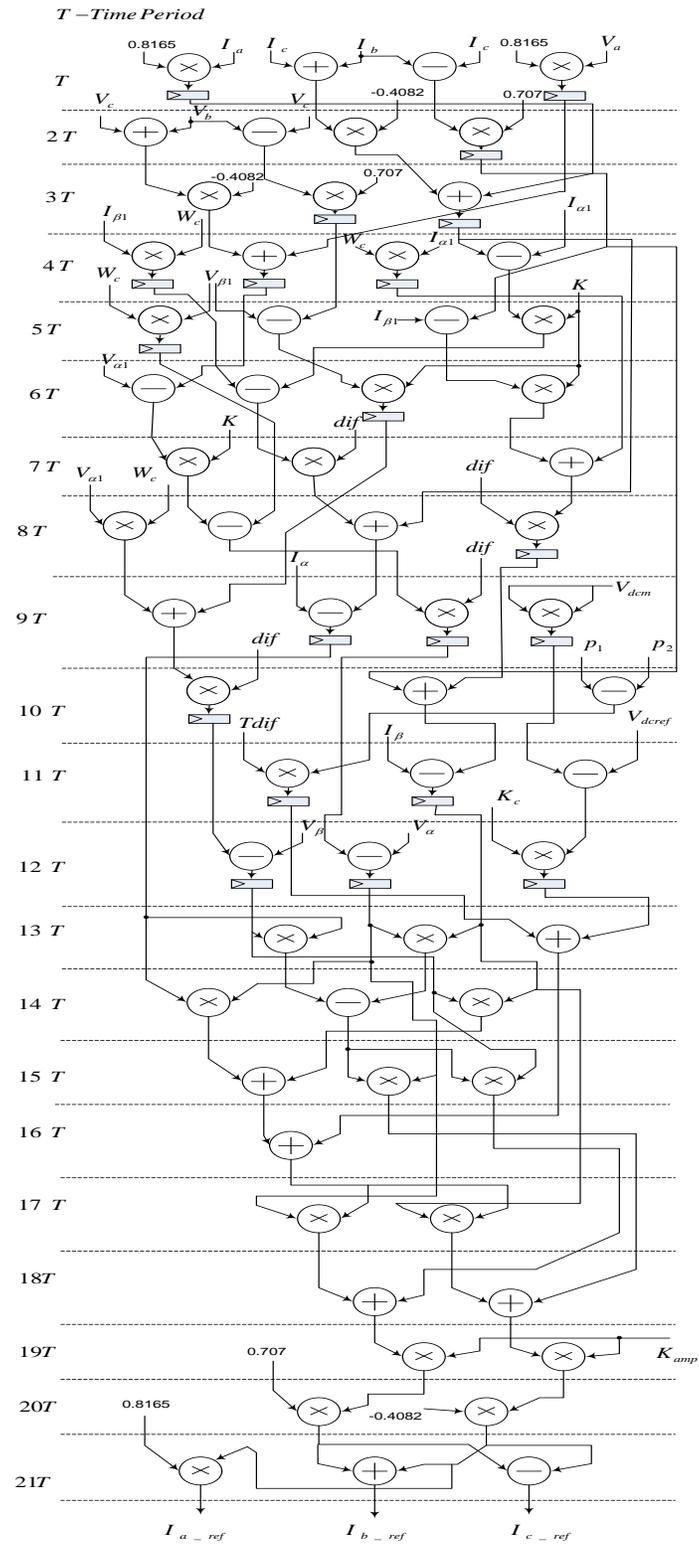


Fig.10: Data flow graph for "architecture 2".

III.4. Digital adaptation of the Control Algorithm

To implement the optimised “architecture 2” on a target FPGA, specific digital properties must be studied: we particularly studied specific data binary format (word length, fixed or floating point), mathematical and numerical calculation methods and quantization effects. Final digital properties are defined to minimize estimation error, which could decrease control performances.

III.4.1. Control Algorithm optimisation

Analogue electrical values are measured and converted using Analogue-Digital Converters (ADCs). The standard ADCs are based on 10-bit or 12-bit conversion. We note V_{ref} the scale factors for the voltages and I_{ref} for the currents. The expressions (1) to (4) become:

$$V_{\alpha} = \sqrt{\frac{2}{3}} V_{ref} \left(V_{ar} - \frac{1}{2} V_{br} - \frac{1}{2} V_{cr} \right) = V_{ref} V_{\alpha r} \quad (10)$$

$$V_{\beta} = \sqrt{\frac{2}{3}} V_{ref} \left(\frac{\sqrt{3}}{2} V_{br} - \frac{\sqrt{3}}{2} V_{cr} \right) = V_{ref} V_{\beta r} \quad (11)$$

$$I_{\alpha} = \sqrt{\frac{2}{3}} I_{ref} \left(I_{ar} - \frac{1}{2} I_{br} - \frac{1}{2} I_{cr} \right) = I_{ref} I_{\alpha r} \quad (12)$$

$$I_{\beta} = \sqrt{\frac{2}{3}} I_{ref} \left(\frac{\sqrt{3}}{2} I_{br} - \frac{\sqrt{3}}{2} I_{cr} \right) = I_{ref} I_{\beta r} \quad (13)$$

$$\begin{bmatrix} I_{\alpha ref r} \\ I_{\beta ref r} \end{bmatrix} = \frac{V_{ref}^2}{v_{\alpha}^2 + v_{\beta}^2} \left\{ \begin{bmatrix} V_{\alpha r} & -V_{\beta r} \\ V_{\beta r} & V_{\alpha r} \end{bmatrix} \left[\begin{bmatrix} \hat{p}_r \\ \hat{q}_r \end{bmatrix} + \begin{bmatrix} \hat{p}_r \\ \hat{q}_r \end{bmatrix} \right] \right\} \quad (14)$$

Where the variables (V_{ar}, V_{br}, V_{cr}) and (I_{ar}, I_{br}, I_{cr}) are respectively the normalized values in [-1,+1] of the measured voltages (V_a, V_b, V_c) and (I_a, I_b, I_c) currents.

Observing the equation (14) and comparing it with the equation (6), we conclude that to normalize values that appear in the algorithm, we have to replace the expression $\frac{1}{v_{\alpha}^2 + v_{\beta}^2}$ by $\frac{V_{ref}^2}{v_{\alpha}^2 + v_{\beta}^2}$.

III.4.2. Specific data binary format

To choose a specific binary format, an analysis must be carried out. We will consider that the error due to the binary data format must be made negligible in comparison with the error due to the ADC. In practical terms, that corresponds to define a specific binary fixed point format with a number of bits for the decimal part higher than the number of bits of the ADCs, which is described with the following expression:

$$\Delta q_f \ll \Delta q_c \quad (15)$$

where Δq_f and Δq_c are respectively the quantification error due to the specific binary format and the quantification error due to the ADC.

We choose a specific binary fixed-point format since the floating-point format would require too long execution time for mathematical operators and high silicon area.

To define the specific fixed-point format, we took three major parameters into account:

- Maximal value of operation results and constants;
- Minimal value of operation results and constants;
- Estimated control accuracy.

Firstly, the maximal computed value defines the integer size m_i , which avoids overflow situations. The maximum computed value for the proposed algorithm and for the control parameters defined in appendix I are defined by:

$$\frac{|V_d(t) - V_d(t-1)|}{T} < \frac{|V_d(t)|}{T} + \frac{|V_d(t-1)|}{T} < 2000 \quad (16)$$

Consequently, the bit number of the integer part, m_i , is established as:

$$2^{m_i} > 2000 \Rightarrow m_i = 11 \quad (17)$$

In the flow algorithm, small constants must be quantified by using at least 20 bits for the decimal part. By taking into account these constraints, we chose n equal to 32-bit to get a fixed-point format standard with a multiple of 8 bit. The resulting specific binary format is noted as [s,11,20] where s is the sign bit.

III.4.3. Synthesizable model and simulation results

Using the specific binary format chosen in previous section, we described the synthesizable models of the “architecture 1” and “architecture 2” whose data flow graph are respectively depicted in Figures 9 and 10. This synthesizable VHDL models were simulated using the same mixed environment. The simulation results are the same for both architectures and are presented in figure 11.

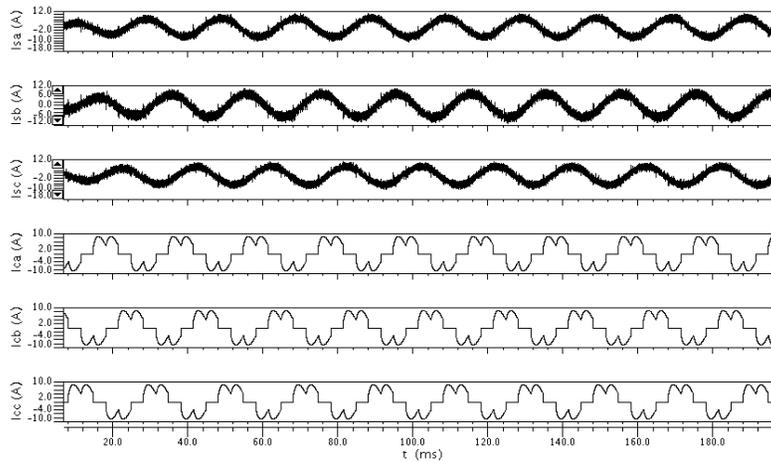


Fig. 11. Three-phase source currents after (top) and before (bottom) active filtering for both architectures.

Simulation results are perfectly coherent with those obtained before. The Total Harmonic Distortion (THD) is respectively equal to 24,9% and 2.6% before and after the filtering. It means that specific binary data format is judiciously chosen and digital adaptation of the algorithm does not decrease the architecture’s performances.

The advantage of the “architecture 1” is the large working frequency, the disadvantage is a very large silicon area. The optimised “architecture 2” is a little bit slower, but also requires a much smaller silicon area. Table 1 and Table 2 present comparison of those two architectures implemented on an FPGA *Xilinx Virtex-II 2V4000bf95* with *FPGA Advantage* CAD Tools.

	Input/Output[%]	Cellul Logic Block[%]
“Architecture 1”	48	64.33
“Architecture 2”	48	13.05

Table 1: Comparison of the two architectures - area criterion.

Table 1 details the comparison of the silicon area for the two architectures implemented in Xilinx VirtexII FPGA technology. The architecture 2 occupied more less area than architecture 1, with a ratio about 5.

	Tmin[ns]	fmax[MHz]
“Architecture 1”	196.56	5.087
“Architecture 2”	451.00	2.217

Table 2: Comparison of the two architectures - time criteria.

Table 2 details the comparison of maximal frequencies for the two architectures. The maximal frequency for the “architecture 1” is around two times larger than the one of the “architecture 2”. However, as far as power electronics applications are concerned, a frequency about 2 MHz is satisfactory because power semi-conductor switching is limited; its usual maximal value is about 20 KHz for the considered power rating.

IV. CONCLUSION

In this paper, we presented a Top-down design methodology using VHDL-AMS language to design a fully digital controller for power electronics systems. We have also presented a unique mixed simulation environment for modelling, simulation, functional validation and design of the digital controller. The proposed methodology allows fast design development time and short time-to-market. It can be used in any application field and can be applied in any other multidisciplinary domains.

The control algorithm of a shunt three-phase power active filter is analysed and an optimised architecture is proposed and detailed. Each block of this digital architecture is modelled using the VHDL language at several levels of abstraction, first of all, a real data format, and finally a specific binary format at synthesizable level. To achieve closed loop simulation of this architecture in its power context, analogue and power elements were modelled using the VHDL-AMS language. The whole closed loop system has been successfully validated using the ADVanceMS mixed CAD tools at any abstraction levels, from the high to RTL level.

The FPGA-based control of power electronics systems is an alternative to conventional digital processors. Moreover, this hardware approach is a first step towards mixed System-On-a-Chip for power control, including digital controllers, acquisition electronics, ADC and current measurement [18]. Consequently, the proposed methodology seems to be better suited than software implementation or hardware/software design for control system mixed integration. Moreover, it allows us to resolve major digital design and mixed simulation difficulties when designing analog and power ASICs.

Appendix I

Simulation parameters

Grid :	230Vrms, 50 Hz
Non-linear load:	R = 40 Ω , L = 40 mH,
Filter:	L _f = 1 μ H, r _f = 0,05 Ω
Filtering capacitor:	C _{dc} = 1 mF

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