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Circuit-Type modelling of SiC power Mosfet in short-circuit operation including selective fail-to-open and fail-to-short modes competition

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Abstract

SiC Mosfet has very unique properties in extreme operation such as a well-known fail-to-short failure mode but in competition with a lesser known fail-to-open failure mode. These two modes are generally studied and modelled separately, whereas, in practice, they are coupled with the junction temperature of the chip. This paper presents a circuit-type modelling approach of these two modes simultaneously. This modelling allows to simulate the selectivity and competition between these two modes, one is clearly critical and the other is advantageously safe. The proposed model is then compared with short-circuit test of 1.2kV-80mΩ MOSFET SiC.

1. Introduction and objectives

SiC Mosfet converters have been spectacularly developed to combine both high efficiency and a high level of compactness. Applications in the fields of transport, railway and also grid-connected PV inverters are targeted in the range of 10kW to several 100kW, in a medium range voltage, from 400V to 900V [1]. The robustness of SiC Mosfet device and the management of its protection are also the subject of extensive research in many laboratories because its short-circuit time capability (T_{SC}) is often lower than Silicon devices and varies greatly from one manufacturer to another [2]. The very thin gate-oxide (typically 50nm against 100nm for silicone-planar device) under a high gate field (4MV/cm compared to 10MV/cm breakdown field of the SiO_2) is highly stressed in short-circuit operation. Indeed, the junction temperature can reach at least 1300K, leading to hot carrier injection in the oxide that could explain the possible weakness of the gate region and its variability in extreme operation [3], [4].

Thus SiC Mosfet has unique properties in short-circuit operation such as a competition between a well-known drain-source fail-to-short (FTS) failure mode (also named "hard" failure mode, or again "catastrophic" failure mode) and a lesser known drain-source fail-to-open (FTO) failure mode (also named "soft" failure mode) caused by a gate – source short-circuit path. The FTS mode, comes from a thermal runaway and/or the parasitic BJT latch-up leading to the semiconductor local destruction and the

creation of a metallic path drain-source [5]. The FTO mode, comes from the Al top metal fusion and diffusion, caused by the extreme heat in short-circuit, between the polysilicon gate and the Al source. The location of this metallic path can be either on top of the chip between the gate fingers and the source pad below the passivation layer, and/or across the ILD (Inter-Layer Dielectric) through metallized cracks [6]–[11] caused by a very low thermal expansion coefficient of the SiO_2 compared to Al and SiC ones. In this last case, gate and source electrodes are shorted leading to a FTO mode.

FTS and FTO modes are generally studied and modelled separately, whereas in practice they are coupled with the temperature of the chip. However, the thermal runaway of the FTS mode is governed by the local temperature at the maximum field along the depletion region, while the FTO mode is dependent of the top metal melting and the ILD cracks which are governed by the oxide thermo-mechanical capability.

This paper presents for the first time a circuit-type modelling approach of the SiC Mosfet including the global thermal dynamic of the FTS and FTO modes simultaneously. This modelling allows to simulate the selectivity and competition between these two modes, one is clearly critical and the other is advantageously safe. The proposed model is then compared with short-circuit test of 1.2kV-80mΩ MOSFET SiC.

The paper is organized in four sections. Section 2 presents the circuit-type electro-thermal modelling of

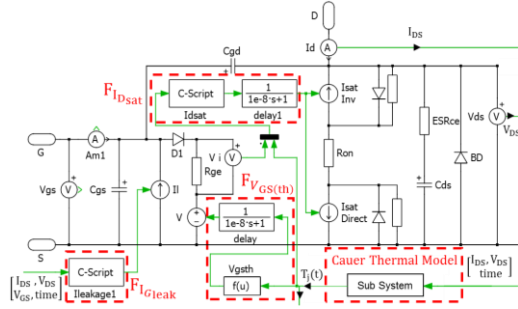


Fig. 1. Electro-thermal PLECS™ Circuit-type modelling-base for SiC Mosfet in short-circuit operation. $F_{I_{GLeak}}$, $F_{V_{GSth}}$, $F_{I_{DSat}}$ are respectively modelling function for $I_{GLeak}(T_j)$, $V_{GSth}(T_j)$ and $I_{DSat}(T_j)$.

a SiC Mosfet based on V_{GSth} , I_{DSat} and I_{GLeak} thermal-dependency. Section 3, deals with the FTO and FTS modelling separately but using the same circuit-type approach which will be embedded in the same model base. Finally, in section 4, the two failure modes are put in competition situation along two short-circuit test and compared with experimentation. The first one under a reduced drain-source voltage, where a stable FTO mode occurs. The second one, under a nominal drain-source voltage where the FTS mode happens after an instable and incomplete FTO mode.

2. Circuit-type electro-thermal modelling

The short-circuit operation shows a very fast thermal dynamics over a wide temperature range (from 300K to more than 1500K in a dozen of μs). Such a stress dynamic can reveal specific drift mechanisms or even degradation mechanisms of weak region which are not visible in nominal operation [2]. For example, the strong gate-source leakage-current is caused by a hot electron injection through the thin gate oxide [4] and the high drain-source peak current decreases as the channel mobility decreases at high temperature [12]. As a matter of fact, in order to model and fit the thermal-dependant physical mechanisms involved during the short circuit operation, an extended electro-thermal modelling is needed. The authors previously presented in [13] a compact and non-segmented electro-thermal model including circuit elements as illustrated in Fig. 1. Note that in the following, all numerical values, unless otherwise specified, are fitted in relation with a 1.2kV-80m Ω DUT, ROHM™ SCH2080 (generation II), based on an active area $\approx 12.4\text{mm}^2$, in TO247 package.

2.1. First thermal modelling

Due to the very short transient operation ($<100\mu s$)

clearly less than the thermal time constant of the chip, a diffusive 1D thermal model is sufficient. Then an 1D Comsol™ model of the chip's layers has been developed [13] including the electric field distribution E_x around the P+/N- depletion region. This model is fed by a time-dependant current density $J_x(t)$ coming from experimental curves. At this stage, the gate regions, with polysilicon gate fingers, SiO_2 and the ILD are not modelled because of their very small thickness ($<1\mu m$) and the possible mesh size problem in a FEM approach. A single temperature value is therefore considered in the thermal modelling, named T_j in the depletion zone at the maximum electric field position. However, the thickness of the top Al metal layer is only taken into account with an increase of the P-well thickness. Note that in SiC structure, the drift region is realized by a very fine epitaxy layer of about ten microns compared to a 300 μm substrate. The gate oxide is also very thin (50nm) on which the Al layer is only 5 μm thick. Given the small dimensions involved in the active zone, we have shown in [13] that the thermal gradient between the maximum electric field position and the gate region is very limited. Then authors only consider the temperature at the maximum electric field position of the depletion zone. In order to adapt this model into PLECS™, the 1D model can be either discretized at a constant geometric step Δx or fitted on a time-domain response to extract an equivalent Cauer's line (R_{thi} , C_{thi}) with a reduced number of cells (typically 30) or embedded by means of a vectorization formalism in a PLECS' functional block. Moreover, due to the "snap" effect of the electric field peak localized around the depletion region, a distributed power heat flux along the 1D x-axis is not necessary. Then a localized input instantaneous heat flux $\phi[W, t]$ connected at the input port of the Cauer's line is sufficient.

2.2. Electric modelling

It has been shown in [2] that the gate leakage-current can be modelled by an ohmic gate-source dipole whose value is in relation to the temperature inside the gate region. Relation (1) gives the behavioral gate leakage-current model in relation to the adiabatic thermal energy accumulated during the short-circuit sequence (E_n) by means of a polynomial equivalent conductance. It is specifically fitted using the *fit* Matlab™ optimization function with experimental values. An offset function is also introduced which is independent of the gate polarization. In this relation, p_{ij} coefficients are in relation to the drain-source voltage applied to the DUT. For 600V, $T_{case} = 25^\circ C$ and $V_{GS} \in [18V, 21.5V]$, it was extracted : $p_{01} = 9.51$,

$$p_{11} = 9.44, p_{21} = 2.512, p_{00} = -156.08, p_{10} = -150.35,$$

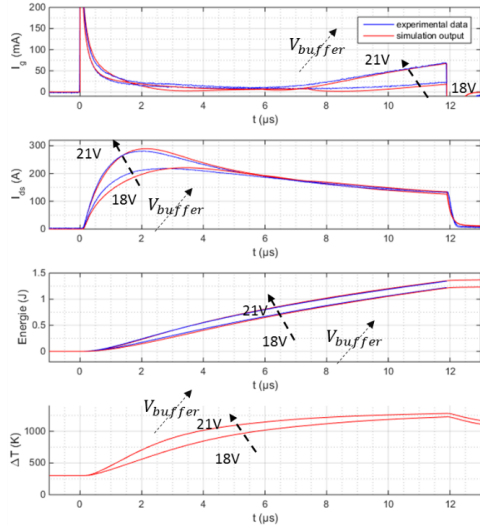


Fig. 2. Type 1 short-circuit SiC MOSFET model evaluation in PLECS™ software for different buffer voltages bias (@ $V_{DS} = 600V$, $T_{jinit} = 25^\circ C$ and $R_G = 47\Omega$).

$$p_{20} = -36.05, p_{30} = 0.628.$$

$$I_{Gleak} = (p_{01} + p_{11}E_n + p_{21}E_n^2) \cdot V_{GS} +$$

$$p_{00} + p_{10}E_n + p_{20}E_n^2 + p_{30}E_n^3 \quad (1)$$

Relations (2) is the well-known physical relations modelling the saturation current (I_{Dsat}). Relation (3) model the channel mobility (μ_n) in function of the temperature (T_j) using the Matheissen's mobility rule [14]. Relation (4) model the threshold voltage ($V_{GS(th)}$) as an equivalent linear model [15].

$$I_{Dsat}(T_j) = \frac{\mu_n(T_j) \cdot C_{ox} \cdot Z}{2L} \cdot (V_{gs} - V_{gs(th)}(T_j))^2 \quad (2)$$

$$\mu_n(T_j) = \frac{\mu_{a0} \left(\frac{T_j}{T_0}\right)^a}{1 + \frac{\mu_{a0}}{\mu_{b0}} \left(\frac{T_j}{T_0}\right)^{b-a} + \frac{\mu_{a0}}{\mu_{c0}} \left(\frac{T_j}{T_0}\right)^{c-a}} \quad (3)$$

$$V_{GS(th)}(T_j) = x_1 \cdot T_j + x_2 \quad (4)$$

Where: μ_{a0} , μ_{b0} , μ_{c0} are mobility parameters at ambient temperature (300K) and a , b and c are sensitive thermal coefficients which have been fitted with experimental measures and temperature extracted from the thermal model presented in the previous subsection in order to obtain a wide range temperature model: [in $cm^2 \cdot V^{-1} \cdot s^{-1}$], $\mu_{a0} = 2.33$, $\mu_{b0} = 2.95$, $\mu_{c0} = 1.94 \cdot 10^3$ and: $a = -1.48$, $b = -4.8$, $c = 2.56$. In the same conditions thee threshold voltage parameters, x_1 and x_2 , have been extracted: $x_1 = -0.025$

$$V/K, x_2 = 15.4V.$$

2.3. First validation of the electro-thermal model

The previous model is evaluated in a short-circuit simulation with a $12\mu s$ pulse for two values of $V_{GS} = 18V$ and $21V$, results are presented in Fig.2. In both cases, the model accurately represents the gate leakage-current with only a few % error. The drain-source current is slightly over-estimated for $V_{GS} = 21V$ while it is slightly under-estimated for $V_{GS} = 18V$. However, the estimation of the adiabatic energy remains very accurate. Note this one greatly exceeds 1000K after $10\mu s$. Such a temperature level is in agreement with recent publications using the same modelling approach but on different chips' size [16] or considering a different V_{DS} bias [17].

3. Fail-to-open and Fail-to-short modelling

In this section the previous electro-thermal model is extended to include FTO and FTS modes. These will be modelled separately because they represent different mechanisms which will be explained in this

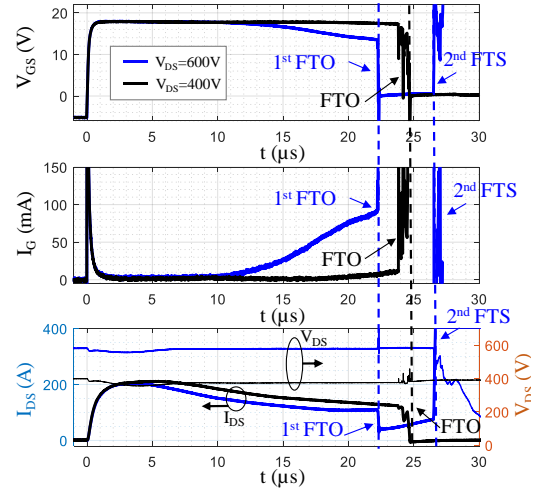


Fig. 3. Experimental FTO and FTS modes in type 1 short-circuit operation for $V_{DS} = 600V$ (cascaded modes) in blue curve and for $V_{DS} = 400V$ in black curve, (@ $T_{jinit} = 25^\circ C$, $V_{buffer(on/off)} = 18V/-5V$ and $R_G = 47\Omega$).

section.

3.1. FTO mode analysis and modelling

Previous thermal simulations shown that the maximum junction temperature near to the top surface can significantly exceed the melting temperature of the Al layer ($660^\circ C$ or $933K$) [13]. Some failure

analysis have shown that the Al fusion cause metallic bridges between source and gate electrodes only if the heat power density is limited by mean of a reduced drain-source voltage $V_{\text{supply}} \cong 450\text{V}$ instead of 600V

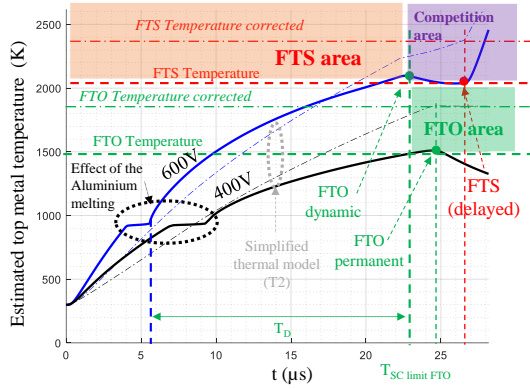


Fig. 4. Simulated temperature from waveforms presented in Fig. 3. The simulation includes melting Al (transition phase) and experimental comparison (dots). FTO, FTS modes and competition areas definition. Black curve $V_{\text{DS}} = 400\text{V}$, blue curves $V_{\text{DS}} = 600\text{V}$ @ $T_{\text{jinit}} = 25^\circ\text{C}$, $V_{\text{buffer}} = 18\text{V}$.

[18], [19].

As shown in Fig. 3, below a given drain-source voltage, the FTO mode is guaranteed. Above this voltage the FTO mode is overtaken by the FTS mode which will be described in §3.2. Indeed, for a reduced drain-source voltage, the heat power density is limited, which therefore reduces the junction thermal dynamics of the chip, allowing a sufficient delay time for the top Al metal to diffuse under the passivation of the chip to form a stable Al metal bridge leading to the device natural turn-off and cooling [19]. In addition, thermal shocks at the Al-SiO₂/ILD and Al-SiC interfaces yield significant differential strains which causes cracks and metal infiltration between source electrode and gate fingers as it was seen on others SiC devices [7]–[10]. These two metallurgical and thermo-mechanical mechanisms allow to understand the origin of the FTO mode [6], [18], [19].

In Fig. 4, the top metal temperature estimation from the experimentation is presented the colours of Fig.3 are respected. The temperature is estimated with an enhanced version of the 1D thermal model presented in §2.2. The thermal sensitivity of the thermal conductivity and the specific heat capacity of the chip materials (Al and SiC) are also modelled from [20], [21] as well as the Al phase-transition from solid to liquid state around 660°C (933K). Based on [20], the heat capacitance in the solid state and the liquid state is displayed in Fig. 5. Relation (5) gives respectively

the relation between the solid state capacitance to the fusion state model to the liquid state model.

$$C_p = C_{pS}(T) \cdot (1 - \alpha(T)) + C_{pL} \cdot \alpha(T) + L_f \cdot \frac{d\alpha}{dT} \quad (5)$$

With : C_{pS} , solid state heat capacitance which is temperature-dependent [20]; L_f , heat of fusion ($L_f = 397 \text{ kJ/kg}$ [20]); C_{pL} , liquid state heat capacitance which is typically considered as a constant value ($C_{pL} = 1.175 \text{ kJ/(kg.K)}$ [20]); $\alpha(T)$ is a phase transition function chosen as a cumulative function of a normal distribution (6) as also illustrated in Fig. 5. The normal distribution is centered in T_f and with a variance $\sigma = 5\text{K}$. The solid and liquid phases of the heat capacitances are combined with the phase transition function to have a smooth transition during fusion. The integration of the normal law gives 1 and multiplying it by the heat of fusion gives the amount of latent heat released during the phase transition. The transition will take place on the interval $6\sigma = \Delta T_{s \rightarrow l}$. For aluminum and also to ensure the convergence of the numerical model, $\Delta T_{s \rightarrow l} = 30\text{K}$. During that time, the material is supposed in a mixed state between solid and liquid.

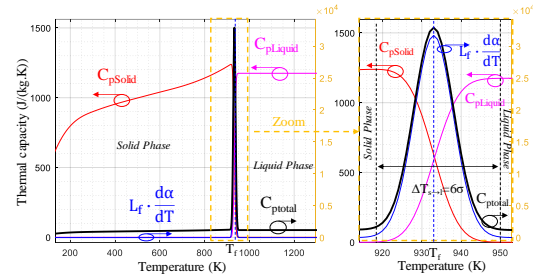


Fig. 5. Thermal-dynamic heat capacitance modelling of Al layer for FTO modelling.

$$\alpha(T) = \int_{-\infty}^T \frac{d\alpha}{dT}(x) dx \quad (6)$$

The proposed modelling is by default implemented in Comsol™. The solid line curves in Fig. 4 show that it allows to simulate by a quasi-plateau corresponding to the quantity of latent energy to be dissipated in order to produce the Al layer phase change. [16] recently proposed the same modelling approach based on our work by including a sensitivity study to the physical parameters.

Concerning the circuit-based electro-thermal modelling of the DUT, these curves are fitted by a Cauer's line of 8 elements with constant parameters to easily allow an integration in PLECS™. The responses of the Cauer's lines are superimposed in a dotted line in Fig. 4. This line represents the simulated

response in a very average way and therefore above all in a qualitative way.

The conditions to access the FTO area safely is presented by means of a "green safe area" in the transient thermal domain: the junction temperature must be at least 1500K and at least 17 μ s after the total melting of the Al, called delay time (T_D). The reference [6] showed that the quasi same FTO temperature is obtained for a different chip manufacturer but with a smaller size and therefore with a lower T_{sc} . Only 100K separates the two FTO temperatures of the two chips while the sizes are in a 1.2 ratio and the T_{sc} in a 2 ratio. These results show that the FTO thermal level is not very variable over a wide range of chip characteristics.

Given the significant temperature difference involved, we believe that the two failure mechanisms are well differentiated. Moreover, experimentally, the authors have verified the existence of these two types of failure-modes on a set of about ten DUTs components. The dispersion is not significant either on the T_{sc} value (17 μ s) or on the specific drain – source voltage value, $V_{DS} \cong 400V$, that define the boundary between the two modes.

3.2. FTS mode analysis and modelling

As seen in Fig. 3 with the blue curve ($V_{DS} = 600V$), the FTS mode is triggered before the consolidation of a complete FTO mode. Such a model concerns the representation of the drain-source leakage current by thermal generation [5]. A Shockley-Read-Hall (SRH) carriers generation model is used by means of relation (8) [5], [22] because it allowed to represent globally the drain leakage obtained in an experimental way. The thermal runaway dynamic of this leakage leads to the FTS mode. In SRH generation, W_D is the space of charges width in short-mode under V_{DS} defined in relation (9) and n_i the intrinsic density of charge carriers described in relation (10) [23].

$$I_{th}(T) = \frac{qW_D n_i(T)}{\tau_g} S \quad (8)$$

$$W_D = \sqrt{\frac{2\epsilon_s}{q} \cdot \frac{N_d + N_a}{N_d N_a} \cdot V_{DS}} \quad (9)$$

$$n_{iSiC}(T) = 1.7 \cdot 10^{16} \cdot T^{\frac{3}{2}} \cdot e^{-\frac{2.08 \cdot 10^4}{T}} \quad (10)$$

With: τ_g , is the SRH generation lifetime [1ns, 1 μ s] from [21][24]. We used this parameter τ_g as a fitting variable (fixed at 1ns) so that our model produces the same drain –source current and failure time at 600V than the experiment. This fit was also evaluated at

400V giving a T_{sc} value in FTO mode very close to the experiment. Our model is therefore robust. The

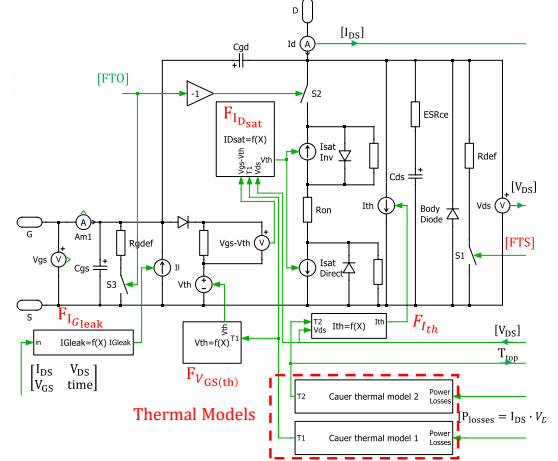


Fig 6. Final proposed electro-thermal SiC Mosfet model for short-circuit simulation including FTO and FTS modes modelling.

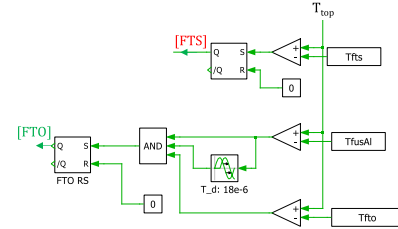


Fig 7. FTO and FTS functional blocks management for the model configuration described in Fig. 7, with : $T_{fuscorrected} = 2400K$, $T_{fusAl} = 933K$, $T_{fto corrected} = 1900K$.

results of this model is presented in the next section in the simulation vs experimentation.

4. FTO and FTS modes competition: simulation vs experimentation

The complete proposed model is depicted in Fig. 6. In addition to electro-thermal modelling of the gate leakage-current, drain-source current and threshold voltage as described in §2, a dedicated FTO and FTS circuit-parts have been included. FTO mode is modelled by a gate-source parallel failed-resistor R_{gdef} (0.1 Ω) controlled by switch S_3 and associated with switch S_2 to force the channel turn-off. These two switches are managed by the functional block diagram presented in Fig. 7: if the top metal estimated temperature is higher than the Al fusion temperature (933K) and the FTO threshold temperature T_{FTO} after the delay time T_d (17 μ s), the FTO mode is triggered by a latch gate. As illustrated in Fig. 4, the estimated temperature comes from a simplified fitted Cauer's line on the phase-transition curve of the top metal

temperature. This thermal line is named T_{top} in Fig.6. FTS mode is modelled by a parallel leakage drain-source controlled current-source I_{th} and F_{lth} block that

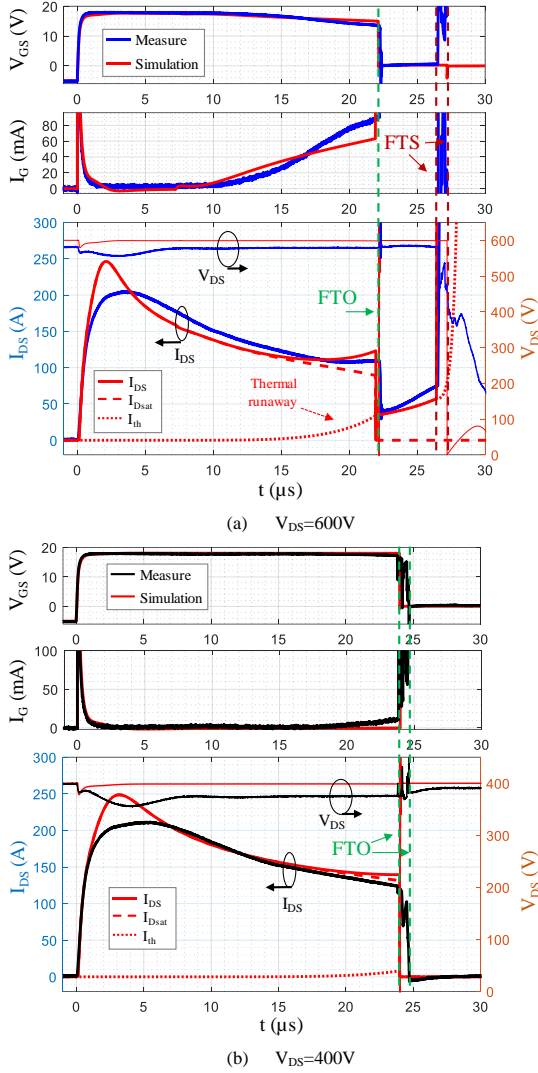


Fig 8. Comparison between the proposed model and the short-circuit failure modes experimentation at $V_{buffer} =$

includes the SRH generation model studied in §3.2. This block is fed by the same thermal line T_{top} . If the estimated temperature is higher than T_{FTS} , the FTS mode is triggered and a dedicated switch S_1 force the turn-on through a failed resistor R_{def} ($5m\Omega$).

The evaluation of the model is given in Fig. 8 in comparison with experimental results from a test-bench described in [2]. At nominal voltage, in Fig. 8a), due to the high thermal dynamic stress applied to the chip, the proposed model is able to highlight the cascaded FTO and FTS modes: the drain-source leakage current is too high to prevent thermal

runaway. Note that the dedicated drain-source leakage component is drawn in dashed line. At reduced voltage but with the same pulse duration, in Fig 8b), due to the low thermal dynamic stress applied to the chip, the FTO mode is the unique and stable mode. The low drain-source leakage current is clearly not enough to trigger the thermal runaway and the FTS mode does not appear.

5. Conclusion

In this article, the authors proposed a complete electrothermal circuit-type model for SiC Mosfet in short-circuit operation able to reproduce the new FTO mode in conjunction with the well-known FTS failure modes. The modelling of the dynamic drain-source carriers thermal generation combined with the FTO and FTS thermal thresholds allow to predictively simulate and to highlight either a specific cascaded failure modes at nominal voltage or an original safe FTO mode at low voltage as analysed from experimentation. This approach complements and extends in an original way the known electrothermal power device models. Finally, the proposed compact model has the following uses and interest:

- modelling and prediction of the T_{sc} and E_{sc} (robustness study model),
- modelling and prediction of failure-modes (failure modes study model),
- modelling separately I_{GS} (leakage), V_{GS} drop and I_{DSS} (leakage) (diagnostic study model).
- fully compatible with gate driver protection design or fault propagation analysis in different conversion architectures.

Acknowledgements

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