Monolithic asymmetric switching cells integrated on vertical multi-terminal Si power chips

Abdelhakim Bourennane, Adem Lale, Frédéric Richardeau

Monolithic asymmetric switching cells integrated on vertical multi-terminal Si power chips

Abdelhakim Bourennane[(1)], Adem Lale[(1,2)], Frédéric Richardeau[(2)]

[(1)]LAAS-CNRS, University of Toulouse, CNRS, UPS, Toulouse, France
[(2)] LAPLACE (Laboratoire Plasma et Conversion d'Energie), University of Toulouse, CNRS ENSEEIHT, 2 rue Charles Camichel, BP 7122, F-31071 Toulouse cedex 7, France

Tel.: +33 / (5) – 613.368.12
E-Mail: abourenn@laas.fr

Acknowledgements

This research work received financial support from the French National Research Agency (ANR). The project name is "ConvPlUS", ANR-13-JS09-0008-01, using the technological support of RENATECH-LAAS and 3DPHI platforms.

Keywords

« Monolithic integration », «switching cell», « N-IGBT », « P-IGBT », « PiN diode », « multi-terminal Si power chip », « multi-phase Inverter ».

Abstract

Power electronic converters (power modules) are essential devices for high efficient power management. Applications are ever more demanding in terms of compactness, reliability and cost reduction with increased intrinsic performance. The current technology of standard power modules, that use IGBT chips, is reaching its limits and the margins for improvement do not allow to meet the short-term emerging needs. Indeed, in a standard power module, each switching cell requires the manufacture of two chips and two wirebonds for interconnections. Each wirebond is a source of stray inductance and constitutes a limiting factor of electrical performance, a source of an increase in the level of electrical stress and of reliability problems. It is customary to place a decoupling capacitor on the power supply terminals of the switching cell. This capacitor makes it possible to compensate the stray inductance prior to the switching cell but it doesn't compensate in any way the stray inductance within the switching cell. This paper proposes for the first time a concept of an ultimate monolithic wire-bondless switching cell that allows to suppress the wirebonds within the switching cell and therefore minimize the stray inductance value. Consequently, it is suited for the emerging applications requiring to achieve simultaneously: reliability, compactness, intrinsic performance and reduced manufacturing cost.

Introduction

Currently commercialized conventional power modules are generally realized using 2D hybrid packaging technology in which two-terminal power dies such as Insulated Gate Bipolar Transistor (IGBT) and PiN-diode are bonded on their backside and interconnected using wire bonds. A power module is made of a great number of two-terminal dies that are interconnected by wire bonds. Power modules are therefore bulky and their mass fabrication is limited in productivity. Moreover, wire bonds in power modules are source of parasitic inductance [1-2] that induces high turn-off voltage overshoot, which not only add electrical stress on the power dies, but also result in switching losses and thus affect the overall efficiency. Another undesirable phenomenon regarding the 2D standard power modules concerns the common mode currents. Indeed, the mid-point of each phase-leg is at a floating potential that evolves as function of the high dv/dt during switching phases, the worst cases

being well-known: at low load-current turn-on and at high load-current turn-off. The mid-point being electrically contacted to the substrate through wire-bonds generates common-mode currents through the parasitic capacitors resulting from the succession of the layers that form the circuit board and the heat-sink. It is important to limit the amplitude of this current through the use of common mode filters.

To improve reliability, electrical performance and reduce cost of power modules, significant breakthrough can be achieved by the monolithic integration of the 2D-multiphase module within a minimum number of multi-terminal dies that are judiciously packaged. Different approaches for converter integration were described in literature in order to reach similar objectives. However, they are either limited in performance (lateral integration with vertical insulation trenches [3]) or require a complex technological process for their realization (molecular bonding of two wafers [4]). Within the same context, the authors have recently proposed vertical quasi-monolithic integration approaches of power converter [5-9].

Generally, the adopted strategy for integrating multi-phase power converters resides on a fractionated integration of the switching cell with a full separation between the high-side and the low-side switches of the converter [5-9]. Indeed, the high-side part of the converter is integrated in one multi-terminal power chip while the low-side part is integrated in another multi-terminal power chip. Even though the followed strategy permits to minimize the number of multi-terminal chips for the converter realization, the functionality of the elementary switching cell can only be synthesized by interconnecting at least two power chips. The new approach proposed in this paper aims at integrating monolithically the switching cell, in a buck or boost mode, within a single silicon chip. The realization of a phase-leg, unidirectional in current, requires consequently only one chip. The current bidirectionality, which is required in the case of an inverter, necessitates the use of two chips per phase-leg. The new proposed approach allows realizing a monolithic switching cell with an intra-silicon switching loop that one can qualify as the ultimate loop.

The paper focuses on the ultimate monolithic switching loop. Its operating modes are validated by Sentaurus^{TM} 2D simulations and the optimized packaging of the chips is discussed.

The concept of ultimate wire-bond-less monolithic switching cell in a silicon substrate

The concept of integrating asymmetric cells is illustrated in Fig.1 and described in [6]. It aims at integrating the voltage inverter-leg within two macro-monolithic chips. One chip that monolithically integrates the high-side IGBT with the low-side diode named a buck-switching cell and the other integrates the low-side IGBT with the high-side diode and is named a boost-switching cell. The boost-cell is integrated in an N-substrate while the buck-cell is integrated in a P-substrate. The gates of the IGBTs are controlled with respect to two constant reference potentials imposed by the external power supply. The gate of the P-IGBT is controlled with respect to VDC while the gate of the N-IGBT is controlled with respect to ground. As a result, the power supplies of the gate drivers are not polluted by mid-points dv/dt at switching, ensuring thus a safer operation. These reference electrodes allow sharing the power supply of the different gate drivers that are referenced to the same electrode. Consequently, only two power supplies are required for the gate drivers of a multiphase converter. This reduces the complexity of the power circuit, reduces the costs and improves reliability.

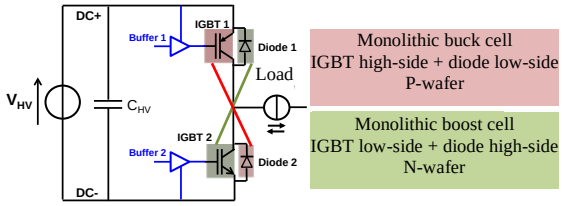


Fig. 1. Illustration of the monolithic switching cell concept.

Fig. 2 shows the monolithic structure of the boost switching cell, integrating an N-IGBT and a diode on N^-substrate. The backside thick P^+ region is used as the anode region of the diode and as a collector

region of the IGBT. This backside P^+ region is also used as a mechanical support for the partial vertical N^+ wall for lateral electrical insulation. Fig. 3 shows the monolithic structure of the buck switching cell integrating a P-IGBT and a P-diode on a P-epitaxial substrate. The backside N^+ region is used as the cathode region of the diode and the emitter region of the IGBT. This backside N^+ region is also used as a mechanical support for the partial vertical P^+ wall for lateral electrical insulation. Each chip is a three-terminal chip (3 power electrodes): the DC^+ and DC^- electrodes that are placed on the front-side are the two electrodes of the external power supply while the third electrode placed on the backside is the phase-leg mid-point. One can notice that no wirebonds were required to realize the switching cell. Consequently, this switching cell can be qualified as being the ultimate switching cell. To realize a complete voltage inverter phase-leg, the two complementary chips need to be assembled.

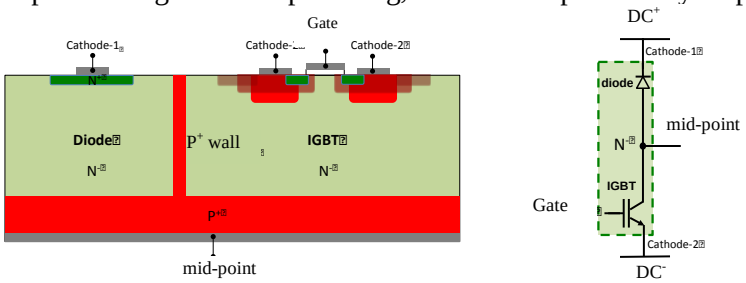


Fig.2. (a) 2D cross sectional view of the monolithic wireless boost cell and (b) electrical circuit.

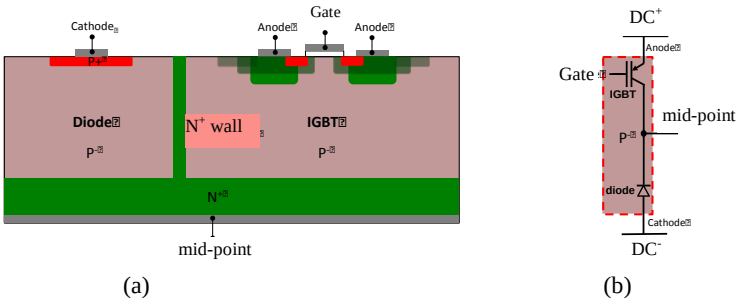


Fig.3. (a) 2D cross sectional view of the monolithic wireless buck cell and (b) electrical circuit.

Fig. 4 shows a possible packaging of the two complementary monolithic switching cells. The chips are bonded by their backside in a conventional manner. By analyzing this assembly, one can remark that the fact that the electrodes DC+ and DC- are on the front-side make easier their connection to the busbar using a unique connection like a (ribbons, integrated busbar, copper clip or direct lead bonding). Such interconnect permits to minimize stray inductance between high voltage DC supply and the power chips. A second interesting property concerns the possibility of placing a decoupling capacitor above each chip. Gate drivers can also be placed above the chips on the same horizontal plane of the busbar. This can be achieved by gathering the drivers and the busbar on the same PCB that will be placed above the chips.

One drawback of this packaging resides in the placement of the phase-leg mid-point (PM). Indeed, this latter is bonded on the PCB substrate. The voltage of this mid-point voltage varies according to the commutations dv/dt and is a source of the undesirable common mode parasitic current that flows through the capacitive layers of the PCB substrate. An alternative packaging to overcome this drawback would consist in flipping the chips but that leads to an increase in the complexity of packaging technology process (not studied in this paper).

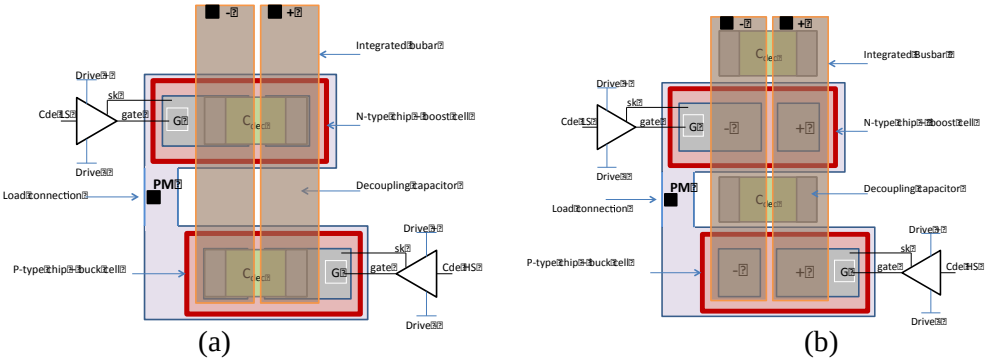


Fig. 4. Proposed assembly of the inverter phase-leg consisting of two complementary cells: (a) version with decoupling capacitors above the chips and (b) version with decoupling capacitors placed on the sides of the chips.

Validation of the operating modes of the ultimate wire-bond-less single switching cell

The operating modes of the two monolithic ultimate switching cell were analyzed using Sentaurus™ 2D simulations. The active area of each switch section within each multi-terminal chip is 1cm^2 for a 600V rating. Each chip is first simulated separately within a chopper circuit application and then they were assembled to form a full voltage inverter phase-leg.

Basic boost switching cell

The monolithic boost switching cell was simulated during a full switching cycle. The two conducting modes of the switching cell were analyzed by observing current density distribution as well as equipotential lines within the structure. The main objective is to check that when one section is in conducting state, the other is in off-state and supports the applied DC bus voltage with a negligible leakage current.

Fig. 5 shows 2D simulation results for IGBT mode. Fig. 6 shows 2D simulation results for diode mode. In the IGBT mode, one can notice a high current density in the right-most IGBT section and decreases as one moves towards the diode section. The current flowlines flow from the backside mid-point region towards the emitter electrode of the IGBT in the front-side. The DC-bus voltage is supported by the diode section and a space charge region expands within the N- drift region of the diode. The junction P$^+$wall/N- is reverse biased. In the diode mode, one can notice a high current density in the left-most section of the chip. The mid-point voltage is almost at the DC-bus voltage and therefore the space charge region expands within the N- drift region.

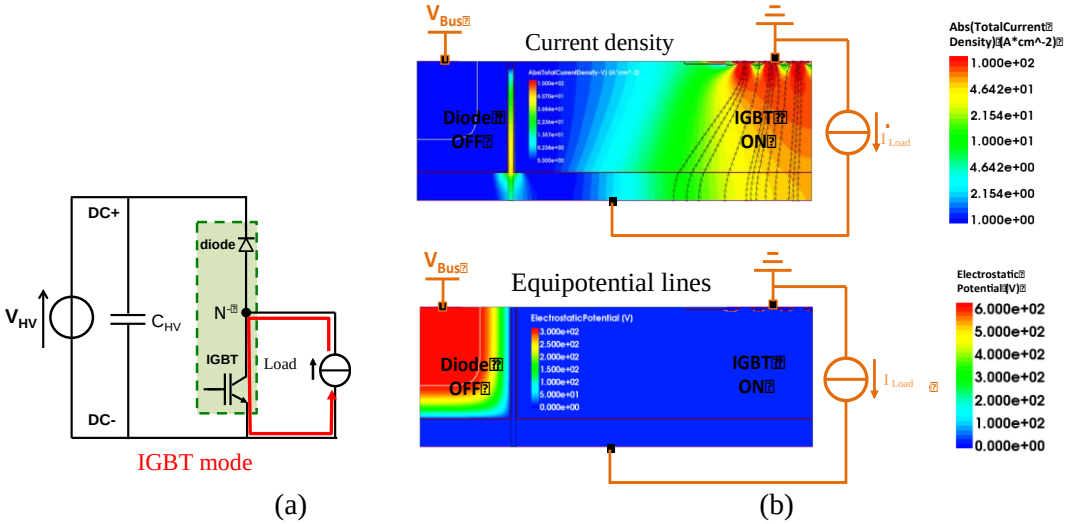
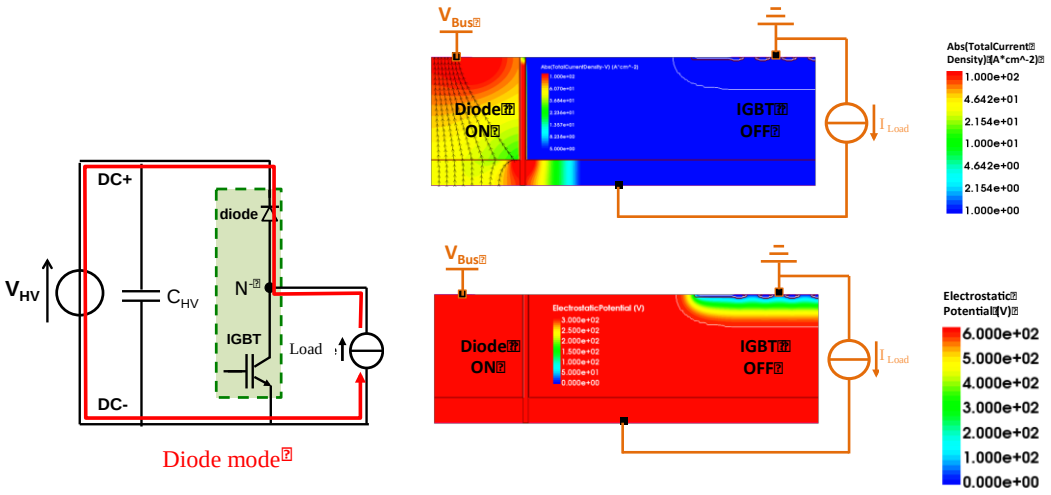


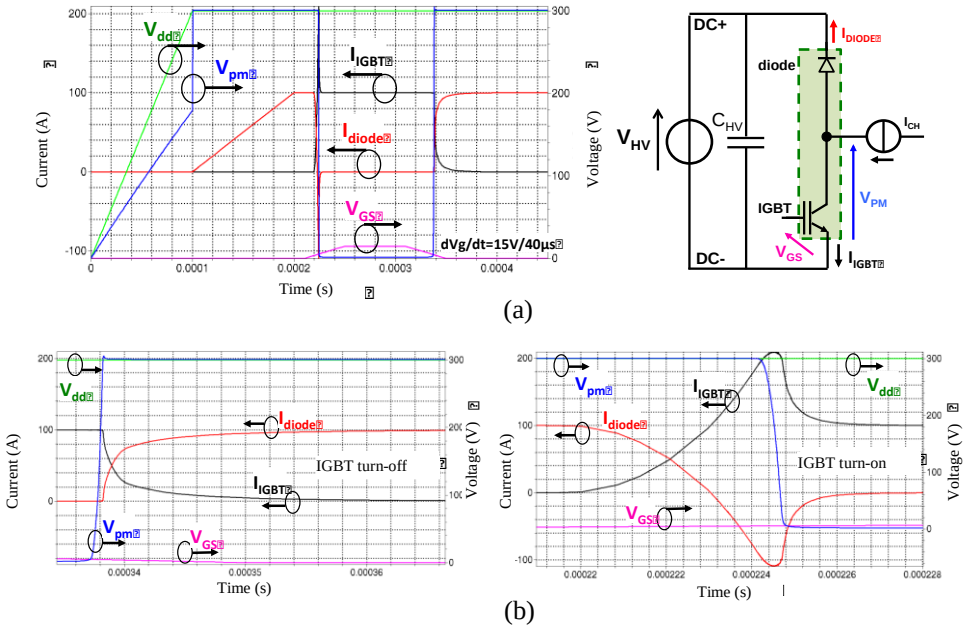
Fig. 5. (a) IGBT mode of the boost cell, (b) current density and equipotential lines in IGBT mode.



(a) (b)

Fig. 6. (a) Diode mode of the boost cell, (b) current density and equipotential lines in diode mode.

The current and voltage waveforms in the boost cell for one full switching cycle are shown in figure (a). One can notice that the mid-point voltage (blue curve) switches between 300V DC^+ voltage and 0V DC^- voltage. A zoom into the dynamic phases allows the identification of the different commutation sequences. At IGBT turn-on, one can notice the diode reverse recovery current (red curve). The mid-point voltage is at about 0V. At IGBT turn-off, the mid-point voltage switches back to 300V. These waveforms are similar to those of the classical boost cell and allow to validate the operating modes of the monolithic boost switching cell.



(a)

(b)

Fig.7. (a) Current and voltage waveforms within a commutation cycle of the boost cell and (b) zoom into the dynamic phases of commutation.

Basic buck switching cell

The buck cell is also simulated in a chopper circuit. Fig.8 shows the simulation results for the IGBT mode and Fig.9 simulation results for diode mode. In IGBT mode, one can notice that the current flowlines flow from the anode electrode (frontside) towards the midpoint in the backside. The space charge region in the left-side section shows that the diode section is reverse biased and supports the applied voltage. This space charge region corresponds to the reverse biasing of the junction P–drift

/N+(wall). For the diode mode (Fig.9), the current flowlines flow from the anode electrode (frontside) towards the midpoint in the backside. The applied voltage is supported by the IGBT section.

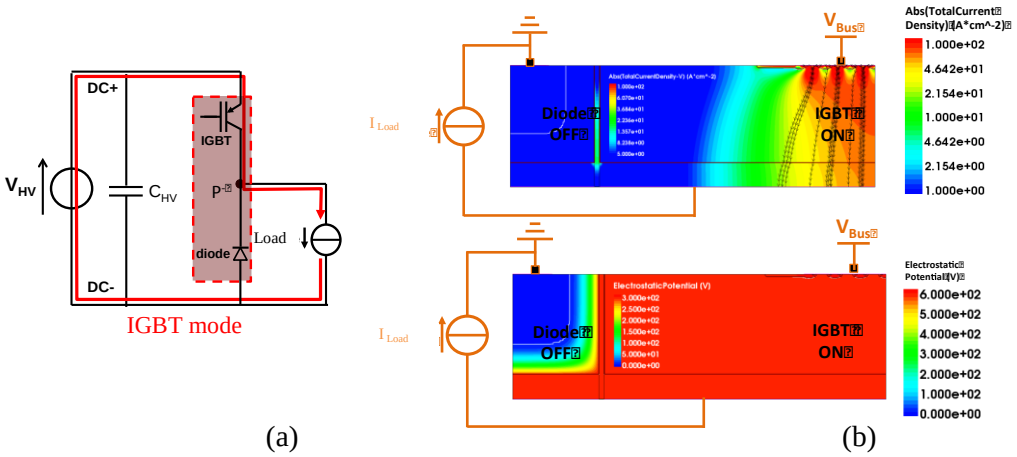


Fig. 8. (a) IGBT mode of the buck cell, (b) current density and equipotential lines in IGBT mode.

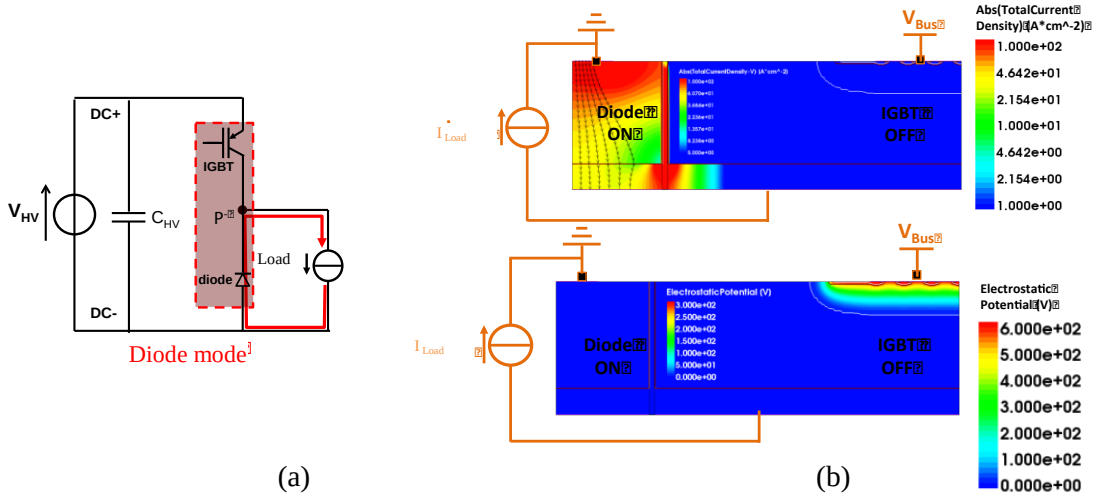
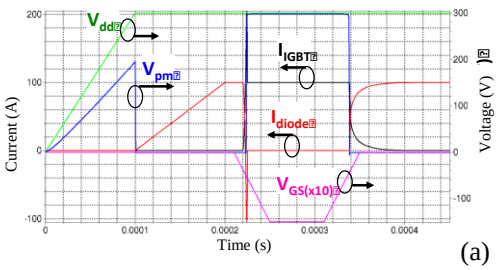
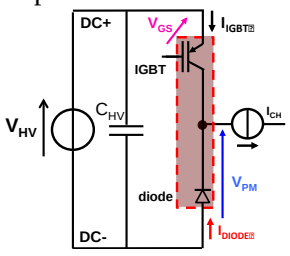
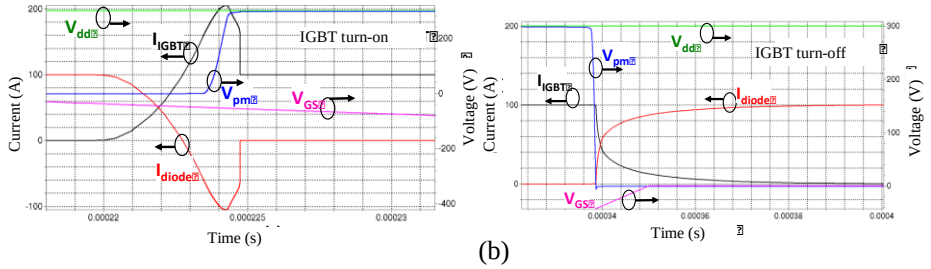


Fig. 9. (a) Diode mode of the buck cell, (b) current density and equipotential lines in diode mode.

Fig.10 shows voltage and current waveforms in the buck cell during one switching cycle. A zoom into the dynamic phases given in Fig. 10(b) allows a better analysis of the commutation sequences. At IGBT turn-on, one can notice the diode reverse recovery current (red curve) and the mid-point voltage switches from DC- voltage (about 0V) to DC+ voltage (about 300V). At IGBT turn-off, the mid-point switches back to DC- voltage (about 0V). These waveforms are similar to those of the classical buck cell and allow to validate the operating modes of the monolithic buck switching cell. The comparison of the diodes post-recovery current waveforms of Fig. 8(b) and Fig.10(b) show that the P-diode post-recovery current is more abrupt than that of the N-diode. Additional 2D simulations will be carried-out in order to confirm this difference. Practically, the snappy recovery is a source of overvoltage across the diode and EMI. Solutions based on a snubber circuit or a clamp placed in parallel with the diode can be used. The control of the converter in ZVS mode also permits to overcome these problems.







(b)

Fig. 10. (a) Current and voltage waveforms within a commutation cycle of the buck cell and (b) zoom into the dynamic phases of commutation.

Association of the elementary cells in an inverter phase leg

The functionality of the phase leg inverter is obtained by associating the two elementary complementary cells as shown in Fig. 11.

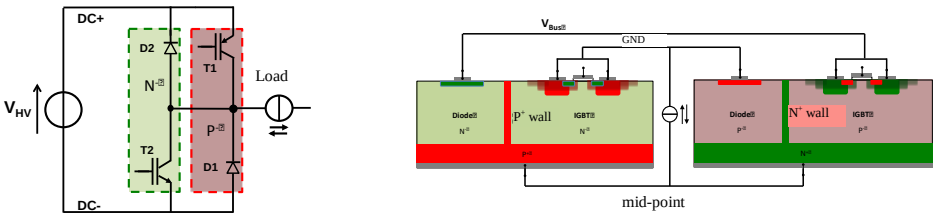
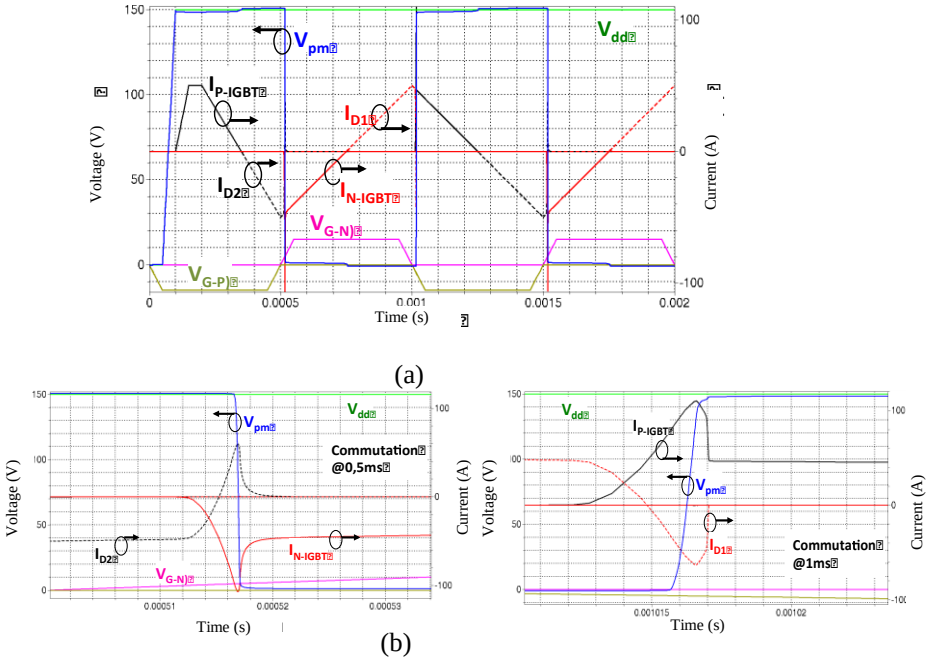


Fig. 11. Association of the two chips to form a phase-leg.

The phase leg's voltage and current waveforms are given in Fig. 12. As a first example, a triangular current source is used. The switching cells commutation takes place at maximum current. On the red and black curves, one can recognize the conduction phases of the different components. When the high-side is driven (mid-point voltage Vpm at DC^{+}), the current flows either through the P-IGBT or through the diode D2, depending upon the current source direction. When the low-side part is driven (mid-point voltage Vpm at DC-), the current flows either through the N-IGBT or through the diode D1. Fig. 12(b) shows in details the current and voltage waveforms during the commutation phases at 0.5 ms and 1 ms, respectively.



(a)

(b)

Fig. 12. (a) Current and voltage waveforms within an inverter phase-leg and (b) zoom into the dynamic phases of commutation.

Conclusion

In this paper, a concept of asymmetric monolithic switching cell integration is presented and validated by 2D physical simulations. The concept relies on the integration of the inverter phase-leg on two complementary chips, in which each chip integrates a monolithic switching cell. The first chip integrates *the buck* cell within a p-wafer while the second chip integrates *the boost* cell in an N-wafer. The operating modes of each cell were first validated separately and then associated in a phase-leg's inverter application. This is the ultimate monolithic wire-bondless switching cell that allows to suppress the wirebonds within the switching cell and therefore minimizes the stray inductance value. Consequently, it is suited for the emerging applications requiring to achieve simultaneously: reliability, compactness, intrinsic performance and reduced manufacturing cost.

References

[1] S. Tanimoto and K. Matsui: High junction temperature and low parasitic inductance power module technology for compact power conversion systems, IEEE Trans. Electron Devices, vol. 62, no. 2, pp. 258–269, Feb. 2015.

[2] Shengnan Li; Tolbert, L.M.; Fei Wang; Fang Zheng Peng: Stray Inductance Reduction of Commutation Loop in the P-cell and N-cell-Based IGBT Phase Leg Module, Power Electronics, IEEE Transactions on , vol.29, no.7, pp.3616-3624, July 2014.

[3] D.W Green, E.M Shankar Narayanan: Fully Isolated High Side and Low Side LIGBTs in Junction Isolation Technology, Power Semiconductor Devices and IC's, ISPSD 2006. IEEE International Symposium on, pp.1-4, 2006.

[4] L. Benaissa et al. :A vertical power device conductive assembly at wafer level using direct bonding technology, in Proc. IEEE 24th Int. Symp. Power Semiconductor Devices ICs , Jun. 2012, pp. 77–80

[5] A. El Khadiry, A. Bourennane and F. Richardeau: Multiphase Power Converter Integration in Si: Dual-Chip and Ultimate Monolithic Integrations, in IEEE Transactions on Electron Devices, vol. 63, no. 5, pp. 1977-1983, May 2016.

[6] Bourenanne Abdelhakim, Richardeau Frédéric, Lale Adem: Multi-pole power chip(s) with monolithic integration of asymmetric chopper cells and multi-phase power module(s) using the or a plurality of said multi-pole chips, Priority number FR20160063038 20161221, Demand number WO2017EP83435 20171219, 2018-06-28.

[7] Lale, A. Bourennane and F. Richardeau: Monolithic Complementary Multi-terminal RC-IGBT Chips for Compact Multi-phase Power Converter, 2018 25th International Conference "Mixed Design of Integrated Circuits and System" (MIXDES), Gdynia, 2018, pp. 333-337.

[8] Adem Lale, Abdelhakim Bourennane, Frédéric Richardeau, Tahir Hakim: Realization of a monolithic multi-terminal Si-power chip integrating a 2-phase rectifier composed of vertical PiN diodes insulated by vertical P+ walls, European Power Electronics Conference septembre 2018, Latvia.

[9] A. Lale, N. Videau, A. Bourennane, F. Richardeau and S. Charlot: Mixed monolithic-hybrid integration of multiphase power converter : Preliminary evaluation of the 3-chip integration concept, 2016 International Conference on Electrical Systems for Aircraft, Railway, Ship Propulsion and Road Vehicles & International Transportation Electrification Conference (ESARS-ITEC), Toulouse, pp. 1-7.