

Aging and failure mechanisms of SiC Power MOSFETs under repetitive short-circuit pulses of different duration

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With relevance to their short-circuit (SC) failure mode, silicon carbide (SiC) power MOSFETs can be broadly grouped into two main categories: Fail-To-Open (FTO) and Fail-To-Short (FTS). The two different behaviors are exemplified in the results of Fig. 1 a): the former involves a short circuit between the gate and source terminals, which effectively shuts-down the device; the latter features current thermal runaway and collapse of the drain-source voltage, V_{DS} . The specific failure signature is extremely relevant from an application perspective, with a clear preference for FTO type devices, since FTS has the twofold negative implication of discharging any energy storage components (e.g., capacitors) connected to the switches, with oftentimes explosion-like characteristics, and of loss of functionality of a whole module in the case of parallel multi-chip architectures. A study conducted on a number of 1.2 kV-rated commercial devices has produced the results summarized in Fig. 1 b): only one device type has been identified, which consistently guarantees SC FTO behavior for V_{DS} values up to 50% of its rated voltage [1]. Because of its application interest, this particular device was studied here in detail, under different damage accumulation conditions.

As is clear from the discussion above, the gate leakage current, $I_{G,LEAK}$, is a valuable monitor of degradation and failure. Previous papers reported no permanent damage and aging in the devices for pulse widths below the minimum required to reach a critical value of $I_{G,LEAK}$ [2]. So, here, our first test was to determine such critical pulse-width value, $t_{PW,CRIT}$ for the device under test. The results of Fig. 2 show: the SC drain current, a); the gate-source voltage, V_{GS} , b); $I_{G,LEAK}$, c), for the device subjected to pulses of different duration, all with $V_{DS}=600$ V. $I_{G,LEAK}$ shows the onset of an exponential type rise starting from about 10 μ s, which was thus retained here as the reference $t_{PW,CRIT}$ value. In a subsequent experiment run, the pulse width was then nearly halved and repetitive stress was applied until degradation was observed. As shown in Fig. 3 a), after some thousand pulses, degradation of the saturation conduction characteristics is manifest; however, it could not be related to any degradation at gate level, as Figs. 3 b) and c) clearly indicate (also additional measurements of the transfer characteristics at various intervals, not reported here, have indicated no change). If the SC pulse width is increased to values around $t_{PW,CRIT}$ the results, Fig. 4, are quite different: degradation of the drain current, a), is still highlighted, however, in this case, it can be related with very clear degradation of the gate-structure, too, as clearly illustrated by the results of b) and c). It must also be noted that the device shows clear capability to withstand in excess of 1000 pulses with SC pulse-width of 10 μ s when 50% of the rated voltage is applied, that is, to satisfy the common basis requirement applied to IGBTs of similar voltage rating even if the gate is degraded.

So, the interpretation is put forward that two different failure mechanisms are at play depending on the SC pulse width: for "short" pulses, only a reduction of the saturation current is involved (type 1 degradation), possibly caused by degradation of the chip metallization and subsequent de-biasing [3]; for "long" pulses, degradation of the gate structure is evident (type 2 degradation), possibly caused by cracks around the inter-layer dielectric (ILD) triggered by the high difference in thermal expansion between the top Al and the SiO₂ and formation of a metallic paths in the gate-source ILD caused by the top Al melting [1] at the edge of the chip during the short-circuit as presented in Fig. 5 a). This last hypothesis is substantiated by additional measurements of the transfer characteristics at various moments of the stress campaign: as can be seen in Fig. 5 a), instability/recovery is manifest on degraded devices as a function of applied V_{GS} for degradation Type2, which can be ascribed to local metallic path leading to a local short-circuit gate-source that only turn-off a part of the chip. Injecting a high current into the gate is supposed to fuse the metallic path leading to the device recovery as observed in Fig. 5 b) at #2500. Further ongoing functional and structural tests are aiming to produce a conclusive interpretation of the two distinct failure mechanisms detected.

[1] F. Boige et al., *Ensure an original and safe "Fail-to-Open" mode in SiCMOSFET devices in extreme short-circuit operation*, *Microelectronics Reliability* (88–90) 2018, 598–603.

[2] C. Chen et al., *Study of short-circuit robustness of SiC MOSFETs, analysis of the failure modes and comparison with BJTs*, *Microelectronics Reliability* 55 (2015) 1708–1713

[3] V. Smet et al., *'Ageing and Failure Modes of IGBT Modules in High-Temperature Power Cycling'*, *IEEE Trans. on Ind. Electr.*, vol. 58, no. 10, pp. 4931–4941, Oct. 2011.

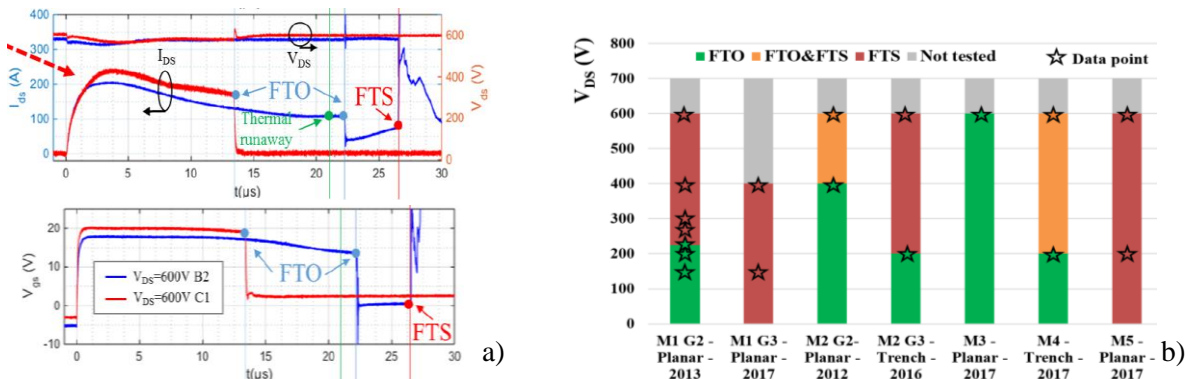


Fig. 1. Short-circuit drain current, I_D , and drain-source voltage, V_{DS} , (top) and gate-source voltage V_{GS} (bottom), a); summary of SC failure mode (FTO or FTS) for different commercial devices at different V_{DS} values, b) [1].

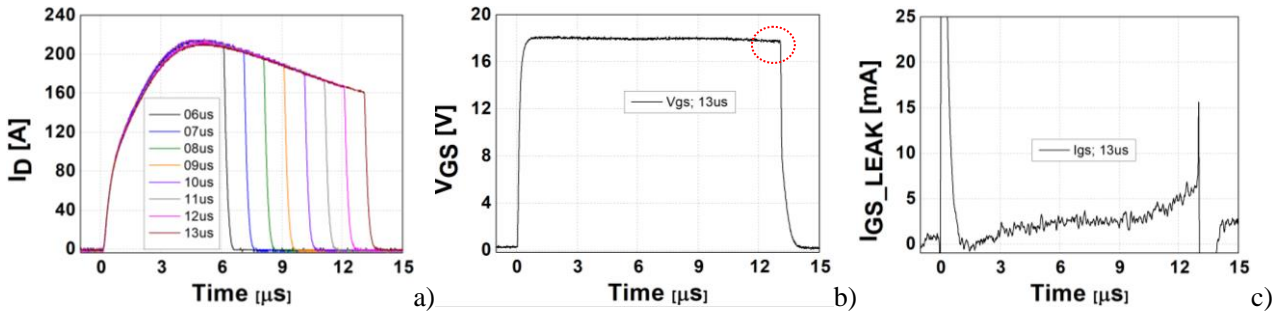


Fig. 2. Experimental results for SC tests with varying pulse durations: I_D , a); V_{GS} , b); $I_{G,LEAK}$, c). A drop in V_{GS} is noticeable (circle) from about 10 μs , at which moment $I_{G,LEAK}$ features a steeper increase.

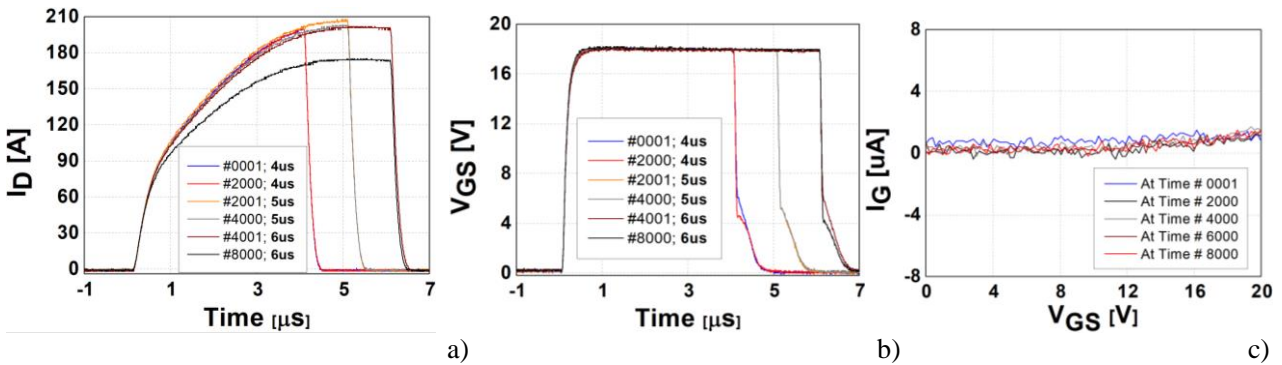


Fig. 3. Experimental results for repetitive SC test with “short” pulse widths: I_D , a); V_{GS} , b); $I_{G,LEAK}$, c)..

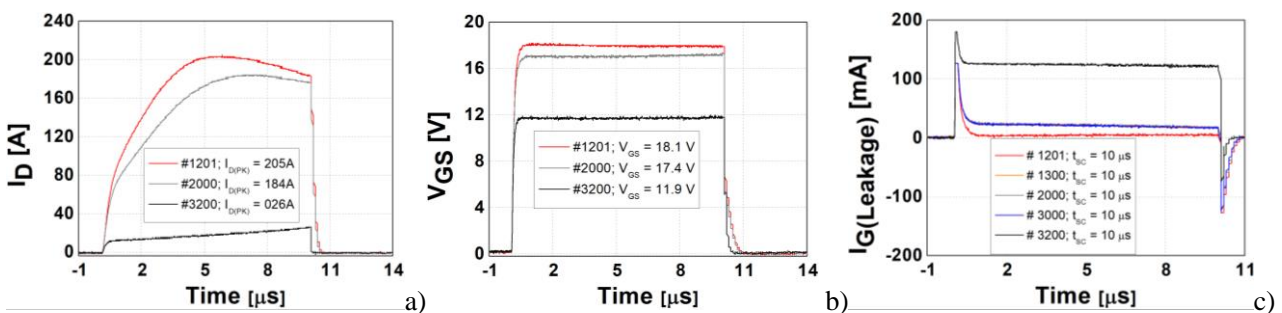


Fig. 4. Experimental results for repetitive SC test with “long” pulse widths: I_D , a); V_{GS} , b); $I_{G,LEAK}$, c).

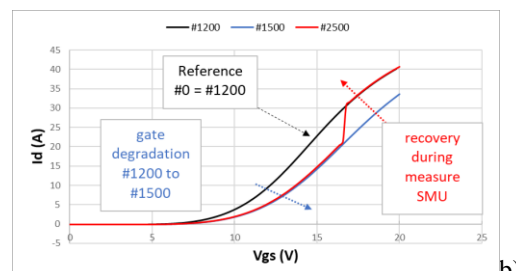
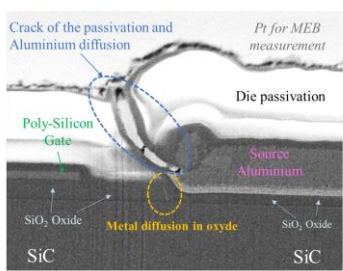


Fig. 5. a) MEB image of a FIB microsection on device M3 after destructive test presented Fig. 1. b) $I_D(V_{GS})@V_{DS}=10V$ during repetitive test presented in Fig. 4.