



HAL
open science

Lowering the Dark Count Rate of SPAD Implemented in CMOS FDSOI Technology

T. Chaves de Albuquerque, D. Issartel, R. Clerc, P. Pittet, R. Cellier, F. Calmon

► To cite this version:

T. Chaves de Albuquerque, D. Issartel, R. Clerc, P. Pittet, R. Cellier, et al.. Lowering the Dark Count Rate of SPAD Implemented in CMOS FDSOI Technology. EUROSOI ULIS 2019, Apr 2019, Grenoble, France. 10.1109/EUROSOI-ULIS45800.2019.9041916 . hal-02333580

HAL Id: hal-02333580

<https://hal.science/hal-02333580v1>

Submitted on 25 Oct 2019

HAL is a multi-disciplinary open access archive for the deposit and dissemination of scientific research documents, whether they are published or not. The documents may come from teaching and research institutions in France or abroad, or from public or private research centers.

L'archive ouverte pluridisciplinaire **HAL**, est destinée au dépôt et à la diffusion de documents scientifiques de niveau recherche, publiés ou non, émanant des établissements d'enseignement et de recherche français ou étrangers, des laboratoires publics ou privés.

Lowering the Dark Count Rate of SPAD Implemented in CMOS FDSOI Technology

T. Chaves de Albuquerque^{1*}, D. Issartel¹, R. Clerc², P. Pittet¹, R. Cellier¹, F. Calmon¹

¹ INL - Institut des Nanotechnologies de Lyon, UMR CNRS 5270, Université de Lyon, France

² LabHC - Laboratoire Hubert Curien, UMR CNRS 5516, Université Jean Monnet, Saint Etienne, France

Email: {tulio.chaves-de-albuquerque, francis.calmon}@insa-lyon.fr

Abstract—This article presents an optimization study aiming at decreasing the Dark Count Rate (DCR) of Single Photon Avalanche Diodes implemented in CMOS Fully Depleted Silicon-On-Insulator technology presenting initially a low breakdown voltage and therefore an excess of band-to-band tunneling generation rate, leading to high DCR. It can nevertheless decrease by 5 decades with a single implant modification in the fabrication process.

Keywords-SPAD; CMOS FDSOI; DCR; TCAD simulation

I. INTRODUCTION

Consumer market applications linked to IoT require the development of photodetectors embedded in CMOS circuitry for facial recognition, camera autofocus etc. In the near infrared (NIR) range, Single Photon Avalanche Diodes (SPAD) have already demonstrated their capacity to answer most of the requirements in terms of performances such as response time and sensibility even if their External Quantum Efficiency (EQE) is rather low for NIR light. The integration of SPAD in CMOS technology is addressed in two ways: planar device [1] or 3D integration with wafer-to-wafer stacking [2]. The second approach allows higher fill-factor with dedicated technology at each level. Then the top die holds the SPAD array with a backside illumination (BSI) and the CMOS bottom die contains all the signal processing, quenching etc. An alternative way is explored based on advanced CMOS Fully Depleted Silicon-On-Insulator (FDSOI) technology [3]. The SPAD is implemented below the buried oxide (BOX) while the transistors are placed in the usual thin silicon layer, as shown in Fig. 1. This SPAD architecture is then intrinsically 3D as the logic is placed above the SPAD (with BSI after die thinning).

II. PRELIMINARY RESULTS AND OBJECTIVE

In [3], authors presented the first experimental results on a SPAD fabricated in STMicroelectronics' CMOS FDSOI 28nm technology without any design rule violation nor process customization. The diode was implemented with P-well and deep N-well layers which are conventionally intended for transistor back-biasing. This kind of architecture actually provides an intrinsically 3D stacking with expected benefits such as a much higher fill factor. A quite low SPAD breakdown voltage $V_{BD} \approx 9.6V$ was

obtained at room temperature due to the abrupt junction resulting from the CMOS FDSOI technology doping profiles (also reproducible in TCAD). Consequently, a low activation energy, that is the signature of the band-to-band and field-enhanced trap assisted tunneling effects, has been extracted from Dark Count Rates (DCR). DCR was of few tens of $Hz/\mu m^2$ at room temperature at 0.3 V excess bias. Even if the SPAD functionality was demonstrated with this first prototype, the low breakdown voltage limits its operating point to small excess bias voltages. To overcome this limitation and to increase the breakdown voltage, we propose an optimization of the deep N-well doping profile based on TCAD simulations. This solution requires only one implant modification without technology design rule violation.

III. DARK COUNT RATE OPTIMIZATION BASED ON DEEP N-WELL DOPING PROFILE MODIFICATION

A. Modified SPAD Cell

We modified in TCAD simulations the implantation parameters of the deep N-well (energy and dose) in order to get a smoother P-N junction and thus a higher breakdown voltage $V_{BD} \approx 16V$. This parametric optimization was based on a single implantation step for the deep N-well, while it is conventionally obtained with two implants. We found that this single implantation

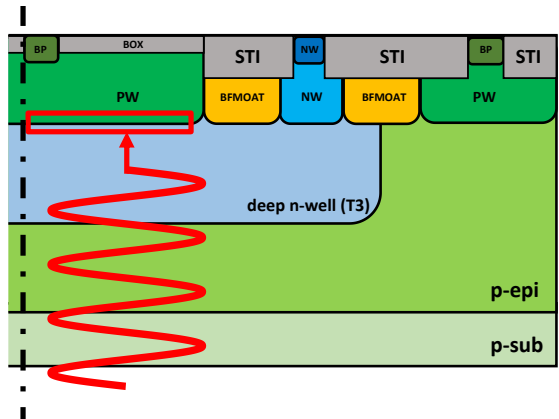


Figure 1. Schematic of SPAD implementation in CMOS FDSOI technology below the buried oxide (half-cell with axial symmetry), scales are not respected [3]

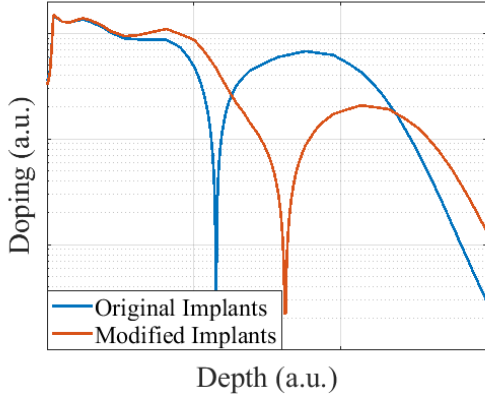


Figure 2. Original and modified net-doping profiles

should be done at a 25% higher energy as compared to the value at second implant used in commercial process.

Original and optimized net-doping profiles are shown in Fig. 2 (we use arbitrary scales for confidentiality purposes). The metallurgical junction is shifted at greater depth, and the optimized deep N-well is about three times less doped than the original one. It results in a junction breakdown voltage increase of $\sim 65\%$.

B. Dark Count Rate Simulation

The dark count rate was estimated thanks to data from TCAD simulations coupled to external routine. From the ionization coefficients, we calculated the avalanche triggering probability P_{tr} [4], then we integrated the product of the band-to-band (B2B) tunneling generation rates (Schenk model) by the probability P_{tr} to evaluate the DCR:

$$DCR = \int P_{tr}(x)G_{B2B}(x)dx \quad (1)$$

The maximum values of B2B generation rates with original and optimized doping profiles are shown in Fig. 3, for different excess voltages. The optimization of the implant in deep N-well produced a reduction of 5 decades in B2B tunneling generation rate. This allows a significant DCR decrease as it is shown in Fig. 4 for different excess bias voltages. An experimental point acquired on the first prototype (original doping profile) is also plotted for comparison. It is consistent with TCAD simulation results. However, it was not possible to acquire additional experimental data at higher biasing voltages, since the DCR is adversely impacted by afterpulsing events for such operating points [3].

IV. CONCLUSION

As previously reported, SPAD behavior can be observed in standard CMOS FDSOI 28nm technology, while using the diode composed by P-well and deep N-well junction biased in Geiger-mode. Nevertheless, breakdown voltage is low, and band-to-band generation rate is high, due to the junction abruptness. The present study proves, by means of TCAD simulations, that a simple implant modification in the whole standard fabrication process allows

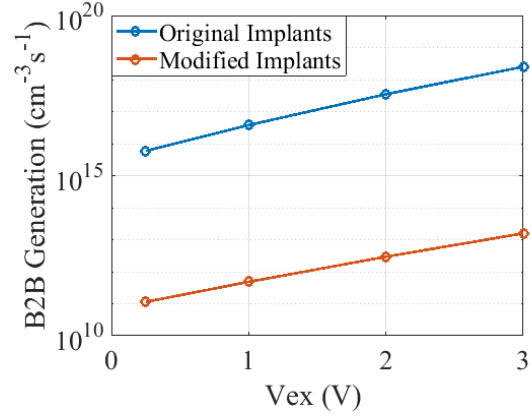


Figure 3. B2B generation rates (before and after implant modification)

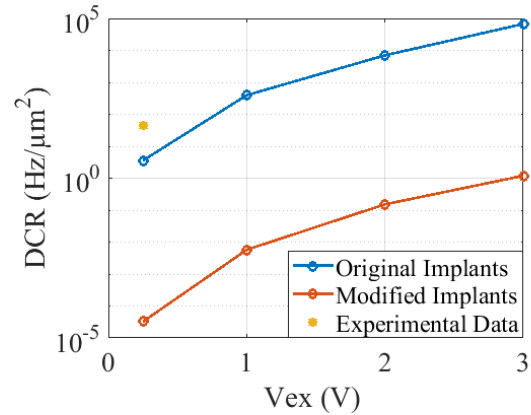


Figure 4. Simulated dark count rates (before and after)

drastically reducing the B2B generation rate ($/10^5$) and consequently the dark count rate, improving SPAD performances. Future work will address the characterization of new samples with the proposed modified process.

ACKNOWLEDGMENT

The authors would like to thank the French national research agency ANR, the Auvergne-Rhone-Alpes region, IngéLySE federation for fundings, and also STMicroelectronics, CMP for IC prototyping facility.

REFERENCES

- [1] S. Pellegrini et al. "Industrialised SPAD in 40 nm Technology," International Electron Devices Meeting (IEDM), pp. 16.5.1-16.5.4, 2017.
- [2] S. Lindner et al. "A High-PDE, Backside-Illuminated SPAD in 65/40 nm 3D IC CMOS Pixel with Cascoded Passive Quenching and Active Recharge," IEEE Electron Device Letters, vol. 38, no.11, pp. 1547-1550, 2017.
- [3] T. Chaves De Albuquerque, et al. "Integration of SPAD in 28nm FDSOI CMOS technology." 2018 48th European Solid-State Device Research Conference (ESSDERC), pp. 82-85, 2018.
- [4] R.J. McIntyre, "On the avalanche initiation probability of avalanche diodes above the breakdown voltage." IEEE Transactions on Electron Devices 20.7, 637-641, 1973.