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Gwenaëlle Hamon, Nicolas Vaissière, Clément Lausecker, Romain Cariou, Wanghua Chen, et al.. Heteroepitaxial growth of silicon on GaAs via low-temperature plasma-enhanced chemical vapor deposition. SPIE OPTO : Quantum Sensing and Nano Electronics and Photonics XVI, SPIE PHOTONIC WEST, Feb 2019, San Francisco, United States. 10.1117/12.2511174 . hal-02331842

HAL Id: hal-02331842
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Event: SPIE OPTO, 2019, San Francisco, California, United States

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Heteroepitaxial growth of Silicon on GaAs via low temperature plasma-enhanced chemical vapor deposition

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ABSTRACT

We present an innovative approach for the growth of crystalline silicon on GaAs using plasma-enhanced chemical vapor deposition (PECVD). In this process the substrate is kept at low temperature (175 °C) and epitaxial growth is obtained via the impact of charged silicon clusters which are accelerated towards the substrate by the plasma-potential and melt upon impact. Therefore, this is a nanometer size epitaxial process where the local temperature (nm scale) rises above the melting temperature of silicon for extremely short times (in the range from ps to ns). This allows obtaining epitaxial growth even on relatively rough GaAs films, which have been cleaned in-situ using a SiF_4 plasma etching. We present in-plane X-Ray Diffraction (XRD) measurements which are consistent with the hypothesis that the epitaxial growth happens at a local high temperature. Indeed, the tetragonal structure observed and the low in-plane lattice parameter determined from XRD can only be explained by the thermal mismatch induced by a high growth temperature. The effect of the plasma on the underlying GaAs properties, in particular the formation of hydrogen complexes with GaAs dopants (C, Si, Te) is studied in view of the integration of the c-Si epi-layers into devices.

Keywords: low temperature plasma epitaxy, integration of silicon on III-V, heteroepitaxy, charged clusters, tetragonal silicon

1. INTRODUCTION

Integration of III-V materials on silicon has been extensively studied over the past thirty years because it would allow combining the current microelectronics industry based on c-Si, with the optoelectronics industry based on III-V materials. Indeed, the indirect bandgap of c-Si makes of this material a poor light emitter compared to III-Vs. Therefore optical interconnects have been developed in order to increase the speed of current processors, but the integration of a light source based on III-V materials directly into a c-Si platform is still challenging[1]. The growth of III-V materials is usually performed at high temperature and/or ultra-high vacuum conditions using Metalorganic Vapor Phase Epitaxy (MOVPE) or Molecular Bean Epitaxy (MBE) techniques. However, this process poses various challenges: i) Polarity: the growth of GaAs, a polar material, on c-Si which is non polar introduces strain at the interface and results in defects[2]. ii) Lattice mismatch: the lattice parameter of GaAs (5,6533 Å) is about 4% higher than that of c-Si (5,4307 Å) and therefore a GaAs film grown on c-Si is submitted to a strong compressive strain which will relax by creating threading dislocations after some critical thickness. iii) Thermal mismatch: the thermal expansion coefficient of GaAs (5,76. 10^{-6} K^{-1}) being higher than that of c-Si (2,7. 10^{-6} K^{-1}), the GaAs film grown at high temperature on a c-Si substrate will experience a tensile strain, which can also result into defects and crack formation when cooling down the sample from the growth temperature down to room temperature. As a consequence, epitaxial growth of III-V on c-Si and the integration of the two technologies on the same platform remain challenging. In this paper we present a new approach to succeed such integration, namely the epitaxial growth of silicon on GaAs.

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Quantum Sensing and Nano Electronics and Photonics XVI, edited by Manijeh Razeghi, Proc. of SPIE
Vol. 10926, 109261C · © 2019 SPIE · CCC code: 0277-786X/19/$18 · doi: 10.1117/12.2511174

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In the case of PECVD epitaxy of Si on GaAs the challenge about polarity is released as silicon is a non-polar material. Moreover, PECVD allows to grow epitaxial layers at a very low "nominal substrate temperature" of 175 °C and therefore the thermal mismatch issues can be minimized when cooling down from the growth temperature to room temperature. Of course, lattice mismatch will always be present, no matter the order of deposition; however the fact that epitaxy is taking place at nanometer scale can reduce the strain as it happens in the case of nanowire growth[3]. Thus, low temperature PECVD may allow an easier integration of Si on III-V compared to the widely studied integration of III-V on Si. Moreover, as shown below, growing Si on GaAs also helped us to better understand the growth mechanism of crystalline silicon by PECVD, because it allows separating the effect of thermal expansion mismatch and lattice parameter mismatch. However, the new process can also lead to unexpected effects related to the exposure of III-V materials to the aggressive PECVD environment. In particular, ion bombardment and the presence of abundant atomic hydrogen are known to disrupt epitaxy and to form complexes with dopant atoms in GaAs. In this paper we present a comprehensive summary of our work on the topic and provide new results that allow explaining the epitaxial growth by PECVD at such low nominal substrate temperatures.

2. EXPERIMENTS

Epitaxial growth of silicon was carried out in a standard PECVD reactor[4] at a substrate temperature of 175 °C. Moreover, the GaAs substrates have been cleaned in-situ using a SiF_4 plasma treatment, whose conditions have been optimized using in-situ ellipsometry measurements[5]. As a fast characterization of the epitaxial quality, spectroscopic UV-visible ellipsometry measurements were carried out and from the analysis of the data we determined the films thickness and composition using Bruggeman Effective Medium Approximation model[6]. Moreover, Raman scattering was used to determine the crystallinity of the films and their degree of disorder from the full width at half maximum of the TO phonon mode[5]. AFM measurements were used to characterize the surface of the GaAs substrates prior to epitaxial growth. We investigated the first stages of the growth of crystalline silicon on top of GaAs, by using in-plane X-Ray diffraction. To do so, the beamline DiffAbs from SOLEIL synchrotron was used[7]. The experimental station consists of a six-circle diffractometer. Four circles are used to orient the sample and two circles are used for XRD measurements in the vertical and horizontal plane. The geometry of this diffractometer enables not only to probe the {004} planes in high angle ω-2θ configuration, with a X-ray beam size around 8x10µm², but also in $2\theta_\chi$-ϕ in-plane configuration. The ω-2θ configuration gives information on the out-of-plane lattice parameter $a_\perp$. The second configuration, Grazing Incidence X-Ray Diffraction (GIXRD) performs $2\theta_\chi$-ϕ scans which probe the {220} planes, perpendicular to the (100) surface. It gives information on the in-plane lattice parameters $a_{//}$. We consider that the parameters along both x and y directions are identical.

3. RESULTS AND DISCUSSION

3.1 Plasma cleaning of the GaAs substrate

In order to remove the native oxide and clean the surface of the GaAs substrate it is not possible to use standard high temperature anneal as currently done in MOVPE or MBE processes. Indeed, the substrate temperature is limited to 300 °C in our PECVD reactor[4]. Therefore, we have developed in-situ plasma cleaning processes for c-Si and GaAs substrates based on the exposure of the wafers to a SiF_4 plasma which can etch the surface of the wafer. This cleaning combines physical processes (ion bombardment) and the etching effect of fluorine atoms to provide a "clean" surface. The optimization of the process has been carried out using in-situ spectroscopic ellipsometry which allows monitoring the evolution of the amplitude of the peak at 4.4 eV of the imaginary part of the pseudo-dielectric function of GaAs. As previously reported[5], the optimization of the SiF_4 plasma etching conditions (pressure, RF power, SiF_4 flow rate) and the etching time permits to determine the optimal treatment required to remove the oxide without introducing an excessive roughness of the GaAs surface. However, as shown by the AFM images in Figure 1, the SiF_4 plasma treatment introduces an increase in the surface roughness compared to that of the GaAs substrate coated with a thin GaAs layer epitaxially grown by MOVPE. Indeed, while atomic terraces can be distinguished in the MOVPE grown thin film, the plasma treatment for 2 minutes at 175° C under an RF power of 30 watts under SiF_4 pressure of 90 mTorr results in an increase of the roughness from 0.24 nm up to 0.4 nm. This is in clear contrast with the standard high temperature cleaning performed in MOVPE growth, in which case the surface has to be atomically flat.

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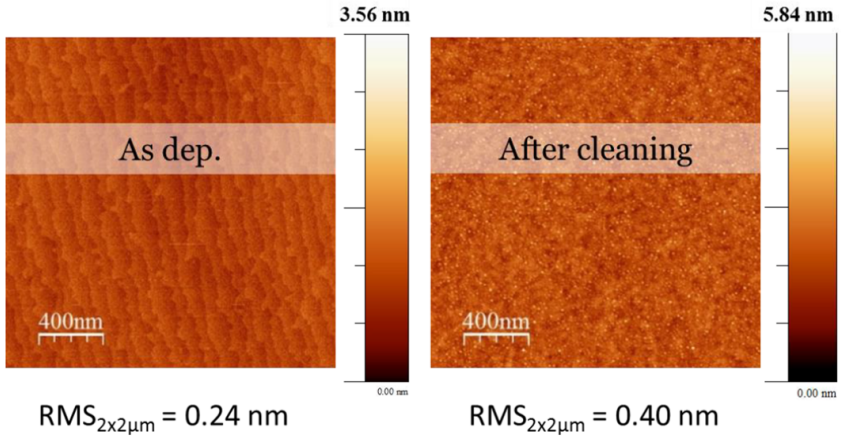

Figure 1. AFM images on a MOVPE GaAs layer epitaxially grown on a GaAs substrate where atomically flat terraces can be distinguished. After the SiF_4 plasma cleaning, the roughness increases and the terraces cannot be distinguished anymore.

3.2 PECVD growth of c-Si on GaAs

Epitaxial growth of c-Si by PECVD has been reported to take place under conditions of hydrogenated polymorphous silicon deposition on glass, i.e. when silicon clusters are produced in the plasma and contribute to deposition[6]. Figure 2 shows the effect of the silane flow rate on the deposition rate and properties of silicon thin films produced at 175 °C, under a total pressure of 2000 mTorr an RF power of 20 mW/cm^2 and a H_2 flow rate of 500 sccm. At low silane flow rate, corresponding to a high dilution in hydrogen, the films are microcrystalline, as can be deduced from the low value of the amplitude of the imaginary part of the pseudo-dielectric function (ε_i), and the large value of the full width at half maximum (FWHM) of the TO Raman mode at 520 cm^{-1}. As the silane flow rate increases, gas phase reactions take place and lead to the formation of silicon clusters which can be positively charged and contribute to the growth with an impact energy corresponding to the plasma potential. After a critical value of 35 sccm (for the given process conditions), the plasma turns into the powder regime where the clusters agglomerate and form large powders rather than contributing to film deposition. This results in a decrease of the deposition rate and the change of the produced films from epitaxial to standard hydrogenated amorphous silicon (a-Si:H). Interestingly, the trends concerning the properties of the films deposited on GaAs (Figure 2) are the same as those previously reported for the homoepitaxy of silicon film of c-Si substrates[6], i.e. epitaxy by PECVD is quite independent of the substrate.

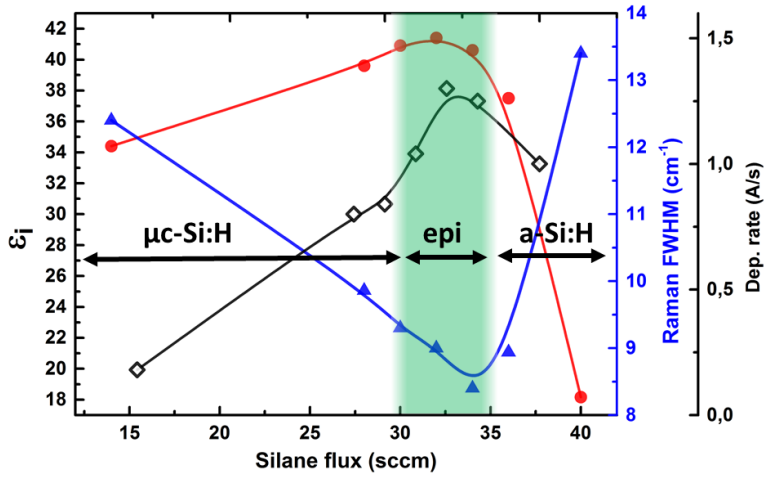

Figure 2. Effect of the silane flow rate on i) the amplitude of the imaginary part of the pseudo-dielectric function (red circles), ii) the full width at half maximum of the TO peak at 520 cm^{-1} (blue triangles), and iii) the growth rate (open diamonds).

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3.3 X-Ray diffraction analysis

In order to better understand the crystalline structure of the epitaxial films and their evolution during growth we deposited by PECVD a series of samples (thicknesses of 7 nm, 12 nm, 20 nm, 43 nm, 53 nm, 100 nm and 1 µm) on GaAs layers previously grown by MOVPE. Grazing incidence X-ray diffraction measurements have been carried out on these samples at the DiffAbs beamline from synchrotron SOLEIL. The geometry of the diffractometer allows to probe the {004} planes in ω-2θ scans, giving access to the out of plane lattice parameter $a_{\perp}$ as well as to the {220] planes from 2θχ scans (grazing incidence), giving access to the in-plane lattice parameter $a_{//}$. For each Si thickness, we performed the measurements in the two configurations. The in-plane and out-of-plane lattice parameters as a function of the Si film thickness are displayed in Figure 3.

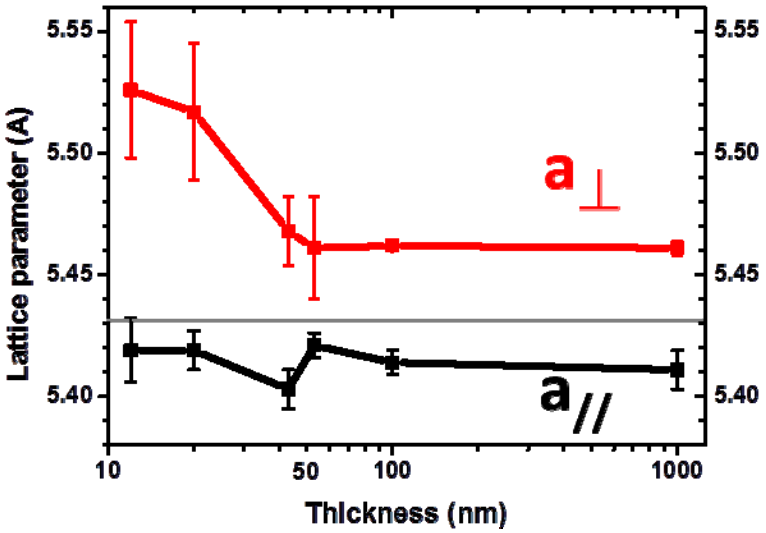

Figure 3. Out-of-plane (red squares) and in-plane (black squares) lattice parameters for c-Si films deposited on GaAs by PECVD at 175 °C. Note that the films are tetragonal, with $a_{\perp} > a_o = 5.4307$ Å $> a_{//}$.

Let us first consider the thickest film (1000 nm); one can see that both lattice parameters are quite different from the lattice parameter of cubic c-Si (a_o= 5.4307 Å) and thus imply that the epitaxial film deposited by PECVD has a tetragonal structure[8]. The larger value of the out-of-plane parameter has been correlated to the incorporation of hydrogen in the films and the fact that this value increases for the thinner films is consistent with a higher concentration of defects and therefore of hydrogen close to the interface with the GaAs substrate[9]. Interestingly, both parameters seem to be independent of the epitaxial layer thickness for thicknesses above 50 nm. Let us note that the 42 nm layer was grown on a GaAs layer highly doped with carbon, which was compressively strained, while all other samples are gown on intrinsic epi-GaAs. This could explain the slight discrepancy in the $a_{//}$ value for this sample. The in-plane lattice parameter is quite independent of the film thickness but smaller than that of cubic c-Si. Two main reasons could lead to a decrease of the in-plane lattice parameter: i) the lattice mismatch between c-Si and GaAs and ii) the difference in thermal expansion coefficient of both materials. If we consider the lattice mismatch, the deposition of c-Si on GaAs ($a_{//c\text{-}Si} < a_{// GaAs}$), should lead to a higher value of the lattice parameter of c-Si (tensile strain), which is opposite to the experimental observation. Thus, the difference in thermal expansion coefficient should be considered. In Figure 4, we plot the evolution of the lattice parameter for c-Si and GaAs according to equation (1).

$$a_{\parallel}(T) = a_{\parallel}(T_0) * (1 + \alpha * \Delta T) \quad (1)$$

If we consider this dependence for both materials, then we obtain the red and black lines shown in Figure 4. Indeed, when a thin film is deposited on a substrate, it follows the thermal expansion of the substrate. Theoretically, if we consider the growth of crystalline Si happening at 175 °C on top of GaAs, then the Si crystal should follow the red dotted line when cooled down to room temperature. Thus, the in-plane parameter should be reduced to the value of 5.4281 Å (open blue circle), as deduced by equation (1). On Figure 4 the value measured by XRD at room temperature of the 53

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nm-thick layer (blue star) is also reported. Assuming that the thin c-Si epitaxial layer follows the thermal expansion imposed by the stiff GaAs substrate, then we can extrapolate the temperature during growth to be around 700 °C, i.e. much higher than the nominal value of 175 °C applied to the substrate. How can we explain this result?

For sure, the average substrate temperature remains low (175 °C), too low to explain the epitaxy by PECVD. However, this result can be explained if we assume that the epitaxial growth occurs via the impact of charged clusters, similarly as in an ionized cluster beam deposition process[10]. The charged clusters are accelerated by the plasma potential, releasing an energy of ~ 1 ev/atom upon impact, which would be enough to account for the epitaxial growth and the low values of the in-plane lattice parameter despite the relatively low average temperature of the substrate. As a matter of fact, the process has been modeled using ab initio molecular dynamics and it has been shown that epitaxy by charged clusters is indeed possible[11]. According to the model, the impact of the clusters can lead to their melting, followed by their thermalization with the substrate in a very short time scale (ns). The fact that the melting is local (nm size of the cluster) allows accommodating the thermal stress and prevents the formation of threading dislocations which takes place in the case of a thin film. This is an important result supporting our hypothesis of epitaxy via charged clusters[6]. Therefore, contrary to MBE and MOVPE, epitaxy in a PECVD environment is possible despite of the contamination of the surface by hydrogen (as well as residual gases present in the PECVD reactor), and the fact that the substrate is not atomically flat but rough.

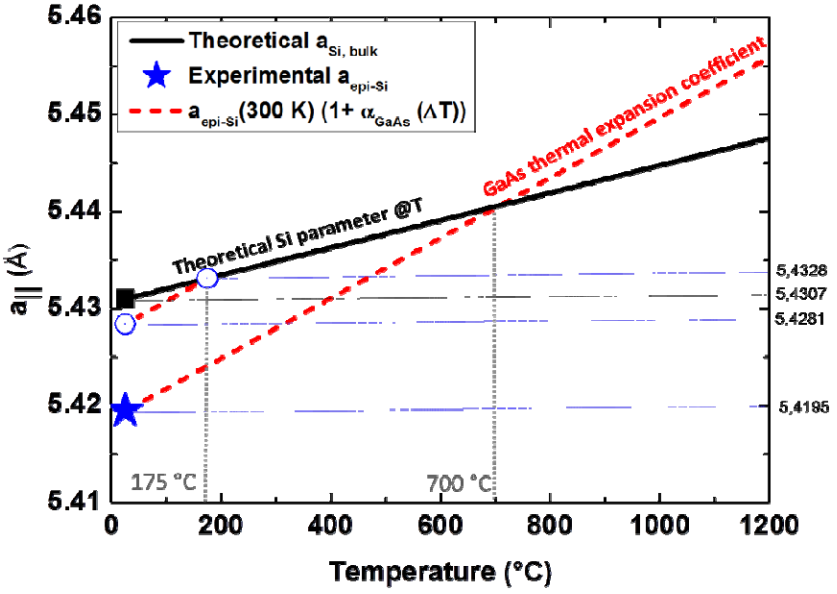

Figure 4. Evolution of $a_{//}$ of a bulk Si as a function of temperature (black) and expected evolution of $a_{//}$ of epi-Si layer that follows the GaAs substrate thermal expansion.

3.4 Impact of the PECVD epitaxy on the GaAs substrate

The above results show that we can obtain epitaxial c-Si films by PECVD at low temperature. The electronic properties of these epitaxial layers deposited on c-Si substrates have been verified by using them as the active layer of heterojunction solar cells[12]. However, for their integration with III-V materials it is necessary to verify that the PECVD growth does not damage the GaAs material. Indeed, the conditions used for the epitaxial growth involve the impact of energetic clusters. Moreover, the PECVD process takes place in a rich hydrogen environment which could also modify the electronic properties of GaAs. To examine the impact of the hydrogen plasma on doped GaAs, several GaAs samples were fabricated on (100) GaAs substrates using MOVPE. For each sample, first a 500 nm-thick intrinsic buffer layer was grown, followed by a 500 nm-thick doped layer. We grew GaAs layers doped with Si, Te (n-type), and C (p-type) with two p-doping levels. The 4 samples and their doping levels are gathered in Table 1.

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Table 1. List of samples grown by MOVPE and their dopants and doping levels

Sample	**A**	**B**	**C**	**D**
Type	p	p	n	n
Dopant	Carbon	Carbon	Silicon	Tellurium
Doping level (cm^{-3})	1×10^{20}	2×10^{18}	1.2×10^{19}	2×10^{19}

Those samples were exposed to very short (30 s for samples A, and B, and 15 s for samples C and D) hydrogen plasmas in our PECVD reactor under the standard conditions of Si epitaxy. To characterize the doping level, ECV measurements were performed before and after hydrogenation. Figure 6.a) shows the resulting carrier concentration profiles before and after H_2 plasma exposure for GaAs:C samples. Figures 6.b) and c) are the ECV profiling before and after plasma exposure for GaAs:Si and GaAs:Te, respectively. On each sample, we notice a strong effect on the doping level at the surface: The doping level has drastically decreased. The doping level in Samples A and B decreases by one order of magnitude at the surface, despite the two orders of magnitude difference in their nominal doping level. For sample A, initially doped at 1×10^{20} cm^{-3}, the 30 seconds hydrogen plasma exposure affected about 20 nm of the layer, while for sample B, initially doped at 2×10^{18} cm^{-3}, the doping level was reduced over a thicker layer (about 100 nm). The thickness over which dopants are neutralized seems to be inversely dependent on the initial dopant concentration. The neutralization of the dopants is attributed to the fact that atomic hydrogen diffuses extremely fast in the GaAs layer and forms complexes with the dopants (here with carbon, thus forming dopant-H complexes) and thus deactivates it. Actually, the shape of the doping profile and the depth of dopant neutralization are quite similar to what Chevallier *et al.*[13] observed in a n-type GaAs doped with silicon. If we look at sample B, the passivated depth is higher than that of sample A that is more doped.

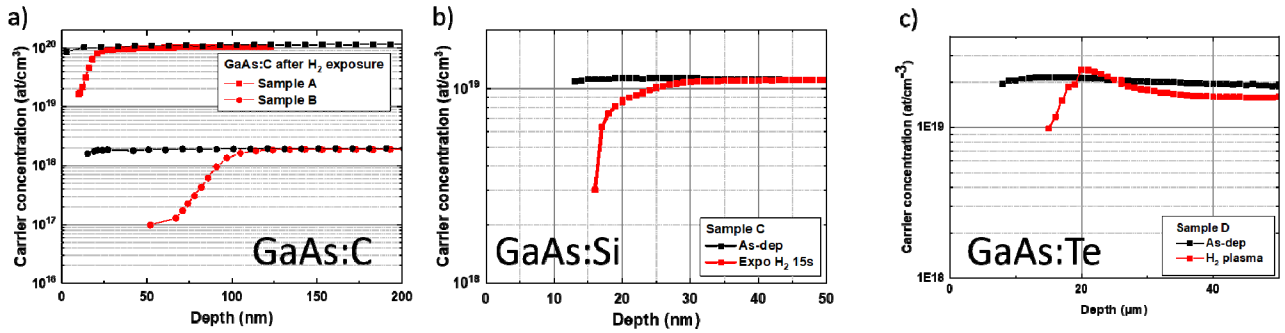

Figure 5. a) Carrier concentration profiles measured by ECV on two p-GaAs:C samples with different initial doping levels, before (black) and after (red) hydrogen plasma exposure. b) and c) Carrier concentration profiles before and after plasma exposure for GaAs:Si and GaAs:Te respectively.

Table 2 summarizes the obtained nominal carrier concentration of the layer and the values measured at the surface of the GaAs after plasma exposure, where **N°** is the nominal carrier concentration, $\mathbf{N}^{H2}$ is the carrier concentration at the surface after plasma exposure and ***d*** is the depth to which the carrier concentration is modified These measurements indicate that the hydrogen plasma that we perform prior to the growth of Si on GaAs affects the doping level of the underlying doped GaAs. This effect is not negligible and must be taken into account in case of integration of c-Ci grown by PECVD on top of a doped GaAs layer. However, this phenomenon can be recovered. Indeed, it has been showed that this loss in doping level can be recovered after rapid thermal annealing at 350 °C for 3 minutes[14].

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Table 2. Doping levels and penetration depth after H_2 plasma exposure.

	Sample A	**Sample B**	**Sample C**	**Sample D**
Dopant	C	C	Si	Te
H_2 exposure	30 s	30 s	15 s	15 s
***N*° (cm^{-3})**	1×10^{20}	2×10^{18}	1.2×10^{19}	2×10^{19}
***N^{H2}*(cm^{-3})**	1.5×10^{19}	1×10^{17}	3×10^{18}	9.5×10^{18}
***d* (nm)**	20	100	15	10

4. SUMMARY AND PERSPECTIVES

We have presented a low temperature epitaxial growth process for the integration of silicon and III-V technologies that overcomes the usual difficulties encountered when trying to integrate III-V materials on c-Si. Indeed, by reversing the deposition sequence, i.e. by growing epitaxial silicon on GaAs at 175 °C by plasma-enhanced chemical vapor deposition, we can release the polarity and thermal mismatch issues. Moreover, thanks to X-Ray diffraction measurements we have shown that the structure of the epi-Si films is tetragonal, with an in-plane lattice parameter smaller than that of cubic silicon, suggesting that the material has experienced a strong thermal stress. This result is compatible with the proposed growth process based on the impact of silicon clusters which melt upon impact on the surface of GaAs. Thus, PECVD epitaxy is a local process involving a very high temperature over very short times and small areas. The presence of large amounts of hydrogen can lead to the deactivation of dopants in the GaAs substrate but the doping properties can be recovered by annealing at 350 °C for a few minutes. This new epitaxial process opens new possibilities for the integration of silicon and III-V technologies.

ACKNOWLEDGEMENTS

This work was supported by the French ANR research program IMPETUS (ANR-13-PRGE-0009) and by a CIFRE convention of the ANRT (n° 2014/1031). The authors would like to thank Cristian Mocuta from SOLEIL synchrotron for his expertise and advices on DiffAbs beam line in the frame of the SUNSET project n° 20160862.

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