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UNDERSTANDING OF THE INFLUENCE OF THE SURFACE DEFECTIVITY ON SILICON HETEROJUNCTION CELL PERFORMANCE.

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ABSTRACT: The fabrication process of silicon heterojunction (SHJ) solar cells can induce locally depassivated regions (so-called *defectivity*) because of transportation steps (contact with belts, trays, etc) or simply the environment (presence of particles embedded within surface thin films). This surface passivation spatial heterogeneity is gaining interest as it may hinder the SHJ efficiency improvements allowed by incremental process steps optimizations. An experimentally-supported simulation study is proposed and applied on full size M2 SHJ cells in order to understand how the local *a*-Si:H/*c*-Si interface passivation loss impacts the overall cell performance. A simulation framework (developed on ATLAS Silvaco) was first validated through comparisons with experimental results. This step allowed then to use simulations results further to explore and understand the physics behind the defectivity-induced efficiency loss. The cell performance drop due to depassivated regions was attributed to a bias-dependent minority carrier recombination current flow towards the depassivated region, which is shown to affect mainly the Fill Factor.

Keywords: heterojunction, defectivity, recombination, silicon solar cells

1 INTRODUCTION

The deposition of stacks of intrinsic hydrogenated amorphous silicon (*a*-Si:H(i)) and highly doped amorphous silicon (*a*-Si:H(n/p)) layers on the monocrystalline silicon (*c*-Si) wafer for heterojunction solar cells (SHJ) provides outstanding surface passivation which has enabled cell efficiencies (η) around 24% on full size SHJ made on the pilot production line at CEA-INES [1]. In a context where very high carrier lifetime wafers are commercially available and extremely efficient surface passivation is reached, inhomogeneity at the cell level are inevitably gaining interest on the way to very high efficiencies. Among them the passivation spatial inhomogeneity, broadly referred to as “defectivity”, is put at the forefront of this study. Affected cells feature spots/patterns on photoluminescence images, which are associated with decreased carrier lifetime due to localized lacks/absence of passivation [2]. In parallel, the continuously increasing throughput of cell manufacturing tools [3] is likely to increase surface defectivity if handling steps are not properly optimized. In order for SHJ cell manufacturers to reach high performances, particular care has to be taken to avoid any surface damage that could locally but irreversibly harm the surface passivation and thus η .

To our knowledge, the physical mechanisms behind the influence of damaged regions on the SHJ cell performance have been very little addressed so far. O. Nos was able to empirically associate Fill Factor (*FF*) losses to photoluminescence (PL) images taken on SHJ cells sampled out of the pilot line at CEA [4]. Furthermore O. Breitenstein developed a local efficiency mapping tool based on Dark Lock-in Thermography (DLIT) which allows to figure out the effects of defectivity on η of SHJ cells taken out of a production line [5]. Both of these studies brought to light the importance of defectivity on the performance losses. However, they were performed on cells with unknown defectivity properties (shape, localization, recombination velocity) so the understanding of the mechanisms behind the device performance losses could only be partial.

In this context, the purpose of this work is to quantify and understand the influence of surface defectivity on the

cell current-voltage (*I(V)*) parameters. To this aim, devices with a well-defined and intentionally performed defectivity have been studied using combined experimental and simulation approaches, in order to unveil the nature of the degradation mechanisms at play.

2 EXPERIMENTAL AND SIMULATION DETAILS

2.1 Cells fabrication and controlled defectivity creation

All SHJ cells in this work are fabricated using the same process on the CEA-INES pilot production line, based on n-type Cz monocrystalline substrates (M2 format, PSQ 156.75 × 156.75 mm²). Wafers are textured and cleaned, with a final thickness of 160 μ m. Doped and intrinsic *a*-Si:H layers are deposited on both sides, with a n-doped stack (*i/n*) on the front side and a (*i/p*) stack on the rear, corresponding to the “inverted emitter” architecture [6,7]. Then, indium-tin oxide (ITO) layers are deposited on both sides by magnetron sputtering from an In₂O₃/SnO₂ target, under an Ar/O₂ gas mixture. Metal grids are screen-printed on both sides using a silver paste. Finally, the cells are annealed at 200 °C to cure the silver paste. More details about the cell process can be found in [6].

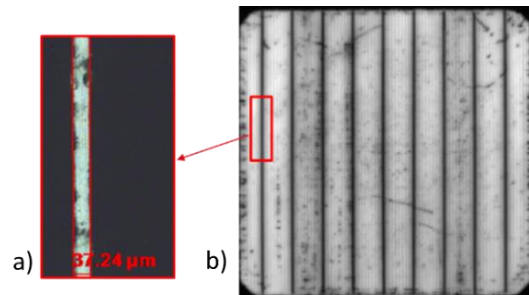


Figure 1: Optical microscopy picture of a scratch (on the left) and photoluminescence image of a cell with nine scratches on its front side.

In order to quantify the *I(V)* parameters losses induced by passivation inhomogeneities, a textbook case has been studied. On ten busbarless cells, controlled scratches have been performed on the front side through the whole length of the cells, using a diamond tip. A typical PL image after

scratches formation is shown in Fig.1b. The choice of busbarless cells was preferred as this metallization scheme facilitates in practice the scratching steps (no perpendicular metallization), and also the modelling of the structure (high level of symmetry). As shown in Fig.1b, nine scratches were made at a regular distance, each time between consecutive metallization fingers. The width of each scratch, measured by optical microscopy was fairly constant ($37\mu\text{m} \pm 5\mu\text{m}$) and proved the repeatability of the protocol the scratches depth was also measured and is assumed to negligibly increase the scratched surface. Furthermore, the optical microscopy performed on one scratch (Fig.1a) shows that the scratches remove the whole TCO/*a*-Si:H stack and in doing so, thoroughly depassivate the silicon surface. Thus the recombination velocity of the depassivated interface is assumed to be limited by carrier diffusion to the defect. This protocol leads to a defectivity whose shape, localisation and recombination velocity are therefore known.

In addition to the intentionally made scratches, other defects can be observed. The origin of these defects are unintended surface injuries or contaminations stemming from some wafer transportation steps and assumed to have a much less important effect on the cells performances than the intentionally created scratches, as can be inferred from Fig.1.b.

2.2 Simulation details

Simulations were run using the ATLAS package from Silvaco [8], a multiphysical simulation software. Fig.2 shows the modelled structure, which is a slice of the cell along its whole thickness, and nine metallisation pitches wide (which is the distance between two experimentally made scratches cf. Fig.1). Thus, the 2D structure is about $160\mu\text{m}$ deep and $16200\mu\text{m}$ wide. Furthermore, the properties of each layer are set based on characterization results obtained on the devices we intend to use for the experimental validation of this code. The (n)*c*-Si has a donor dopant density of $1.10^{15} \text{ cm}^{-3}$ and a single level acceptor-like defect centred at mid-gap with a defect density of 10^9 cm^{-3} leading to a resistivity $\rho = 4.5\Omega\cdot\text{cm}$ and a bulk lifetime $\tau_{\text{bulk}} = 1.7\text{ms}$. For all the *a*-Si:H(n) and *a*-Si:H(p) layers the band gap was set to 1.75 eV and to 1.65eV for the *a*-Si:H(i) layers.

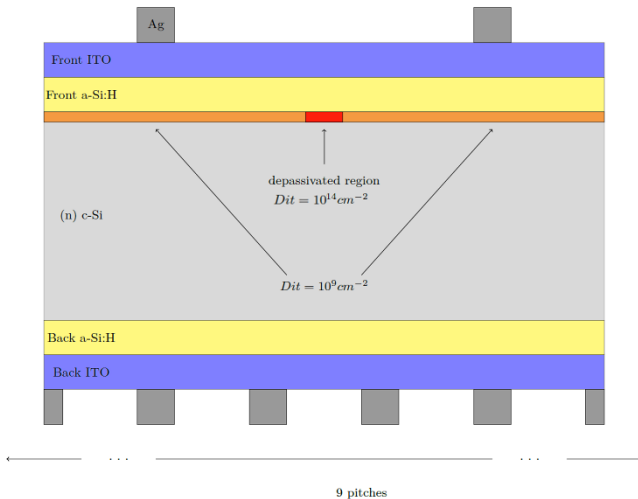


Figure 2: Representation of the simulated structure with the implementation of the depassivated region.

The valence and conduction band tail states were modelled by two decaying exponential functions with characteristic temperature T_v and T_c . The deep defects, known to be dangling bonds, obey an amphoteric statistics. The deep defect distribution was generated following the defect pool model from standard pool parameters used by Powel [9,10]. The emitter/absorber interface defects were simulated by introducing a 1 nm thick, highly defective layer at the front side (to reproduce scratches on experimental samples) or back side (to extend the study) (*i*)*a*-Si:H/(n)*c*-Si interfaces. On the front side D_{it} is set at 10^9 cm^{-2} to fit the cell performance. In order to implement the depassivated region, the D_{it} has been locally set at 10^{14} cm^{-2} in the middle of the device, on a width of $37 \mu\text{m}$. This has been chosen to have as many defects as Si atoms on the *c*-Si surface. The *a*-Si:H and *c*-Si electronic affinities have been set to 4.05 eV and 3.9 eV, respectively. Thermionic emission and tunnelling through the conduction or valence band spike at the *a*-Si:H/*c*-Si interfaces were taken into account. The front and back ITO are modelled as degenerated semiconductors. The front contact is taken to be ohmic and the necessary hole-electron recombination is set to occur at the backside (*p*)*a*-Si:H/ITO interface following Danielson's model [9].

Firstly, the structure is solved at the equilibrium. Then the structure is exposed to a AM1.5G spectrum and the collected current is calculated for several forward bias voltages in order to derive the cell $I(V)$ curve. The curve is then used to determine the individual $I(V)$ parameters

3 VALIDATION OF THE SIMULATION CODE

In order to validate the simulation code, a confrontation between simulation predictions and measurements performed on actual cells has been carried out. To this aim, $I(V)$ measurements were performed after each scratch creation on the ten busbarless cells described in section 2.1. The results are shown in Fig.3 (colored squares, 1 color = 1 cell). This graph calls for several comments. First of all, these results show a good repeatability of the scratch creation protocol.

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Indeed for all the cells the scratches induced efficiency losses amounts 6%rel. The efficiency loss are driven by FF losses which represent 4 of the 6%rel efficiency losses while the short circuit current J_{sc} and the open circuit voltage V_{oc} are decreased by about 1.5% each. This result shows that the defectivity has an effect much more important than the only impact of unpassivated surface.

In order to validate the simulation code, simulations have been performed without defectivity and then with the same proportion of good and degraded area as for the measured samples. The results are shown in Fig.3 as red stars. The good agreement between experimental details and simulation results shows that the simulation is able to predict accurately the defectivity induced $I(V)$ parameters losses: the difference between the simulated and measured $I(V)$ parameters are lower than 1%. This comparison is a validation of the simulation model. Thus, the simulation constitutes a solid basis for an investigation on the defectivity induced cells performance losses.

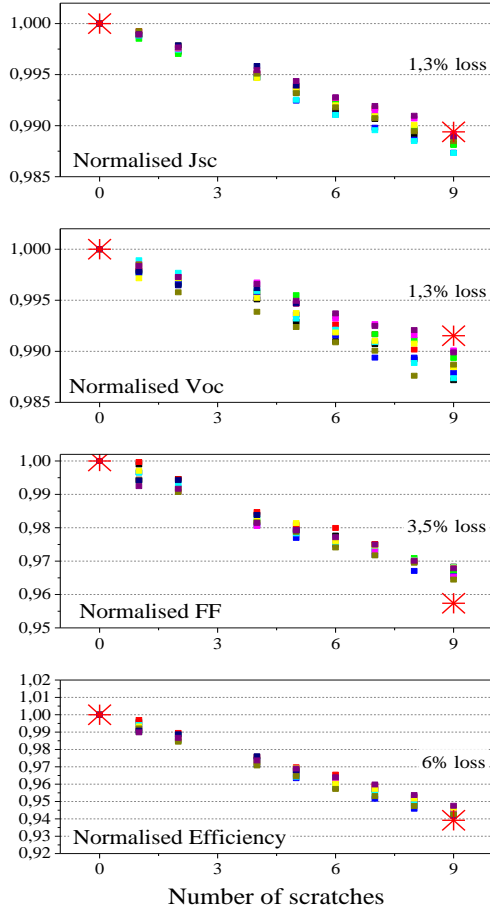


Figure 3: Normalized $I(V)$ parameters evolution with an increasing number of scratches made on 10 busbarless SHJ solar cells. Each cell corresponds to a coloured square. The red stars are the simulated $I(V)$ for cells with or without defectivity on their front c -Si/ a -Si:H interface

4 LOSS MECHANISMS STUDY

In this part, the simulation code is used to explain the mechanisms behind the defectivity-induced performance losses. The simulation software allows the calculation and plotting of physical quantities like quasi-Fermi levels, current densities, carriers concentration, etc. The minority carriers quasi fermi level has been studied because it takes into account both the diffusion and the electric field components of the minority carriers current densities: the quasi Fermi level gradient in space is thus directly proportional to the force applied to the holes [10].

In Fig.4, the hole quasi fermi level $\varepsilon_{F,h}$ is plotted without (a) and with (b) a depassivated region on the cell front a -Si:H/ c -Si interface. The quasi fermi level zero is set as its level in the equilibrium structure. Without the depassivated region, there is a $\varepsilon_{F,h}$ gradient $\vec{\nabla} \varepsilon_{F,h}$ towards the backside a -Si:H/ c -Si interface which favors the holes motion towards the (i+p) a -Si:H hole contact. It can be noticed that the gradient norm $\|\vec{\nabla} \varepsilon_{F,h}\|$ is decreasing as the voltage increases. When the voltage is lower than a threshold voltage $V_t \approx 0.45V$ (see Fig.4c) the $\varepsilon_{F,h}$ profile does not change significantly and the collected current is the same for any bias voltage. This can be explained as for $V < V_t$, the strong field effect allows for an efficient hole extraction via the junction. For $V > V_t$ instead, the field effect at the (i+p) a -Si:H/ c -Si interface decreases leading to a less effective hole extraction. The collected current decreases, until open circuit condition is reached where no current flows any longer (corresponding to $\|\vec{\nabla} \varepsilon_{F,h}\|=0$). Let us now turn to the case where a depassivated region is present at the front a -Si:H/ c -Si interface. While the picture is basically the same at the BS, a strong additional gradient directed towards the depassivated region shows up (Fig.4b)). This component is denoted $\nabla \varepsilon_{F,h}\{def\}$.

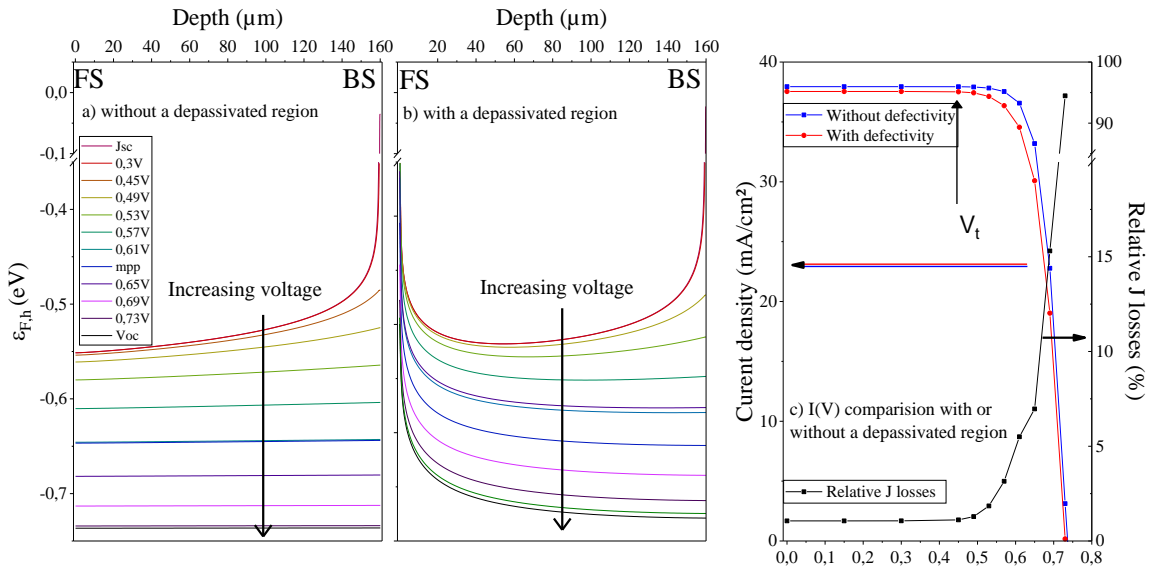


Figure 4: Vertical profile of the hole QFL $\varepsilon_{F,h}$ (relative value with respect to its value in the structure at the equilibrium) under the depassivated region and along the c -Si depth from the front side FS (left) to the backside BS (right) without (a) or with (b) a depassivated zone at the front a -Si:H/ c -Si interface at several working point under a AM1.5G illumination. $I(V)$ measurement for cells with or without a depassivated region and the associated current relative losses are plotted in c).

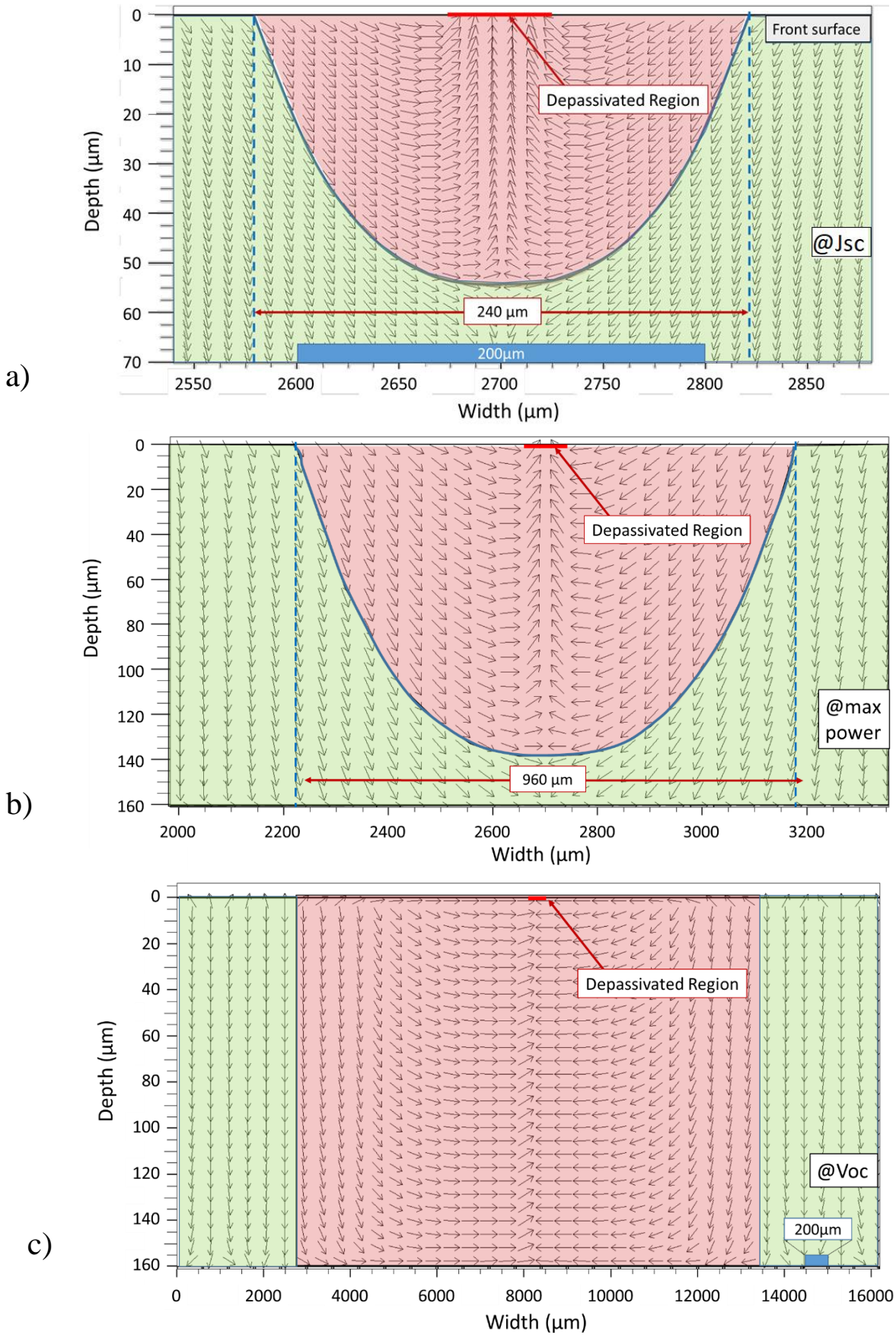


Figure 5 : Hole current density map in the c-Si around the depassivated region, at a) the short circuit working point b) the max power working point and c) the open circuit working point. The current densities are directed towards the depassivated region (red zone) or the emitter (green zone).

In a similar fashion to the BS, if the bias voltage increases from V_i to the open circuit voltage, the $\vec{\nabla} \varepsilon_{F,h}\{def\}$ contribution to $\vec{\nabla} \varepsilon_{F,h}$ becomes greater until the open circuit working point where the hole QFL gradient is equal to $\vec{\nabla} \varepsilon_{F,h}\{def\}$.

From this observation, it can be noticed that the $\vec{\nabla} \varepsilon_{F,h}\{def\}$ relative contribution to $\vec{\nabla} \varepsilon_{F,h}$ increases with increasing bias voltage. As a consequence, the relative current losses at a given bias voltage increases from V_i to the open circuit working point (Fig.4c).

These observations can be used back to explain quantitatively the results of Fig.3. Firstly, as exposed above, at the open circuit working point, $\nabla \varepsilon_{F,h} \approx \nabla \varepsilon_{F,h}\{def\}$. So at this working point, charge carriers wherever they are located, feel a force directed towards the depassivated area. Thus, holes are attracted towards the defective area as shown in Fig.5c. However, on average, they can only reach it provided that they have been photogenerated at a distance L from the depassivated area smaller than their diffusion length L_d . Assuming that all holes photogenerated at a distance $L < L_d$ from the depassivated area recombine there, and taking into account that the simulation shows that 85% of the photogeneration occurs in the first 20 μm from front a-Si:H/c-Si interface, we can approximate that the depassivated region affects a $2L_d$ wide surface around the scratch, which corresponds to 15% of the whole cell surface leading to a 15% carriers loss. Given the expression of the open circuit voltage:

$$V_{oc} \approx \frac{kT}{e} \text{Ln} \left[\frac{\Delta p(\Delta n + n_0)}{n_i^2} \right]$$

where k is the Boltzmann constant, T the temperature, e the elementary charge, $\Delta n, \Delta p$ are the excess carrier concentration (or injection level) at V_{oc} operating point, n_0 the doping concentration and n_i is the intrinsic carrier concentration. In this study, the open circuit excess carrier concentration far from a depassivated area is $1.6 \times 10^{16} \text{ cm}^{-3}$, as obtained from simulations. Applying a 15% carrier concentration loss to FS defectivity, the open circuit voltage is decreased by 1.4%, which is consistent with the results shown in Fig.3.

An analogous analysis can be carried out for the short circuit current losses. As exposed above, at this working point, $\|\vec{\nabla} \varepsilon_{F,h}\{def\}\|$ has only a little contribution to $\vec{\nabla} \varepsilon_{F,h}$. Thus the depassivated region affected area is very little extended. Furthermore, given that photogeneration under an AM1.5 spectrum occurs mostly at the vicinity of the front c-Si surface, the short circuit current loss is determined by the area where $\vec{\nabla} \varepsilon_{F,h}$ is directed towards the depassivated area close to this interface. The hole current densities at this interface is mapped on Fig.5. Note that the hole current densities are directly proportional to $\vec{\nabla} \varepsilon_{F,h}$. From Fig.5, the frontier line between the regions where the holes flow to the depassivated area and where they flow to the back side to be extracted is situated at a distance $L < 115 \mu\text{m}$ from the depassivated region. This corresponds to 1.4% surface area. Considering that all the holes photogenerated in this area are lost through recombination in the depassivated region, one can calculate the short circuit current losses to be around 1.4%, which is again consistent with the results presented in Fig.3.

Finally, the same argument holds for the FF losses. At the maximal power working point, the $\vec{\nabla} \varepsilon_{F,h}$ was analyzed in the same way as for the short circuit current (Fig.5). It appears that the affected region is about 6% of the cell surface leading to a 6% loss of the total photogenerated carriers. This observation leads to the conclusion that the efficiency losses are expected to be about 6% which is consistent with the results presented in Fig.3. Furthermore, the cell produced power relative losses are given by

$$\Delta P = \Delta V_{oc} \times \Delta J_{sc} \times \Delta FF,$$

it can be deduced that the FF losses are about 3.3% which is consistent with the results in Fig.3.

4. CONCLUSION

In this work, we investigate by means of experiments and simulations the impact of surface local defectivity on the front side of SHJ solar cell performances. First, a protocol of controlled defectivity formation was established, which was subsequently used to investigate the influence of incremental defectivity creation on all $I(V)$ parameters. This first experimental study demonstrated a strong effect on the efficiency, amounting to -6%rel for “only” 0.2% of the surface being defective, mostly driven by a FF loss (in agreement with previous work on industrial solar cells). In a second part, we resorted to numerical simulations in order to explain the physical mechanisms behind this effect. In a first step, the ability of simulation to predict the cell degradation was ascertained by comparison with experimental values on a textbook case. Simulation results were then trusted further, and a deeper analysis was then carried out on the basis of the calculated quasi-Fermi level mappings throughout the cell. In particular, we evidenced how the depassivated region at the cell front side creates a bias voltage-dependent current towards itself and explained how this reduces the overall cell performances. An equivalent study focused on the defectivity on the cell back side has been carried out, and we be detailed in a forthcoming paper. We also intend to use the developed simulation framework to investigate how the defectivity-induced degradation is influenced by cell properties (substrate electronic properties, doping of a-Si:H layer, etc), and by the defectivity geometry (size, spatial distribution).

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