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Doping profile extraction in thin SOI films: application to A2RAM

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Abstract—We propose for the first time a method based on C-V measurement to extract the bridge doping profile which governs the operation and performance of A2RAM capacitorless memory cell. Assessed with TCAD simulation and simple extraction model adapted from bulk devices, this technique is validated with experimental data.

Keywords— A2RAM; C-V characteristic; SOI; electrical characterization, doping profile.

I. INTRODUCTION

The A2RAM (Fig.1) is a capacitorless, single-transistor 1T-DRAM [1] with an N-doped layer (nMOS case) called ‘the bridge’ located at the bottom of the low-doped p-type body. The bridge allows short-circuiting the source and drain. The concept of A2RAM has been presented in [2] and its experimental performance in [3]. Recently, the scalability issues of the A2RAM have been studied by TCAD simulations [4]. We noticed some inconsistencies with measurements, presumably related to the mismatch of the bridge doping profile between TCAD simulations and experiments. As the A2RAM behavior is strongly related to the bridge parameters, we need an accurate solution to evaluate them. The use of physical characterization such as Secondary-Ion Mass Spectroscopy (SIMS) is not reliable here because (i) the silicon film is too thin and (ii) the target doping is too low (around 10^{18}cm^{-3}). Therefore, a method based on electrical measurement is the most suitable option. For this purpose, the C-V electrical characterization is emulated through TCAD simulations and validated with experimental data.

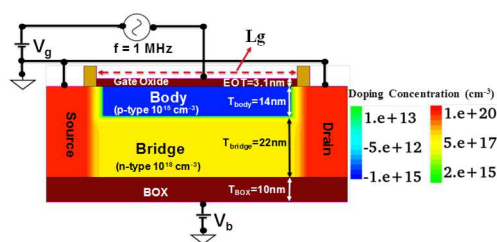


Figure 1. Simulated A2RAM cell with parameters defined by the process flow in [3].

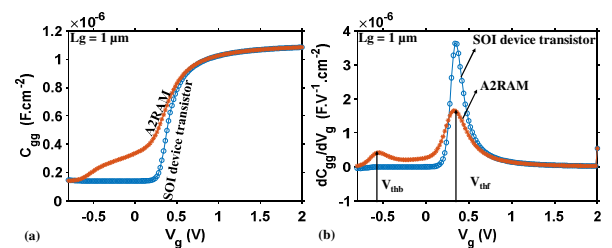


Figure 2. (a) $C(V_g)$ characteristic of the A2RAM and standard SOI transistor with same silicon thickness but no doped bridge. (b) First derivative of the C-V curves.

II. A2RAM: TCAD SIMULATION METHODOLOGY AND C-V CHARACTERISTIC

The A2RAM structure (Fig. 1) is simulated with Synopsys TCAD tools [5] using Drift-Diffusion and doping-dependent mobility models. We consider abrupt Gaussian doping profiles for source, drain and bridge. A mid gap metal electrode is used at the top and back gates. The main technological parameters of the reference structure (fabrication details provided in [3]) are body thickness $T_{\text{body}} = 14$ nm (p-type with a concentration of 10^{15} cm^{-3}), bridge thickness $T_{\text{bridge}} = 22$ nm, n-type bridge doping $N_{\text{bridge}} = 10^{18}$ cm^{-3} , equivalent oxide thickness $EOT = 3.1$ nm and buried oxide (BOX) thickness $T_{\text{BOX}} = 10$ nm. We performed small signal simulation on long gate ($L_g = 1$ μm) device and report on Fig.2-(a) the gate capacitance C_{gg} versus the gate voltage V_g for both A2RAM and standard SOI transistor (having the same technological parameters as the A2RAM, but without bridge).

For high voltage ($V_g \gtrsim 1$ V), we can notice that the FDSOI and A2RAM C-V behavior is the same, providing to front-gate channel capacitance C_{gg} in strong inversion. Then, similarly to back-biased FDSOI devices with an inverted back channel, the A2RAM $C_{\text{gg}}-V_g$ characteristic shows a second hump related to the activation of the conduction in the bridge. It is possible to define two threshold voltages for the formation of these channels. Fig.2-(b) shows the first derivative of the C-V curves. When the front-gate bias increases, the first hump is related to the activation of the ‘conduction in the bridge’ at V_{thb} and the second one to the formation of the classical front inversion channel at V_{thf} .

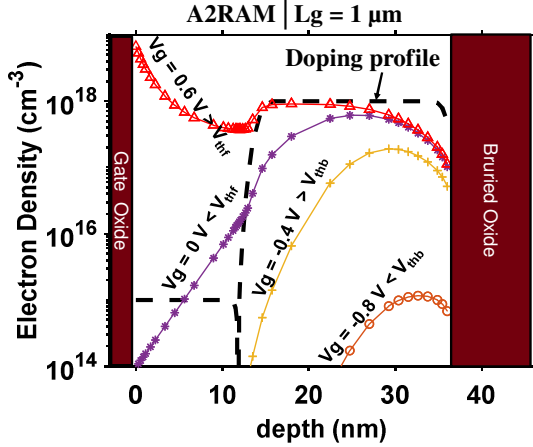


Figure 3. Comparison of the doping profile with electron density profile at different gate bias V_g during the small signal simulation of Fig.2.

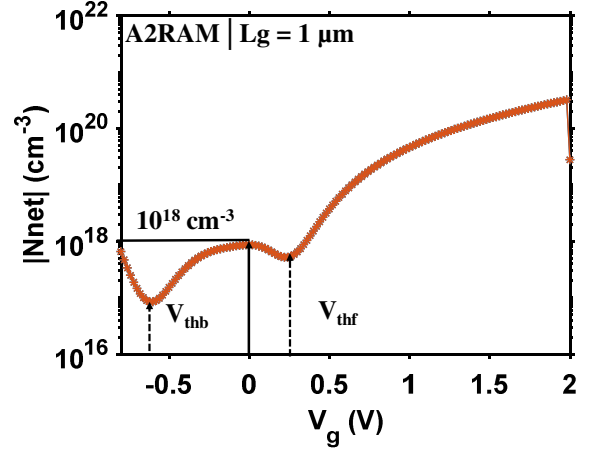


Figure 4. Doping function evaluated from the C-V in Fig.2-a.

III. BRIDGE DOPING PROFILE EXTRACTION METHODOLOGY WITH TCAD

Doping profile extraction through C-V measurement has already been performed with several techniques suitable for bulk technology [6-9]. The selected method was adapted to our case and relies on three following equations:

$$C_{\text{gg}}^{-1} = (C_{\text{ox}}^{-1} + C_s^{-1}) \quad (1)$$

$$Y(V_g) = \frac{1}{C_{\text{gg}}^3} \frac{dC_{\text{gg}}}{dV_g} = \frac{1}{C_s^3} \frac{dC_s}{d\Psi_s} \quad (2)$$

$$N_{\text{net}} = (q\varepsilon_s Y(V_g))^{-1} \quad (3)$$

where C_{gg} , C_{ox} and C_s are the total gate capacitance, the gate oxide capacitance and the semiconductor capacitance respectively. Ψ_s is the surface potential, q the elementary charge, and ε_s the silicon permittivity. Equation (1) is given for a bulk MOSFET where

C_{gg} corresponds to C_{ox} and C_s in series. Equation (2) called the ‘‘Maserjian formula’’ was demonstrated in [6] using (1) to extract the density of state at the front interface in MOS device transistors. From equation (2), the total density of charges in the semiconductor N_{net} can be evaluated using equation (3) called the ‘doping function’. Actually in a MOS transistor, small signal variation applied on the top metal electrode leads to the variation of the charge in the semiconductor. Besides, in the hypothesis of depletion regime, equation (1) can be used for the evaluation of the depletion depth in semiconductor and equation (3) to determine the total charge in the semiconductor. In [7], this technique is used for a uniformly doped bulk MOSFET to extract the impurity charge density as a function of the depletion depth. In the same way, [8] used also this technique in bulk technology but with high uniformly doped heterojunction. Finally, [9] used the technique in the depletion regime to extract the impurity density of charge as a function of the depletion depth in thick (partially depleted) and uniformly doped SOI transistor.

Previously, this technique was utilized only for thick and/or uniformly doped MOS transistor. Therefore, our goal is to adapt this method to thin and lower doped SOI layer like A2RAM structure and explore its reliability limits. The idea is to extract the body thickness from (1) and use (3) to determine the bridge doping value. To ensure that the density of charge extracted equals N_{bridge} , the body must be in depletion regime but without depleting the bridge layer. Thanks to the small signal simulation, we can find this condition by checking the evolution of the charge (electron density) in the A2RAM structure. Fig.3 shows the modification of the vertical electron density profile in the A2RAM at different gate bias in comparison with the original doping profile. Before the activation of the bridge ($V_g < V_{thb}$, when the bridge is also fully ‘‘depleted’’), the whole structure is fully depleted, this is why on Fig.2-(a), the C-V of the A2RAM and SOI device transistor are alike. After the activation of the bridge ($V_g \geq V_{thb}$), the electron density profile increases suddenly at the bottom of the body but its value is lower compared to the nominal bridge doping value. The whole body can still be considered as being in depletion regime. At $V_g = 0$ V (it corresponds to the lowest V_g close to V_{thf} on Fig.2-b), the value of the electron density is increased, and it nearly equals the doping profile but the body starts to become inverted. Finally, after the activation of the front interface ($V_g \geq V_{thf}$), the electron density profile shows an inversion charge below the gate oxide much higher than the bridge doping; that is why on Fig.2-(a) the C-V of the A2RAM and SOI transistor are identical again. From this description, we can understand that the extraction of the doping profile must be performed in the range of gate bias such as $V_{thb} < V_g < V_{thf}$.

A. Extraction of the ‘doping profile of the bridge’

Having measured C_{gg} and considering the depletion regime in the body with all the dopants ionized, we can use equation (3). Fig.4 shows $|N_{net}|$ versus V_g derived from the C-V characteristic of the A2RAM (Fig.2-(a)). In the gate bias range between V_{thb} and V_{thf} , the ‘doping function’ presents a broad peak between V_{thb} and V_{thf} with the maximum value 10^{18} cm^{-3} at $V_g = 0$ V which is equal to the doping value set in TCAD (Fig.1).

Then, we aim to determine a range of bridge doping where this method can be applied. We perform small signal simulation of the same A2RAM structure as in Fig.1, by varying the bridge doping from 10^{17} to $3 \cdot 10^{18} \text{ cm}^{-3}$. We also consider the SOI MOSFET of Fig.2 (*i.e.*, no bridge). The role of the SOI transistor here is to evidence when the A2RAM structures start to behave like FDSOI (*i.e.*, no free charge in the silicon film). As it can be noted on Fig.5-(a), the bridge is in conduction for high N_{bridge} ($> 3 \cdot 10^{17} \text{ cm}^{-3}$) because it is not fully depleted by the field effect. That is why on Fig.5-(b), we can effectively see the double peak only for $N_{bridge} > 3 \cdot 10^{17} \text{ cm}^{-3}$. The double peak is not visible in the case of $N_{bridge} = 3 \cdot 10^{18} \text{ cm}^{-3}$ where the first peak is located at very negative gate voltage. In fact, while the increase of N_{bridge} shifts V_{thb} to the left (*i.e.* towards more negative V_g values), the reduction of N_{bridge} shifts V_{thb} in the opposite direction (Fig.5-(b)). For lower N_{bridge} ($\leq 3 \cdot 10^{17} \text{ cm}^{-3}$), the corresponding V_{thb} and V_{thf} tend to be equal.

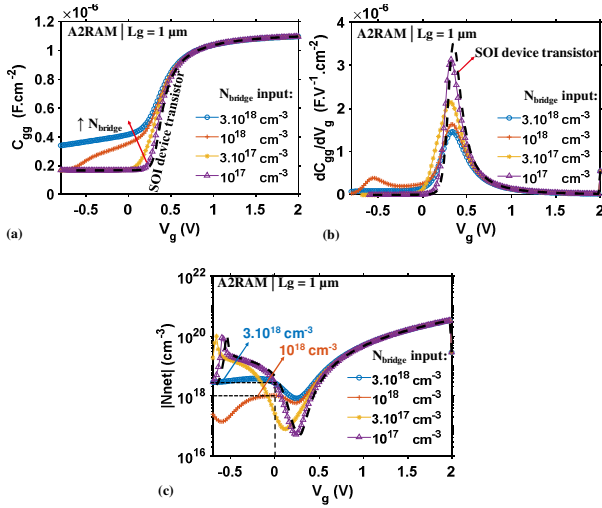


Figure 5. Comparison of the C-Vs and its first derivative of a SOI device transistor with (a,b) A2RAM as defined in Fig.1 but with $N_{\text{bridge}} = 3.10^{18}$, 10^{18} , 3.10^{17} , and 10^{17} cm^{-3} , and (c) Doping function obtained from small signal simulations of A2RAMs as defined in Fig.1 but with $N_{\text{bridge}} = 3.10^{18}$, 10^{18} , 3.10^{17} , and 10^{17} cm^{-3} .

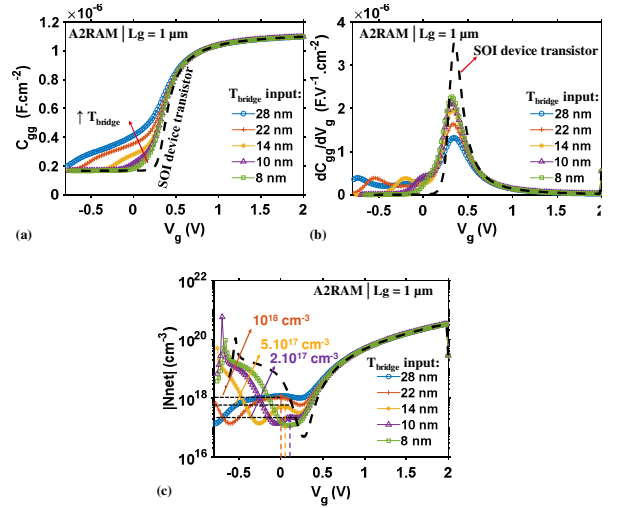


Figure 6. Comparison of the C-Vs and its first derivative of a SOI device transistor with (a,b) A2RAM as defined in Fig.1 but with $N_{\text{bridge}} = 3.10^{18}$, 10^{18} , 3.10^{17} , and 10^{17} cm^{-3} , and (c) Doping function obtained from small signal simulations of A2RAMs as defined in Fig.1 but with $T_{\text{bridge}} = 28, 22, 14, 10$ and 8 nm .

This implies that the conduction of the bridge and the front interface channel are simultaneously activated. Thus, the A2RAM behaves as a standard SOI transistor and the N_{bridge} extraction on Fig.5-(c) has no sense. Nonetheless, with higher values of N_{bridge} ($> 3.10^{17} \text{ cm}^{-3}$), the bridge doping can be accurately evaluated (Fig.5-(c)).

We conducted a similar sensitivity analysis to assess the validity of our method considering the T_{bridge} variation. The small signal simulations of A2RAM described on Fig.1 are performed with bridge thickness T_{bridge} from 8 to 28 nm. The results are compared with the ones of a SOI transistor (*i.e* without bridge). Fig.6-(a) shows that the conduction of the bridge increases for thicker T_{bridge} . V_{th} is shifted to the left when T_{bridge} increases and to the right if T_{bridge} decreases as evidenced on Fig.6-(b). Good accuracy can be guaranteed for T_{bridge} thicker than 22 nm as it can be noticed on Fig.6-(c). For $T_{\text{bridge}} < 22 \text{ nm}$, the bridge doping extracted is very low compared to the input value set in TCAD due to partial depletion of the bridge.

However, on Fig.3 when the bridge is in conduction (for V_{th}

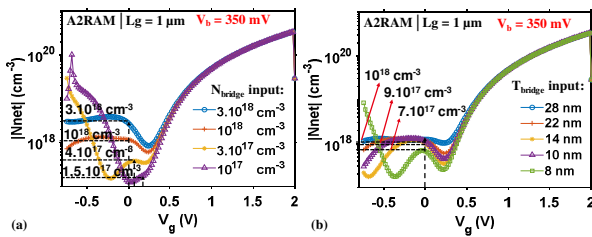


Figure 7. (a) Doping function obtained from small signal simulations at back gate voltage $V_b = 350 \text{ mV}$ of A2RAMs as defined in Fig.1 but with $N_{\text{bridge}} = 3.10^{18}$, 10^{18} , 3.10^{17} , and 10^{17} cm^{-3} . (b) Doping function obtained from small signal simulations at back gate voltage $V_b = 350 \text{ mV}$ of A2RAMs as defined in Fig.1 but with $T_{\text{bridge}} = 28, 22, 14, 10$ and 8 nm .

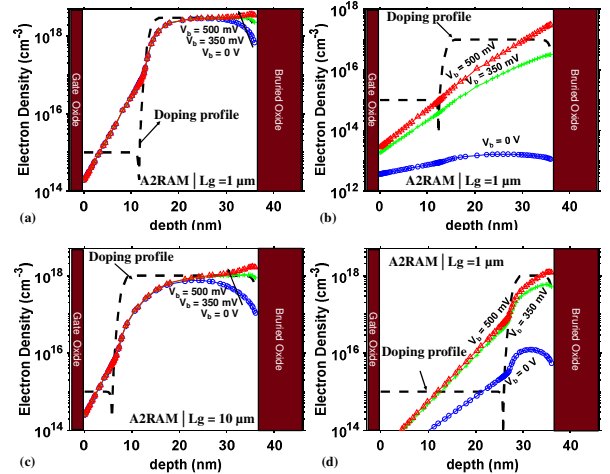


Figure 8. comparison of the doping concentration with the electron density extracted at $V_g = 0 \text{ V}$ for different V_{back} for an: (a) A2RAM as defined in Fig.1 with $N_{\text{bridge}} = 3.10^{18} \text{ cm}^{-3}$, (b) A2RAM as defined in Fig.1 with $N_{\text{bridge}} = 10^{17} \text{ cm}^{-3}$, (c) A2RAM as defined in Fig.1 with $T_{\text{bridge}} = 28 \text{ nm}$, and (d) A2RAM as defined in Fig.1 with $T_{\text{bridge}} = 8 \text{ nm}$; obtained TCAD simulations.

$< V_g < V_{thr}$) electron density at the back interface remains lower than the concentration in the volume (thus also lower than to the initial doping concentration). This means that flat band condition at the back interface is not achieved (*i.e.*, the back interface is still in depletion regime). For high $N_{bridge} (> 3.10^{17} \text{ cm}^{-3})$, the effect of this ‘depletion’ remains within few nanometers above the BOX (not shown). This explains why equation (3) is valid for the extraction of N_{bridge} (Fig.5). But, reducing the bridge doping value like in Fig.5, while keeping the same mid gap metal at the back gate, increases the depletion of bridge due to the change in flat band condition. Accordingly, we need to apply a back-bias V_b that compensates the flat band voltage shift. In fact, if the back gate is properly biased, it is possible to extract an accurate doping value even for lower doping ($< 3.10^{17} \text{ cm}^{-3}$) as it is highlighted on Fig.7-(a). This observation encouraged us to further investigate if we can improve the accuracy of the bridge doping extraction when T_{bridge} is reduced. Fig.7-(b) confirms that biasing the back interface enhances the resolution of the extraction.

As observed for the N_{bridge} variation, the T_{bridge} variation shifts also the flat band condition. However, there is a limit of the back bias that can be applied on the back-interface. On Fig.8, we compare the electron density extracted at gate voltage $V_g = 0 \text{ V}$ with the original ‘doping concentration’ for different structures at variable V_b . For $V_b > 500 \text{ mV}$, the electron density at the back interface is higher than the concentration in the volume of the bridge. Its variation is restricted to just a few nanometers above the BOX, due to ‘‘weak inversion’’. That is why, for this study, we have limited V_b at 350 mV.

Our simulations consider a metal electrode directly below the BOX with a mid-gap work function. In real A2RAM devices [3], a silicon ground plane GP acts as the back gate. We can deduce that the presence of a GP instead of a metal electrode at the back interface will change the flat band condition. To determine the impact of GP on our extraction methodology, we performed simulation of A2RAM including a p-type GP (doping 10^{18} cm^{-3}). Because of the flat band condition changes at the back interface induced by the depletion in the GP, the C-V curves are not aligned (Fig.9-a). We need to apply 500 mV on the GP to superpose the C-V plots for metal and silicon back gate (Fig.9-(a,b)). In this condition, the bridge doping extracted is the same as the one without the GP (Fig.9-c).

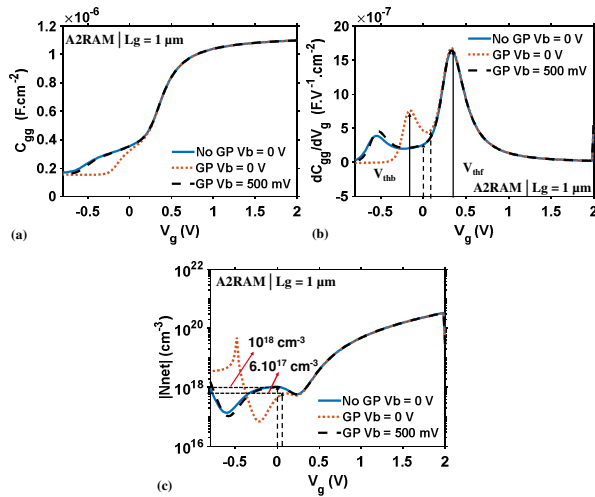


Figure 9. (a) C-V characteristic, (b) first derivative of the C-V, (c) doping function, and (d) depletion depth of the A2RAM with mid-gap back metal and with a p-type GP (TCAD simulations).

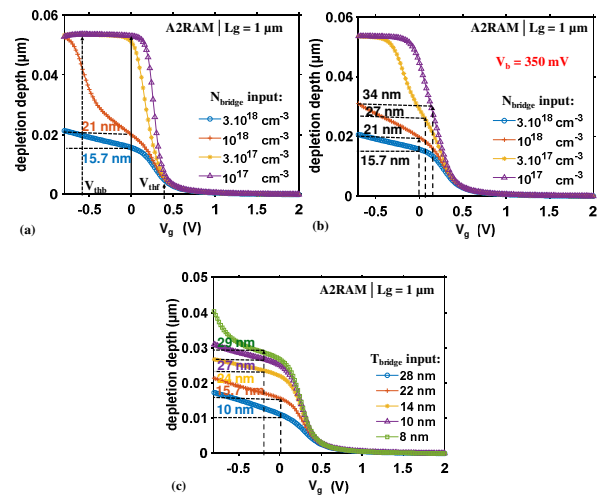


Figure 10. depletion depth as defined with (4) evaluated from: (a) the C-V in Fig.2-a, (b) small signal simulations of A2RAMs as defined in Fig.1 but with $N_{bridge} = 3.10^{18}, 10^{18}, 3.10^{17},$ and 10^{17} cm^{-3} , (c) small signal simulations of A2RAMs as defined in Fig.1 but with $N_{bridge} = 3.10^{18} \text{ cm}^{-3}$ and $T_{bridge} = 28, 22, 14, 10$ and 8 nm .

In conclusion, we demonstrate that our doping extraction methodology is valid for $N_{bridge} > 10^{17} \text{ cm}^{-3}$ and $T_{bridge} > 8 \text{ nm}$ if flat band condition at back interface is guaranteed by adequate back-gate polarization V_b .

B. Extraction of the 'Body' thickness

We aim to extract the body thickness T_{body} . At a gate voltage between V_{thb} and V_{thf} , the bridge is still formed, and the body is depleted. In this particular case, we can use equation (1) and the depletion layer corresponds to the p-doped body layer, so we have:

$$\text{depletion depth} = T_{\text{body}} = \varepsilon_{\text{Si}}(C_{\text{gg}}^{-1} - C_{\text{ox}}^{-1}) \quad (4)$$

As we precisely know the value of the total silicon thickness T_{Si} , we can easily deduce T_{bridge} ($T_{\text{bridge}} = T_{\text{Si}} - T_{\text{body}}$). Fig.10-(a) shows the depletion depth versus the gate bias V_g for bridge doping value from 10^{17} to $3 \cdot 10^{18} \text{ cm}^{-3}$. The depletion depth corresponding to the electrical thickness of the 'body' must be determined at same gate voltage as the one used for the bridge doping extraction (in this case $V_g=0$). When N_{bridge} is high ($> 3 \cdot 10^{17} \text{ cm}^{-3}$), it is still possible to extract a depletion depth because the bridge is not depleted by the gate electric field effect. If N_{bridge} is too low ($< 3 \cdot 10^{17} \text{ cm}^{-3}$), the silicon film is fully depleted (Fig.5-(a) and Fig.5-(b)) including the bridge. It follows that C_{gg} capacitance depends on BOX capacitance and equation (4) cannot be used. This explains why $T_{\text{body}} > T_{\text{Si}}$ for low N_{bridge} . But, T_{body} extraction is more accurate for higher doping: for $N_{\text{bridge}} = 3 \cdot 10^{18} \text{ cm}^{-3}$, we obtain $T_{\text{body}} = 15.7 \text{ nm}$, just 2 nm thicker than the expected 14 nm.

In order to examine the effect of flat-band condition on the accuracy of T_{bridge} for $N_{\text{bridge}} < 3 \cdot 10^{18} \text{ cm}^{-3}$, Fig.10-(b) shows the extraction of T_{body} for $V_b = 350 \text{ mV}$. But even in this condition, the resolution of the extraction is not improved. So good accuracy on T_{body} extraction is guarantee only for $N_{\text{bridge}} > 10^{18} \text{ cm}^{-3}$.

For a bridge doping of $3 \cdot 10^{18} \text{ cm}^{-3}$, we now determine a range of bridge thickness T_{bridge} where (4) can still be used. Fig.10-(c) shows the results obtained for different bridge thickness values (28, 22, 14, 10, and 8 nm) with the same bridge doping N_{bridge} ($3 \cdot 10^{18} \text{ cm}^{-3}$). The T_{body} extracted are 10, 15.7, 24, 27, and 29 nm instead of 8, 14, 22, 26, and 28 nm, respectively. The error does not exceed a difference of 2 nm (the maximum). Therefore, T_{body} extraction accuracy depends on the bridge doping: higher N_{bridge} means higher accuracy.

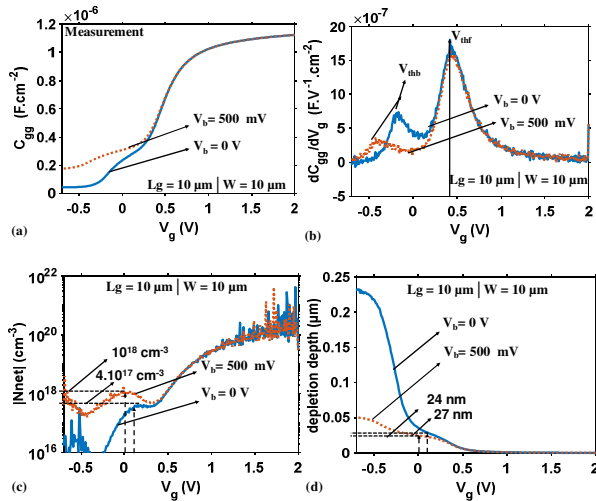


Figure 11. (a) C-V characteristic, (b) first derivative of the C-V, (c) doping function, and (d) depletion depth of the A2RAM sample [3] with mid-gap back metal and with a p-type GP.

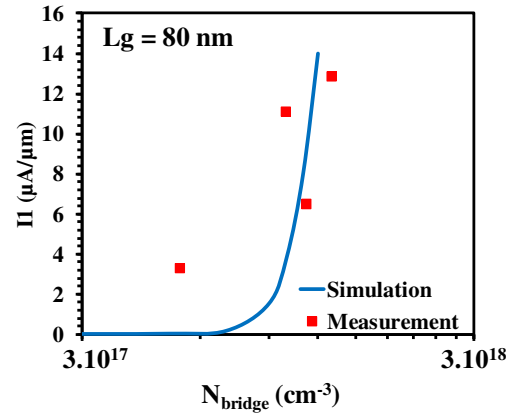


Figure 12. The '1' state reading current I_1 versus the bridge doping N_{bridge} measured on devices reported on Table II, and we compare the results achieved in measurement with the prediction of TCAD simulations.

C. Experimental results and discussion

We have extracted the doping profile of the bridge on the samples fabricated at LETI with process flow described in [3] (the expected experimental parameters are the ones used on Fig.1). The experimental C-V characteristics with two V_b shown on Fig.11-(a) are comparable to C-V curves obtained from TCAD simulations. On Fig.11-(b), the double peak evidences the conduction of the bridge and the front interface. The bridge doping value extracted at $V_b = 0$ V (dotted lines) is $4 \cdot 10^{17} \text{ cm}^{-3}$. From the TCAD analysis of part III-A, since the extracted value is below 10^{18} cm^{-3} , to guarantee an accurate extraction, it is mandatory to apply a bias $V_b > 0$ V as close as possible to flat band condition in back interface. From the process flow, we know that the concentration of P-type GP is around 10^{18} cm^{-3} . So, from the results of the simulation shown on Fig.8 and Fig.9, we have used the C-V curves measured with $V_b = 500$ mV. As a consequence, on Fig.11-(a) and Fig.11-(b) (solid line), we can notice a shift of the curves due to the flat band condition change. From Fig.11-(c) at $V_b = 500$ mV, the corresponding N_{bridge} extracted value (10^{18} cm^{-3}) is higher than the previous one ($4 \cdot 10^{17} \text{ cm}^{-3}$) and it is in the range of the expected value. However, the T_{body} extracted (Fig.11-d) at $V_b = 0$ V (27 nm) or at $V_b = 500$ mV (24 nm) is overestimated because the value of N_{bridge} is low (as we have noticed and concluded on Fig.10).

TABLE I.

EXTRACTION OF THE DOPING PROFILE ON 4 SAMPLES [3] AT TWO BACK INTERFACE BIAS

| | <i>Die 01</i> | <i>Die 02</i> | <i>Die 06</i> | <i>Die 09</i> |
|----------------------------|---|--|--|--|
| <i>V_b=0V</i> | <i>T_{body}=26nm</i> | <i>T_{body}=25nm</i> | <i>T_{body}=26,5nm</i> | <i>T_{body}=46,6nm</i> |
| | <i>T_{bridge}=10nm</i> | <i>T_{bridge}=11nm</i> | <i>T_{bridge}=9,5nm</i> | <i>T_{bridge}= NaN</i> |
| | <i>N_{bridge}=4.10¹⁷cm⁻³</i> | <i>N_{bridge}=5.10¹⁷cm⁻³</i> | <i>N_{bridge}=3.6.10¹⁷cm⁻³</i> | <i>N_{bridge}=6.10¹⁶cm⁻³</i> |
| <i>V_b=500mV</i> | <i>T_{body}=24,4nm</i> | <i>T_{body}=23,5nm</i> | <i>T_{body}=24,3nm</i> | <i>T_{body}=25nm</i> |
| | <i>T_{bridge}=11,6nm</i> | <i>T_{bridge}=12,5nm</i> | <i>T_{bridge}=11,7nm</i> | <i>T_{bridge}=11nm</i> |
| | <i>N_{bridge}=1,12.10¹⁸cm⁻³</i> | <i>N_{bridge}=1.10¹⁸cm⁻³</i> | <i>N_{bridge}=1,3.10¹⁸cm⁻³</i> | <i>N_{bridge}=5,3.10¹⁷cm⁻³</i> |

On Table I, we summarize the values extracted on different samples (gate length $L_g = 10 \mu\text{m}$ and width $W = 10 \mu\text{m}$) at two back gate voltages ($V_b = 0$ V and $V_b = 500$ mV). We can notice that even if all the devices have the same fabrication process, the doping profiles are different on each sample. We can suppose that this doping fluctuation has a consequence on memory performance. So, we have performed memory characterization on the samples in Table I and compared the results with the ones obtained by TCAD simulations. Fig.12 shows the evolution of the '1' state reading current when N_{bridge} varies. Note how the TCAD simulation trends match with the measurements.

Furthermore, this technique of extraction suggests that if we want to increase the memory performance, we must guarantee the flat band condition in the bridge (apply a bias $V_b \neq 0$ V). To further document this observation, on Fig.13-a we apply the pattern of drain bias (V_d) and gate bias (V_g) used for memory characterization. They are composed of: an erasing phase (E) to initialize the memory state, followed by the '1' state writing phase (W), then the '1' state reading phase (R_I1), the '0' state writing phase (E), and the '0' state reading phase (R_I0). Between each phase, there is a holding state (H). Fig.13-b reports the drain current versus the time during the bias sequence of Fig.13-a at two different V_b on Die 01 (Table I, with $L_g = 100$ nm and $W = 10 \mu\text{m}$). We can notice that I1 is increased by a factor of 5 when $V_b = 500$ mV while I0 (the '0' state reading current) remains at the same very low value.

IV. CONCLUSION

In this paper, we have developed an electrical characterization method to extract the doping profile in thin SOI films with special application to the A2RAM memory cell. This technique provides accurate results for bridge doping higher than 10^{18} cm^{-3} and bridge thickness larger than 20 nm. For low values of N_{bridge} and T_{bridge} , the accuracy can be enhanced by biasing the back gate. The extraction technique has been implemented on the samples fabricated in Leti [3] and the results agree with the ones shown in simulation. We have also evidenced the importance of this extraction technique in terms of memory optimization.

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REFERENCES

- [1] S. Okhonin, P. Fazan, and M.-E. Jones, "Zero Capacitor Embedded Memory Technology for System on Chip," 2005 IEEE International Workshop on Memory Technology, Design, and Testing (MTDT'05).
- [2] N. Rodríguez, S. Cristoloveanu, and F. Gámiz, "New concepts for 1T-DRAMs: overcoming the scaling limits," 978-1-61284-172-4/11/\$26.00 © 2011 IEEE.
- [3] N. Rodríguez, C. Navarro, F. Gámiz, F. Andrieu, O. Faynot, and S. Cristoloveanu, "Experimental demonstration of capacitorless A2RAM cells on silicon-on-insulator," IEEE Electron Device Letters, Vol. 33, No. 12, December 2012.
- [4] F. Tcheme Wakam, J. Lacord, M. Bawedin, S. Martinie, S. Cristoloveanu, and J.-Ch. Barbe, "Optimization guidelines of A2RAM cell performance through TCAD simulations," in SISPAD2017.
- [5] TCAD Sentaurus software – Synopsys vM-2016.12-SP1.
- [6] J. Maserjian, G. Petersson, and C. Svensson, "Saturation capacitance of thin oxide MOS structures and the effective surface density of states of silicon," Solid-State Electronics Vol. 17, pp. 335-339, 1974.
- [7] W. van Gelder, and E. H. Nicollian, "Silicon impurity distribution as revealed by pulsed MOS C-V measurements," Solid State Science January 1971.
- [8] S. Chattopadhyay, K. S. K. Kwa, S. H. Olsen, L. S. Driscoll, and A. G. O'Neill, "C-V characterization of strained Si/SiGe multipleheterojunction capacitors as a tool for heterojunction MOSFET channel design," Semicond. Sci. Technol. 18 (2003) 738–744.
- [9] S. Cristoloveanu, J-H Lee, and J. Pumfrey, "Profiling of inhomogeneous carrier transport properties with the influence of temperature in silicon-on-insulator films formed by oxygen implantation," J. Appl. Phys. 60, 3199 (1986).

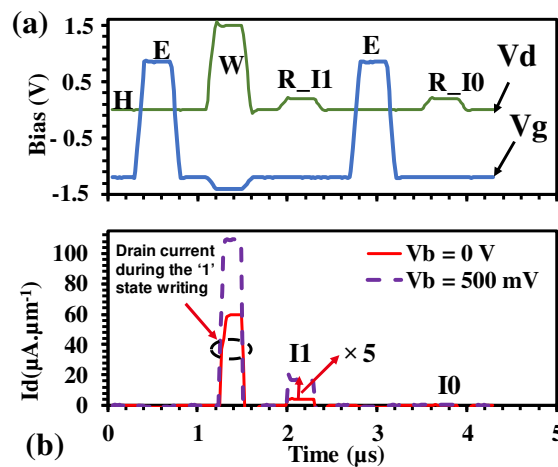


Figure 13. (a) Memory bias sequence used to the electrical characterization the die01 of Table I with gate length $L_g = 100 \text{ nm}$ and width $W = 10 \mu\text{m}$, (b) the drain current of die01 versus the time when we apply the bias sequence in Fig.13-a.