



A configurable operational amplifier based on oxide resistive RAMs

Hassen Aziza

► To cite this version:

Hassen Aziza. A configurable operational amplifier based on oxide resistive RAMs. 2018 13th International Conference on Design & Technology of Integrated Systems In Nanoscale Era (DTIS), Apr 2018, Taormina, France. pp.1-2, <10.1109/DTIS.2018.8368572>. <hal-02314659>

HAL Id: hal-02314659

<https://hal.science/hal-02314659v1>

Submitted on 13 Oct 2019

HAL is a multi-disciplinary open access archive for the deposit and dissemination of scientific research documents, whether they are published or not. The documents may come from teaching and research institutions in France or abroad, or from public or private research centers.

L'archive ouverte pluridisciplinaire **HAL**, est destinée au dépôt et à la diffusion de documents scientifiques de niveau recherche, publiés ou non, émanant des établissements d'enseignement et de recherche français ou étrangers, des laboratoires publics ou privés.



HAL Authorization

A Configurable Operational Amplifier based on Oxide Resistive RAMs

H. Aziza, C. Dufaza, A. Perez

Aix Marseille Univ, Université de Toulon, CNRS, IM2NP, Marseille, France

Hassen.aziza@univ-amu.fr, Tel: +33 491 054 782; Fax: +33 491 054 790

Abstract— This paper proposes a memristor-based operational amplifier design in which semiconductor resistors are suppressed and replaced by memristors. Such design is developed based on a calibrated memristor model, and offers dynamic configurability to realize different gains at reduced chip area.

Keywords— Memristor; opamps ; RRAM; analog calibration.

I. INTRODUCTION

Emerging technologies such as Resistive RAMs (RRAMs) are attracting significant attention, due to their interesting characteristics such as high integration density, CMOS compatibility and non-volatility to replace the current conventional memories [1] [2]. A recent advance in the field of RRAM memories is related to Multi Level Cell operation (MLC) [3]. According to this approach, more than two data states are made possible for each memory cell, simply by finely controlling the programming of the cell. The proposed memristor-based operational amplifier (OpAmp) uses RRAM cells as analog programmable devices by exploiting all the resistance states of the memory cell (i.e. extension of the MLC approach). High voltages are used to program the RRAM states during the OpAmp calibration and low voltages are applied across the RRAM cell during OpAmp operation. Thus, the state of the RRAM cell does not change during the OpAmp operation.

The approach to use memristors in programmable analog circuits was suggested in [4] and [5]. However, the approach was too conceptual and far from actual memristive device implementations. In [6], an ultra-low power open-loop OpAmp was designed using a memristor-based compensation technique. Also in this case, no references to actual memristive devices was provided.

In this work, a configurable close-loop operational amplifier is developed based on 130nm High Voltage technology from ST-Microelectronics and an Oxide-based RAM (OxRAM) model calibrated on silicon [7][8][9]. Before its integration in operational amplifiers, the analog storage feature of the OxRAM cell is evaluated based on actual data.

The paper is organized as follows: Section II presents the configurable OpAmp topology. Section III is dedicated to simulation results. Finally, section IV gives some concluding remarks.

II. CONFIGURABLE OPAMP TOPOLOGY

A. OxRAM operation as a programmable analog device

In operating conditions, after an initial electroforming process, the OxRAM element can be reversibly switched between a High Resistance State (HRS or OFF state) after a RESET operation and a Low Resistance State (LRS or ON state) after a SET operation. The ElectroFORMING operation, achieved one time in the OxRAM device life is a voltage-induced resistance switching from an initial virgin state with a very high resistance to a conductive state. In Fig.1a, an OxRAM I-V characteristic is presented. The resistance change is triggered when the voltage difference across the TOP and BOTTOM electrode of the cell (labeled respectively “T” et “B” in Fig.1b) reaches specific voltages (namely V_{RES} and V_{SET}). To obtain intermediate ON and OFF states, programming can be done gradually by applying an increasing number of voltage pulses.

To monitor the variation of the analog resistance, an analysis of the cell resistance variation after FORMING is performed. The memory cell is formed gradually by applying a series of short programming pulses across the cell. The number of pulses is controlled by a programmable pulse generator. The pulse width is set to 50 ns within a period of 100 ns and the pulse level is set to 3 V. As a result, the resistance of cell decreases.

Fig. 2.a presents the evolution of the HRS resistance versus the number of pulses. Fig. 2.b presents the LRS resistance versus the number of pulses. The resistive switching from HRS to LRS occurs at cycle number 40. HRS resistance variations are in the $M\Omega$ range [$15M\Omega$ - $156k\Omega$] and LRS resistance variations are in the $100\ \Omega$ range [955Ω - 500Ω]. The abrupt change of the resistance (at cycle number 40) is a rapid phenomenon preventing the use of this area for resistance calibration purposes. In contrast, HRS and LRS resistance variations exhibit two interesting areas suitable for analog calibration (between programming cycles 14 and 40 for the HRS resistance and between cycles 45 and 200 for the LRS resistance).

B. OxRAM based closed-loop amplifier

A CMOS closed-loop inverting OpAmp configuration is built and presented in Fig. 3a. The feedback resistance R2 and the input resistance R1 are replaced by OxRAM cells. In OpAmp normal operation mode, OxRAM cells behave as conventional resistances, and voltages across the cells are always below the OxRAM programming voltages ($\sim 3V$). Indeed, the input voltage is meant to be low and the OpAmp output swing voltage is limited to 0.9V far from the programming voltage. The OpAmp including its programming interface is presented in Fig. 3b. In OpAmp calibration mode, the programming interface is activated when the EN signal is set High. In the same time transmission gates S1 and S2 disconnect the OpAmp output and isolate the OpAmp input from the rest of the circuit. Then, SET and RESET pulses are applied across the cell through the 3-state buffers in order to program dynamically and independently each OxRAM cell. Table II presents the different voltage levels to apply across R1 and R2 OxRAM cells to perform “soft” SET/RESET operations. Note that the OxRAM bottom electrode B is shared between R1 and R2 allowing the use of only one RESET signal.

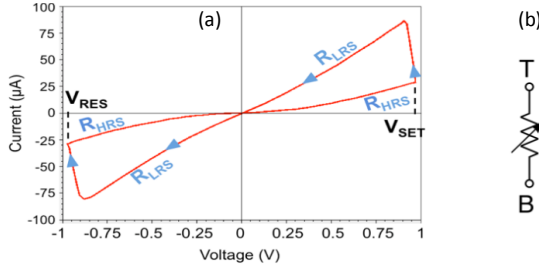


Fig. 1. (a) OxRAM I-V hysteresis and (b) OxRAM cell symbol.

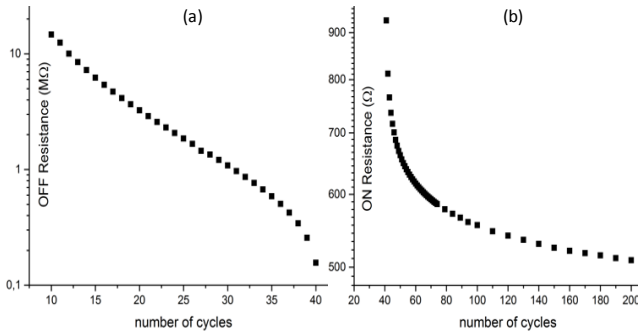


Fig. 2. (a) HRS and (b) LRS resistance variation versus pulse numbers.

III. SIMULATION RESULTS AND ANALYSIS

According to Fig.2, HRS resistance variation is in the $M\Omega$ range [$15M\Omega$ - $156k\Omega$] and LRS resistance variation is in the range [955Ω - 500Ω]. The gain of the open-loop OpAmp presented in Fig.4 is equal to $-R2/R1$. Thereby, the gain of the OpAmp can be adjusted dynamically after changing R1 and R2 resistance states. As an application example, let's consider configuration 3 of Table II. In this configuration, R1 and R2 are reset to $250k\Omega$ after applying a series of 39 programming pulses across both OxRAM cells (see Fig.2a). As expected, a

unity gain is provided by the OpAmp. Then, only R1 is set to 662Ω after 50 programming cycles according to configuration 2 of Table II (see Fig.2b). A new gain equals to 377 is now provided by the OpAmp. This gain can be increased dynamically by increasing the number of pulses applied across R1. Fig. 4 presents the evolution of the OpAmp gain versus the number of pulses. The gain variation is in the range [377 - 490].

IV. CONCLUSION

Benefits of the presented methodology are related to the suppression of semiconductor resistances usually implemented in a closed-loop OpAmp topology. Moreover, an in-circuit resistance calibration feature is provided.

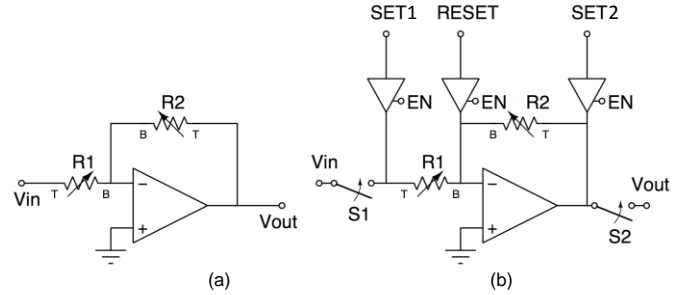


Fig. 3. (a) OxRAM-based inverting OpAmp (b) OxRAM-based inverting OpAmp including the programming interface.

TABLE I. SET/RESET LEVELS

OxRAM input signals ^b			^b $H = 3V$ $L = 0V$	
SET1	RESET	SET2	OxRAM states	# Configuration
L	L	L	no effect	1
L	L	H	R2 SET	2
L	H	L	R1 & R2 RESET	3
L	H	H	R1 RESET	4
H	L	L	R1 SET	5
H	L	H	R1 & R2 SET	6
H	H	L	R2 RESET	7
H	H	H	no effect	8

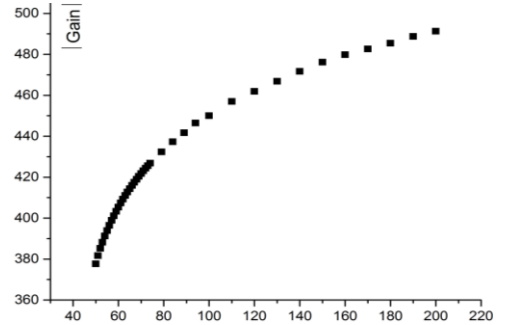


Fig. 4. OpAmp gain ($|-R2/R1|$) versus pulse number applied across R1.

REFERENCES

- [1] E. Shahrabi et al., “Towards chip-level reram-cmos co-integration”, MEMRYSIS, pp 1-5, 2017.
- [2] S. Hamdioui et al., “Memristor based memories: Technology, design and test”, DTIS Conf., pp 1-7, 2014.
- [3] H. Aziza et al., “Multilevel operation in oxide based resistive RAM with SET voltage modulation”, DTIS Conf., pp 1-5, 2016.
- [4] Y. V. Pershin, M. Di Ventra, “Practical approach to programmable analog circuits with memristors”, IEEE TCAS, 57(8), 1857-1864, 2010.

- [5] T. Ibrayev et al., "Memristive Operational Amplifiers", *Procedia Computer Science*, 41, pp. 114-119, 2014.
- [6] M. R. Jahromi et al., "Ultra-low power Op-Amp design with memristor-based compensation", *CCECE Conf.*, pp. 1-4, 2017.
- [7] M. Bocquet et al., "Robust compact model for bipolar oxide-based resistive switching memories", *T-ED*, 61.3, pp. 674-681, 2014.
- [8] B. Hajri et al., "Oxide-based RRAM models for circuit designers: A comparative analysis", *DTIS Conf.*, pp. 1-6, 2017.
- [9] H. Aziza et al., "Evaluation of OxRAM cell variability impact on memory performances through electrical simulations", *NVMTS Conf.*, 2011.