Digital RF Transmitter With Single-Bit ΔΣM-Driven Switched-Capacitor RF DAC and Embedded Band Filter in 28nm FD-SOI

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***Abstract*—This paper presents a single-bit RF transmitter based on single-bit switched-capacitor RF digital-to-analog converters (DAC) embedded in an FIR filter (FIR-DAC). The transmitter system comprises a single-bit quadrature Delta-Sigma Modulator (ΔΣM), a digital mixer, and a 109-tap RF FIR-DAC stage with a single external inductor, combining D-A conversion with discrete and continuous time filtering. The on-chip part of the FIR-DAC is built exclusively with CMOS inverters and Metal-Oxide-Metal (MOM) capacitors, which are implemented in the interconnect layers to propose a compact fully-digital solution, suitable for advanced CMOS nodes. A method for canceling redundant switching in the FIR-DAC is proposed to reduce its complexity and power consumption. Combining discrete and continuous-time filtering, the out-of-band quantization noise of the 1-bit RF signal is strongly attenuated below the level required by emission masks. The RF FIR-DAC prototype is implemented in 28nm FD-SOI CMOS technology with 10 metal layers and occupies a total active area of only 0.047 mm^2. The overall power consumption is 38 mW at 4.6 dBm peak output power, 900 MHz carrier frequency and 1 V supply. FD-SOI body-bias Vt tuning is used to effectively correct mixing clock duty-cycle errors in order to perform precise high-frequency I/Q interleaving, which enables high image and local oscillator (LO) rejections. The resulting power consumption, surface and performance of the measured prototype make the proposed circuits and concepts particularly appropriate for use in emerging Internet of Things (IoT) applications.**

***Index Terms*—All-digital transmitter, body-bias, Delta-Sigma modulation (ΔΣM), finite impulse response filter (FIR), FIR-DAC, switched-capacitor (SC) DAC, 28nm FD-SOI.**

I. Introduction

CONSTANT technology downscaling drives the transition from analog to digital-intensive transmitters for integrated mobile devices developed to support emerging Internet of Things (IoT) applications [1]. Recent research concentrates on the complete System-on-Chip (SoC) implementation of the transmit chain, as well as pushing the digital signal processing domain boundary closer to the antenna.

The main challenges specific to digital transmitter design are to reduce quantization noise below spectrum mask requirements, to achieve power consumption levels similar or below analog/RF transmitters and to reach carrier frequencies in the GHz range. Proposed approaches in literature range from high-resolution high-speed digital-to-analog converters (DAC) to single-bit Delta-Sigma modulated digital RF signals at multi-GHz clock rates.

A. Speed vs. resolution trade-off in digital transmitters

Various trade-offs between resolution and clock rates have been used in digital to RF conversion (DRFC) approaches, embedding the DAC into the baseband to RF mixer. Examples are the 6-bit switched-capacitor (SC) I/Q sharing DRFC structure in [2] or the 13-bit RF power DAC in [3], which present significant conceptual differences, since [2] optimizes power efficiency using a low-resolution scheme, and [3] targets improved noise performance thanks to additional resolution and digital pre-distortion. In [4], a 10-bit current-steering DAC is demonstrated and digital Delta-Sigma Modulators (ΔΣM) with mismatch shaping (MS) are used to reduce OOB emissions at a programmable duplex distance. Similarly, a 12-bit resistive quadrature DAC (RQDAC) is presented in [5] with incremental-charge based operation to reduce the power consumption required to drive the RF load.

Low-resolution ΔΣM-based architectures [6], [7] have the potential to achieve excellent in-band performance and be efficiently integrated in CMOS technologies. On the one hand, the architecture in [6] introduces a 4-bit ΔΣM driving a 1-bit pulse width modulator (PWM), which enables the use of an efficient class-G switched-capacitor PA, similar to [8]. On the other hand, in [7] an all-digital RF signal generator is designed based on single-bit low-pass ΔΣMs and a simplified digital mixer, thus opening the way towards the implementation of an all-digital transmitter scheme based on switching-mode (SM) power amplifier (PA).

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B. *Known filtering techniques*

One solution to reduce out-of-band quantization noise is to introduce highly selective analog filtering. Bulk acoustic wave (BAW) filters have been developed for mobile RF-front-ends with significantly higher quality factors (Q up to 1000) than on-chip *LC* tanks, better temperature stability and power handling capability compared to surface acoustic wave (SAW) devices, and the potential to be fabricated in above-IC approach [9]. However, manufacturing cost and yield issues have so far limited above-IC integration at an industrial scale.

Semi-digital solutions based on finite impulse response (FIR) filters represent another attractive approach, thanks to the possibility of digitally adjusting the transfer function. In [10], a parallel DRFC structure is introduced to create a 2-tap FIR filter with two notches at ±500 MHz from the 2.45 GHz center frequency. A 5-channel power combiner based on transmission lines was proposed in [11], allowing a digitally reconfigurable RF FIR filter with binary coefficients. A similar approach was used in [12], integrating a power combiner using on-chip transformers in a 3-tap FIR configuration. The measured noise floor is -149 dBc/Hz in a selected 20 MHz band, whereas the 3.4 Ω output resistance enables 30 dBm peak output power. In addition, a 6-tap FIR-DAC is introduced in [13] based on 1-bit band-pass (BPF) ΔΣ-DAC and a current-steering FIR reconstruction filter with programmable zero location based on 6-tap digital delay line. These FIR-based quantization noise filtering techniques propose to create notches in the OOB noise spectrum using few taps for the filtering function. To provide a global out-of-band attenuation over the complete spectrum, [14] suggested a 63-tap semi-digital FIR-DAC in a differential current-steering architecture targeting 60 dB stopband attenuation for 802.11 ac/ad signals.

In this paper, a low-power 109-tap RF FIR-DAC taking advantage of a switched-capacitor structure designed for single-bit ΔΣ RF signals is presented. Section II describes the theory of the digital transmit chain and the study of the FIR-DAC non-idealities model. Next, Section III details the 28nm FD-SOI CMOS circuit implementation, emphasizing the integration of the FIR-DAC under a signal pad. The proposed concept is validated with measurement results in Section IV, and Section V concludes this paper.

II. Theory of Operation

The proposed all-digital RF transmitter architecture is shown in Fig. 1. It comprises two quadrature 1-bit 3rd order ΔΣMs, working synchronously at twice the carrier frequency (f_c), a digital mixer (DRFM) producing a digital RF signal at the final sample rate of $4*f_c$, a pseudo-differential RF DAC with embedded FIR filtering, and an *RLC* band-pass filter.

The digital mixing process is simplified by setting the sampling frequency to $f_s = 4*f_c$ [7], allowing the cosine and sine versions of the LO signal period to be expressed as simple sequences, namely {1; 0; -1; 0} and {0; 1; 0; -1}. In this case, one out of two values in the I and Q paths can be dropped. Thus, the mixer is reduced to time-interleaving the appropriate

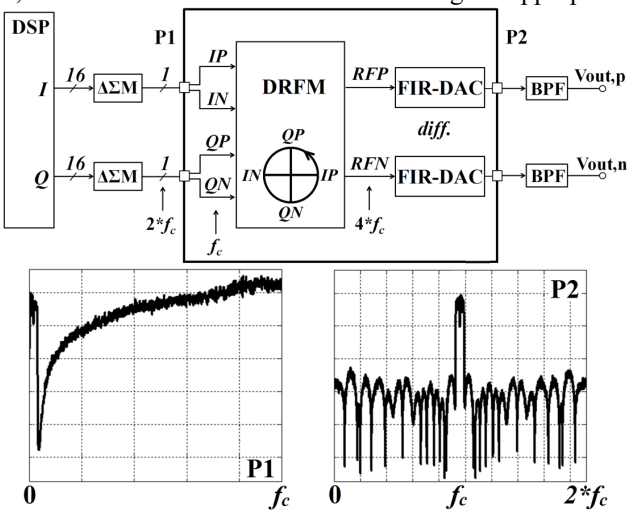


Fig. 1. Proposed all-digital RF transmitter architecture and conceptual representation of the 1-bit digital input signal spectrum and the analog output signal spectrum of the transmitter.

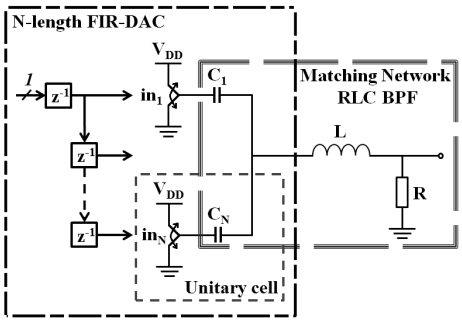


Fig. 2. Conceptual view of the proposed N-length FIR-DAC.

I and Q path samples with positive (*IP*/*QP*) or negative (*IN*/*QN*) polarity. The resulting mixer output over one LO period can be represented by the sequence {*IP*; *QP*; *IN*; *QN*} at the sampling frequency $4*f_c$. Hence, by generating only the useful I and Q samples, the effective sampling rate of the ΔΣM stage can be reduced to $2*f_c$. Additionally, time interleaving of the ΔΣMs enables multi-GHz carrier frequency operation, as shown in [15].

Furthermore, the constant-level switching at the output of the ΔΣM allows the implementation of N 1-bit switched-capacitor DACs, which are recombined to form an FIR filter. The FIR filter function is embedded into the DAC by introducing delays between N successive driver/capacitor sections, which correspond to N delayed versions of the single-bit ΔΣM output (Fig. 2). Relative sizes of capacitors are used to implement arbitrary coefficients in the FIR filter, which has linear phase, thanks to the symmetrical capacitor ratios, i.e. $C_i = C_{N-i+1}$, where $i = 1 \ldots N/2$.

Combinations of elementary DAC cells can be used to create programmable coefficients of an N-tap digital FIR filter, embedded in the DAC stage. With respect to its current-source counterpart, the SC scheme has the advantages that it does not require stringent transistor matching and has constant

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impedance seen from the output. Furthermore, in a switched-capacitor DAC, signals can be combined on an inductor in series with the load [16]. The total DAC capacitance and the inductor form the *LC* matching network to the load resistance, where *L* and *C* are tuned to resonate at the carrier frequency. The band-pass filter created around f_c contributes to quantization noise filtering, thus being highly useful in relaxing the design constraints of the FIR filter.

A. FIR filter design optimization

In a conventional DAC, the number of bits is set according to the target minimum noise floor, even though the OOB noise requirements are not uniform over the entire spectrum. To avoid overdesign, a configurable FIR filter is used to i) set a lower overall target noise rejection of 70 dBc, and ii) adjust the zeros placement to target 80 dBc noise rejection only at specific frequency bands for multi-standard coexistence. We note that 80 dBc corresponds approximately to the thermal noise floor, when considering a 20 MHz channel bandwidth, a succeeding power amplifier with an average output power of 20 dBm, and 40 dB isolation from antenna to antenna [17].

The FIR filter was designed in MATLAB using a window method, i.e. convolution in frequency domain between the ideal impulse response filter and a window function to derive a finite impulse response filter. Different types of integration windows (same conditions on filter length and coefficient quantization) were evaluated, in order to obtain a trade-off between near-band and far-out-of-band noise attenuation. The ΔΣM is designed according to [15] as a single-bit 3rd order CIFB (Cascade-of-integrators feedback form) with quantized coefficients and OSR (oversampling ratio) of 100, resulting in a peak SNR (signal to noise ratio) of ~90 dB, and requires extensive filtering of the quantization noise, as shown in Fig. 3(a). The required performance can be achieved by an FIR filter using a Hann window [18] with 109 symmetric coefficients quantized to 8 bits. The total number of unitary filter taps, i.e. DAC cells, is estimated by summing the 109 quantized coefficients (lowest is 1, largest is 256), which adds up to ~14500. Hence, building such a filter is not physically feasible, as it would produce a tremendous overhead in wiring, which will negatively impact electrical performance.

The first optimization step is to co-design the FIR filter together with the output *RLC* band-pass filter (Fig. 3(b)). By relaxing the filtering constraints, the resolution of the FIR coefficients can be reduced to 5 bits (largest is 32), which lowers complexity by 8 times (1800 total unitary cells), and facilitates integration in advanced CMOS technology nodes.

B. FIR-DAC architecture optimization

The second optimization step addresses the optimization of the switched-capacitor scheme, by reducing switching redundancy and power consumption

$$P_{SC} = \alpha_{SC} \cdot C_T \cdot V_{DD}^2 \cdot f_s \tag{1}$$

where the factor α_{SC} represents the contribution of the single-bit ΔΣM (driving *N* delayed paths of the FIR-DAC) switching activity to the average dissipated energy, C_T is the total output node capacitance, V_{DD} the supply voltage, and f_s the sampling frequency, respectively.

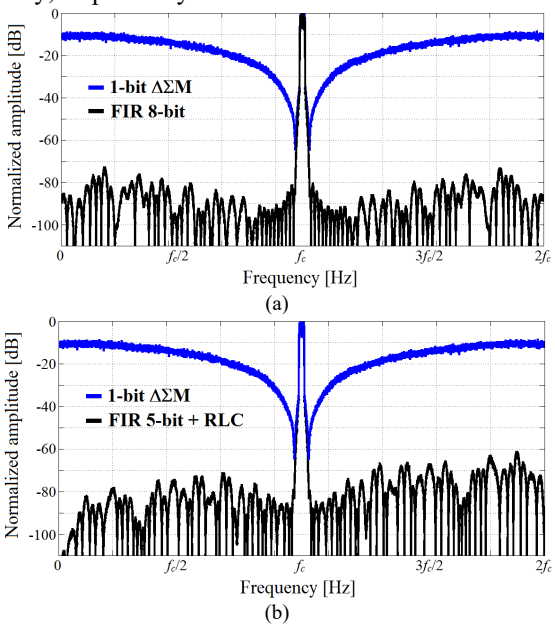


Fig. 3. Output spectrum: (a), (b) 1-bit ΔΣM; (a) FIR with 8-bit coefficient quantization; (b) FIR with 5-bit coefficient quantization and *RLC* filter.

Let us consider the differential FIR-DAC structure in Fig. 4(a). Taking into account that during fast transitions the inductor can be seen as an open circuit, we identify that when the digital inputs in_k and in_{N-k+1} to symmetric FIR coefficients ($C_k = C_{N-k+1}$) have opposite values, the resulting contribution on the differential output is zero. Switching redundancy is cancelled by introducing AND/NOR gates on the positive/ negative sides of the FIR-DAC, which allows an estimated switching activity reduction of ~20%.

Therefore, the FIR-DAC driving signals for k = 1..54 and $m = N/2 + 1 = 55$ are:

$$\begin{cases} RFP_k = RFP_{N-k+1} = in_k \ AND \ in_{N-k+1} & RFP_m = in_m \\ RFN_k = RFN_{N-k+1} = in_k \ NOR \ in_{N-k+1} & RFN_m = \overline{in_m} \end{cases} \tag{2}$$

Now, both symmetric coefficients and corresponding driving signals are equivalent. As a result, the symmetric sides become redundant and one side of the filter is simply removed (Fig. 4(b)). Though it is a classic technique in digital FIR filter design, it is the first time it has been applied to FIR-DAC design, being driven by the need to implement a very large number of FIR coefficients.

Hence, 109-tap FIR filter performance can be achieved using only half the filter coefficients, namely 55 out of 109, whereas the coefficients $C_{1..54}$ keep their initial value and the middle non-symmetric coefficient C_{55} is halved. In practice, this translates to the digital signal processing of 109 consecutive samples, to obtain 55 signal streams $RF_{1..55}$ which drive 55 DAC cell groups. With respect to the straight-forward approach, the FIR complexity is reduced by 16 times in terms of total number of cells, and 2 times in terms of number of signal streams for similar OOB noise performance. Thus, for a

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constant unitary capacitance, the inductance value is doubled to maintain the same resonance frequency of the *LC* network

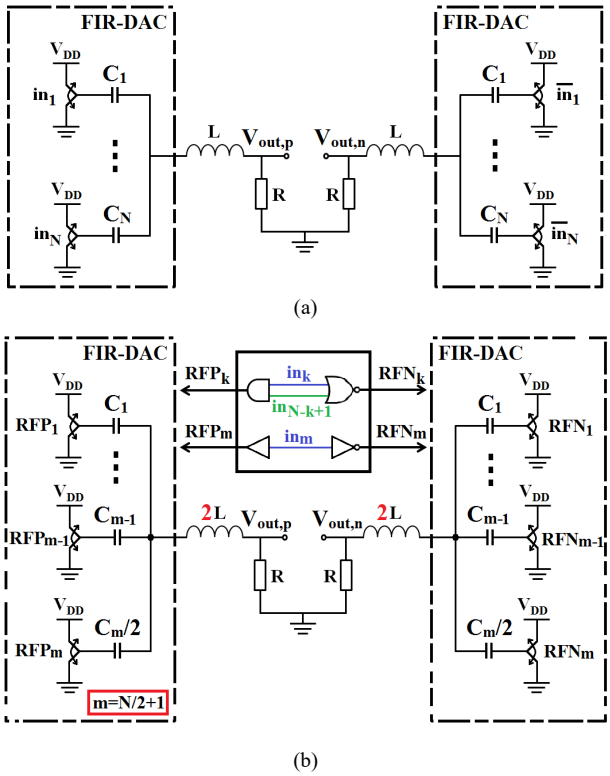


Fig. 4. Differential FIR-DAC: (a) conventional; (b) optimized with reduced switching activity and number of unitary cells.

(the total output node capacitance is halved), which also changes the *RLC* quality factor. Moreover, the three remaining possible combinations of positive and negative driving signals, *RFP/RFN* = {1/0; 0/0; 0/1}, result in a pseudo-differential configuration, which might cause increased even-order harmonics due to non-ideal differential to single-ended conversion. Finally, the key advantage of the proposed architecture is that it combines the increased output power of the differential architecture with the performance of the single-ended architecture in terms of switching power, area, number of unitary cells and input signal drivers.

C. *FIR-DAC switching model*

A comprehensive study of the switching model for switched-capacitor PA schemes is shown in [16], where the unitary PA cells are activated based on the input signal amplitude during the first half-period, whereas in the second half, all the cells are switched-off, so that the switching power does not depend on the cell switching transitions. However, in the proposed architecture (Fig. 4), the unitary cells are de-/activated during a complete time period, based on the control signals derived in the FIR filter, meaning that the switching scheme model has to take into consideration also the previous state (on/off) of the cells (transitions). To evaluate the average switching power, the simplified switching model in Fig. 5 is considered at the switching instants t_0 and t_1. The capacitances are denoted C_{ij}, where the first index i corresponds to the connection of the bottom plate at time t_0, and the second index j corresponds to time t_1 ("1" denotes V_{DD} and "0" denotes *GND*). The output voltages V_0 and V_1 at time instants t_0 and t_1

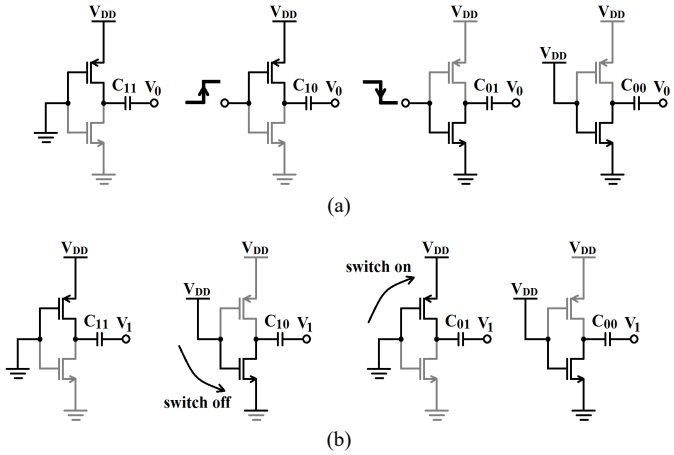


Fig. 5. 2-bit SC scheme: switching activity from time instant t_0 (a) to t_1 (b); On-transistors are depicted in black and off-transistors in grey.

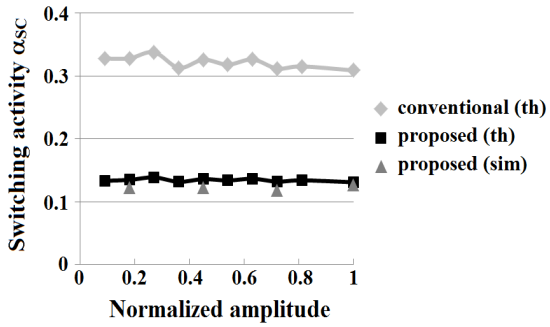


Fig. 6. Switching activity α_{SC} as function of the input signal amplitude; validation of the theoretical switching model by Spectre simulations.

are obtained from the ratio between switched-on capacitances and the total capacitance C_T times the supply voltage V_{DD}

$$\begin{cases} V_0 = \dfrac{C_{11}+C_{10}}{C_T}\cdot V_{DD} \\ V_1 = \dfrac{C_{11}+C_{01}}{C_T}\cdot V_{DD} \end{cases} \tag{3}$$

The average switching power P_{SC} can be expressed as the total energy E_x spent during N_P periods divided by the number of periods N_P and the sampling period $T_s = 1/(4*f_c)$

$$P_{SC} = \frac{1}{N_P \cdot T_s}\cdot \sum_{i=1}^{N_P} E_{x,i} \tag{4}$$

Combining (1) and (4), the average switching activity α_{SC} is computed with the voltage drop difference on C_{ij}

$$\alpha_{SC} = \frac{\sum_{i=1}^{N_P} \alpha_{10,i}\cdot(\alpha_{01,i}+\alpha_{11,i}) + \alpha_{01,i}\cdot(\alpha_{10,i}+\alpha_{00,i})}{N_P} \tag{5}$$

where all the capacitances C_{ij} are normalized to the total capacitance C_T, namely $\alpha_{ij} = C_{ij} / C_T$.

Hence, considering (5), the power consumption is reduced

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by ~60% in the case of the proposed FIR-DAC (Fig. 4(b)), with respect to the conventional scheme (Fig. 4(a)) for the same OOB noise performance, thanks to optimized switching (20%), and architecture simplification (50%).

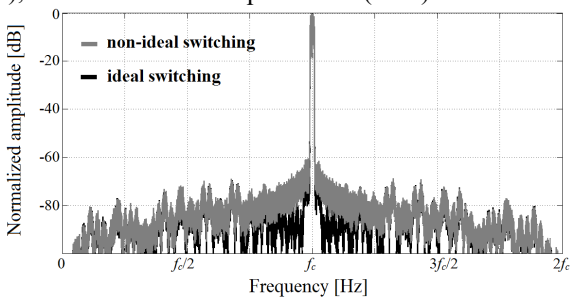


Fig. 7. Output spectrum: ideal and non-ideal switching – $\sigma_{tr/tf} = 0.5\% \cdot T_s$, $\sigma_{PLH/PHL} = 0.5\% \cdot T_s$, $\sigma_{j,var} = 1\% \cdot T_s$. $\sigma_{j,var} \approx 2.8$ ps when $f_c = 900$ MHz.

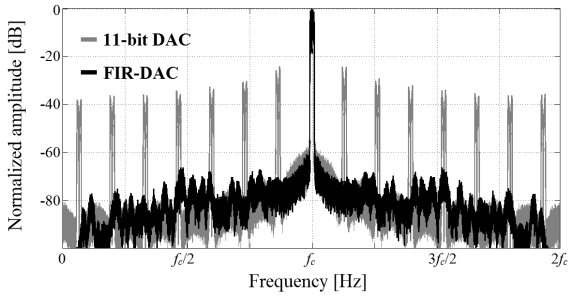


Fig. 8. Output spectrum: coefficient mismatch - standard deviation 10%; Comparison with 11-bit RF DAC with ideal upconversion.

This is highlighted in Fig. 6, in addition to the validation of the switching model combining (1) and (5) using behavioral Spectre RF simulations. We may remark that the switching activity is almost independent of the input signal amplitude (before DSM). Furthermore, generating only 55 out of 109 signal streams leads to a significant reduction of complexity and power consumption of the FIR-DAC driving circuit.

D. FIR-DAC non-idealities model

In this section, a model for the unitary DAC cell non-idealities is proposed and the impact of circuit integration on the FIR filter function is evaluated. First, the switch driving signals *RFP/RFN* are subject to non-idealities due to rise/fall time (t_r/t_f), propagation delays (t_{PLH}/t_{PHL}) and jitter ($t_{j,var}$). We assume that all parameters are specific to each path and normally distributed, with Δt_r, Δt_f, Δt_{PLH}, and Δt_{PHL} constant throughout simulation, and variable cycle-to-cycle $t_{j,var}$. System-level simulations reveal that jitter causes the main noise performance degradation, rendering part of the FIR filter zeros indistinct compared to the ideal case. Still, when considering the combined switching non-idealities (Fig. 7), we remark that the noise level near the signal-band is lower than in the case of jitter only, which may be accounted for by a slight cancellation effect between the variable propagation delay and jitter which lowers overall deviation.

A different source of non-ideality arises from the matching errors of the unitary capacitances, which directly impacts the FIR filter coefficients and transfer function (Fig. 8). It is seen that for large deviations, the proposed FIR-DAC can achieve a noise attenuation performance similar to a conventional 11-bit RF DAC at specific critical bands. Also, the proposed scheme does not create additional signal images, like in an RF DAC [19], where a trade-off is made to reduce baseband sampling

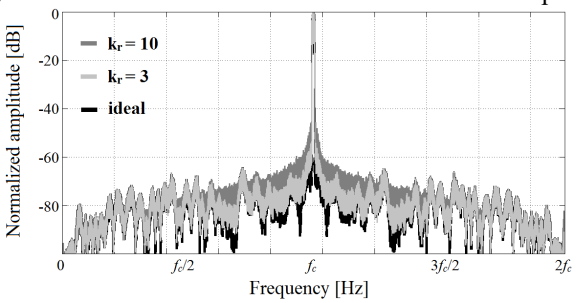


Fig. 9. Output spectrum: effect of voltage supply variation with respect to the tolerated supply resistance k_r.

frequency and power consumption. The 11-bit RF DAC is modelled as in [19], with 1/3 of the total number of bits binary and 2/3 thermometer coded, respectively.

Moreover, the variation of the voltage supply has a significant impact on both switching and coefficient non-idealities (Fig. 9), because it is mainly dependent on the cycle-to-cycle switching current I_{SC} and it may become critical in high-frequency switching schemes. The supply variation is defined here as $\Delta V_{DD} = k_r \cdot I_{SC}$, where k_r is used to derive the tolerated supply resistance for the filter transfer function. We note that an increase of k_r determines a gradual degradation of the near-band noise performance.

Finally, the signal-band performance of the proposed FIR-DAC is evaluated in the presence of non-idealities, showing very good EVM (error vector magnitude) performance, when applying static correction of the I/Q constellation similar to [20]. In the case of an orthogonal frequency-division multiplexing (OFDM) 20 MHz 16QAM (quadrature amplitude modulation) signal, the resulting rms EVM of the transmit chain is close to 1.5%.

III. Circuit Description

A top-level schematic of the proposed digital RF transmit chain is presented in Fig. 10. The digital inputs *DSI* and *DSQ* are single-bit ΔΣ modulated signals generated externally, and a serial-to-parallel (S/P) converter was inserted to reduce digital core operating frequency, leading to a 4-phase system configuration on both *I* and *Q* paths at a sample rate $f_c/2$. The FIR-DAC SIGGEN blocks generate the baseband level delayed control signal groups, in the I and Q paths, for the 55 switching blocks of the FIR-DAC. Finally, the groups are processed by digital RF mixers (DRFM), which work as interconnection matrixes to derive the digital streams at $4*f_c$, namely *RFP* = {*IP1*, *QP1*, *IP2*, *QP2*, *IP3*, *QP3*, *IP4*, *QP4*}, and *RFN* = {*IN1*, *QN1*, *IN2*, *QN2*, *IN3*, *QN3*, *IN4*, *QN4*}, which drive the switching blocks of the positive and negative sides of the pseudo-differential FIR-DAC.

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A. Digital RF signal generation

The FIR-DAC SIGGEN block uses the output of a single-bit quadrature ΔΣM to provide the necessary signals that implement (2) to perform the FIR filter simplification. At the input, a shift register holds 112 consecutive samples $I/Q[1,\ldots,112]$ at each time period $(2/f_c)$.

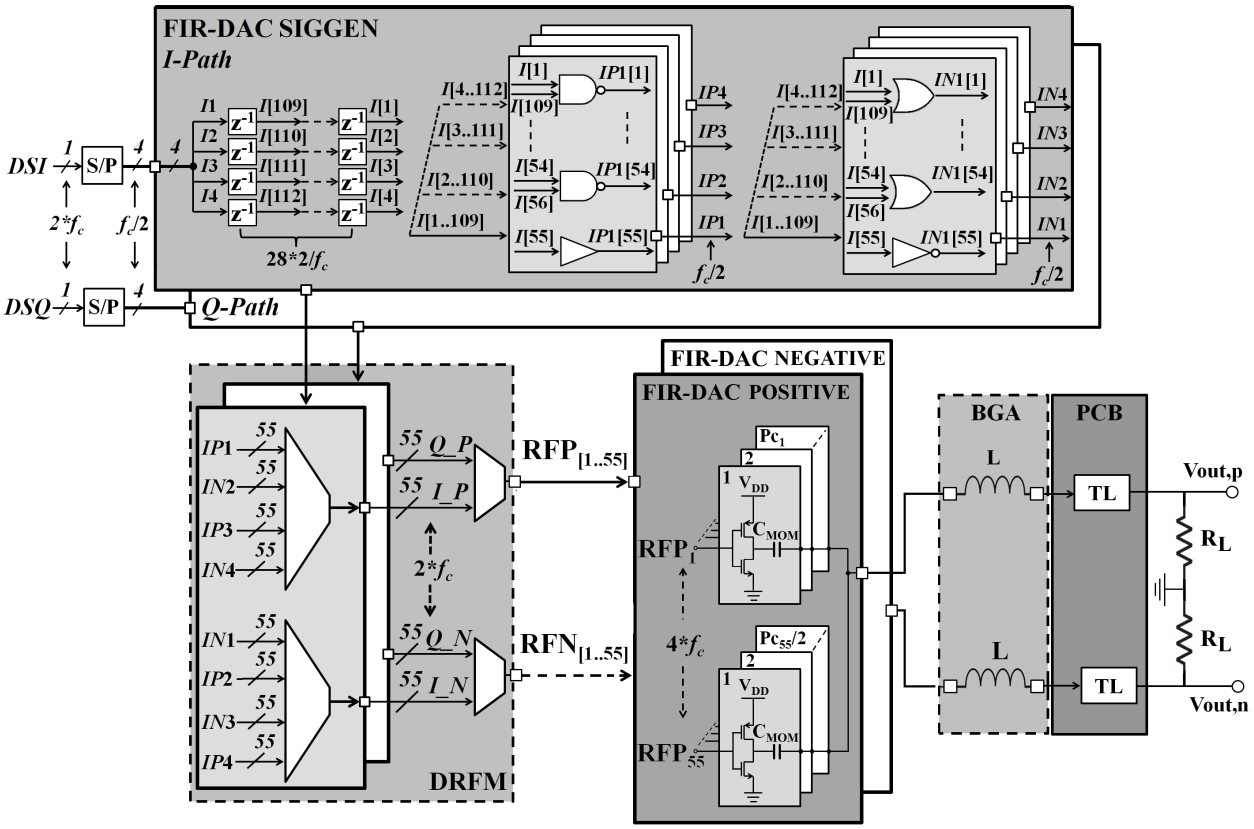


Fig. 10. All-digital RF transmit chain block diagram.

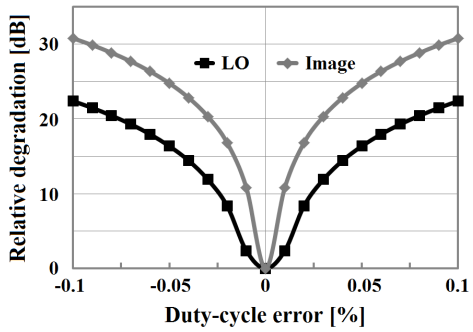


Fig. 11. Relative LO and image rejection degradation vs duty-cycle error

Furthermore, 4 groups of 55 signal streams per path (I/Q) and per side (positive/negative) are derived to drive the FIR-DAC. The DRFM block is implemented as a multiplexer (MUX) which reconstructs the RF signal streams $RFP/N_{1,\ldots,55}$ at $4*f_c$. Signal multiplexing is performed in two steps: 1) a 4:1 MUX driven by two clocks of frequency $f_c/2$ and f_c, which creates the signals for the I and Q paths on the positive and negative sides at $2*f_c$, followed by 2) a 2:1 MUX driven by the main clock of frequency $2*f_c$, which interleaves the I and Q paths. Normally, the mixing process would require high frequency signal sampling at $2*f_c$ (first step) and $4*f_c$ (second step) for precise I/Q interleaving. Instead, we propose to use the FD-SOI body-bias V_t tuning feature [21] in the DRFM to adjust digital clock tree switching (equalize rise/fall times and propagation delays), and thus correct the clock duty-cycle errors (DCE) causing I/Q mismatch.

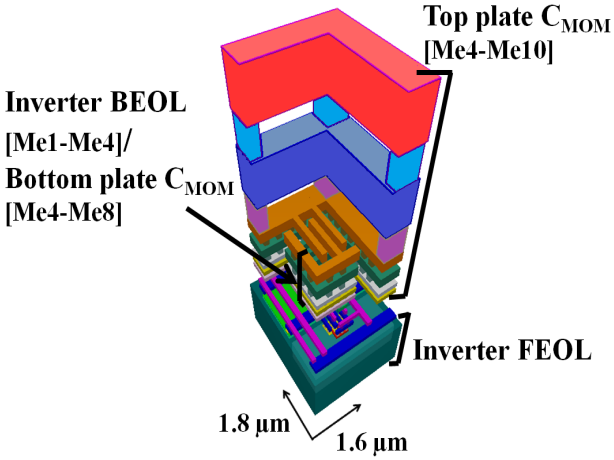


Fig. 12. Unitary cell 3D layout (3D GDSII Viewer).

System-level simulations showed that clock DCE determine an overall degradation of the noise performance (including image, LO, noise floor) in the first multiplexing

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step (separate I and Q paths) and introduce I/Q mismatch in the second multiplexing step (I/Q path interleaving), which mainly impacts the image rejection, as shown in Fig. 11 (for $\Delta_{DCE} = \pm 0.1\%$, where the duty cycle is $DC = 50\% + \Delta_{DCE}$). In addition, an interface buffer is included between the digital RF signal generator and the FIR-DAC, according to a theoretical estimation of the line load in each path and an RC extraction of the output stage.

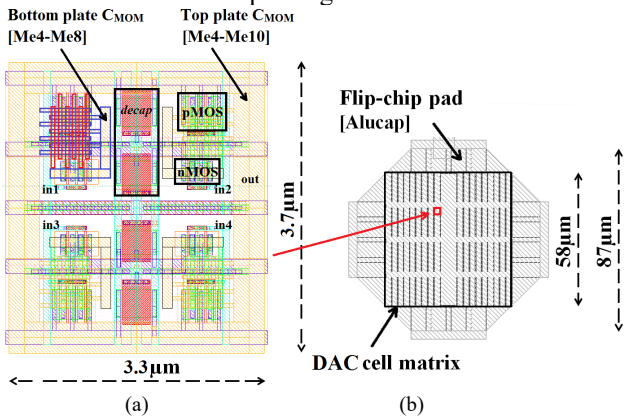


Fig. 13. (a) Group of 4 power cells; (b) DAC under FC pad.

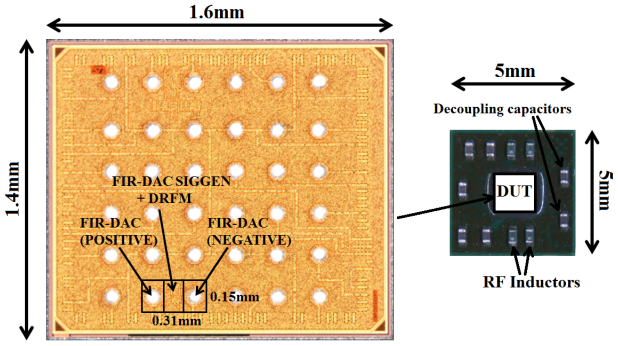


Fig. 14. Die micrograph and IC mounted flip-chip BGA package cavity. The cavity includes also SMD inductors and decoupling capacitors.

The complete design of the digital blocks was done based on VHDL/Verilog descriptions with digital synthesis tools, although some custom design was needed at the interface with the FIR-DAC. The simulated power consumption of the digital core is estimated at ~16 mW, when operating at a center frequency f_c = 0.9 GHz. Moreover, integrating the two ΔΣM would add ~6 mW power consumption, as described in [15].

B. FIR-DAC circuit design

The unitary cell of the FIR-DAC comprises a CMOS inverter and a metal-oxide-metal (MOM) capacitor, which were co-designed to enable a performance optimization in terms of power consumption and area, achieving ~1.4 μW per GHz switching frequency for an area of 1.6x1.8 μm^2. The integration of the complete FIR-DAC under flip-chip (FC) RF pads is achieved through a specific multi-layer structure in a 10 metal (Me) process (3D view in Fig. 12).

The CMOS inverter is built up to Me1, inter-/intra-cell connections on Me2 to Me4, and the MOM capacitor on Me4 up to Me8 ($C_{MOM} \approx 1.7$ fF), whereas the top-plates of the capacitors are connected together directly to the pad on Me10 and Alucap. Furthermore, in order to reduce layout-induced parasitic elements on the output, unit cells are grouped by 4, which presents the following advantages:

1) The ring provides isolation between the cell groups;
2) There is no inner-group ring, thus reducing the parasitic capacitance seen at the output terminal;
3) The free space can be used for supply decoupling.

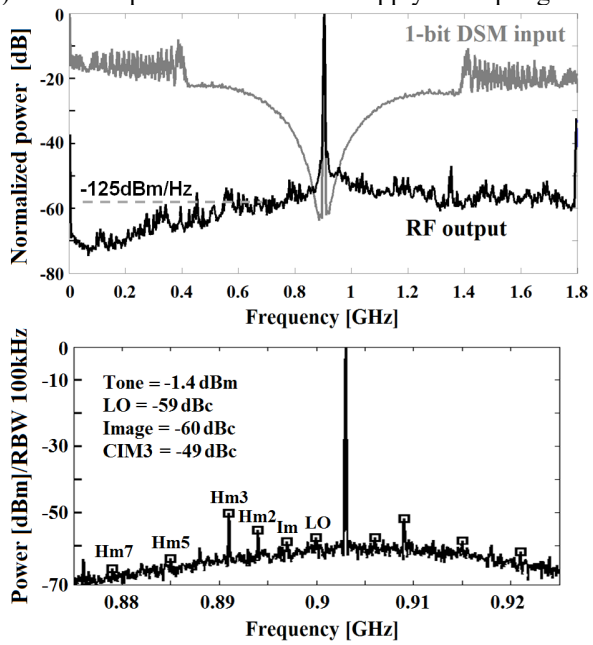


Fig. 15. Measured spectrum: 3 MHz single-tone at 6dB back-off.

The FIR-DAC has a total of 1152 unitary cells, divided into a 32 by 36 matrix to fit under the 58x58 μm^2 flip-chip pad (Fig. 13). Post-layout simulations of the FIR-DAC and the switching cells indicate a power consumption of 4 mW for the inverters and 2.5 mW for the capacitor banks, when operating in the 900 MHz band.

IV. Experimental Results

The circuit is fabricated in 28nm FD-SOI CMOS from STMicroelectronics and integrates the FIR-DAC SIGGEN, the DRFM and the FIR-DAC, with a total active area of 0.047 mm^2, including RF output pads. The IC is mounted on a 5x5 mm^2 dedicated flip-chip ball grid array (BGA), which embeds RF inductors to create the *LC* matching network, as well as additional decoupling capacitors. The device is connected to a dedicated printed circuit board (PCB), with RF differential output traces designed as adapted transmission lines at the targeted center frequency to complete the *RLC* filter. The chip micrograph and dedicated flip-chip BGA package are shown in Fig. 14.

The digital data inputs are generated externally in MATLAB, including the S/P conversion process, and streamed in using synchronized Tektronix AWG7000A arbitrary waveform generators at a clock rate $f_{data} = f_c/2$, whereas the main clock frequency is $2*f_c$. At the output, the differential to single-ended conversion is provided by an

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Agilent E2695A RF probe, and the RF output is measured on 50Ω using a Keysight N9030A PXA signal analyzer.

In Fig. 15, the measured output spectrum of a 3 MHz baseband (BB) single-tone at 6 dB back-off from the peak output power of 4.6 dBm emphasizes the out-of-band attenuation provided by the combined 109-tap FIR and *RLC* filtering. The in-band (100 MHz band) SNR is ~61 dB, which corresponds to 10 effective number of bits (ENOB).

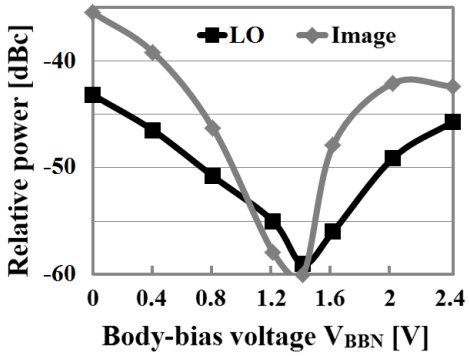


Fig. 16. Measured duty-cycle error correction using wide range FD-SOI body-bias tuning

The carrier frequency is 900 MHz and the voltage supply is set to 1 V for an overall power consumption of 34.5 mW, out of which the RF output stage, differential RF FIR-DAC, consumes 8.3 mW and the digital blocks, FIR-DAC SIGGEN and DRFM, consume 26.2 mW. Measurements also confirm the results in Fig. 6 regarding the relatively constant switching power consumption in the FIR-DAC, regardless of the signal amplitude.

It was previously described that the 2-step MUX-based digital mixer is highly sensitive to clock duty-cycle errors (~30dB image rejection degradation at $\Delta_{DCE} = \pm 0.1\%$). Duty-cycle errors can be corrected by tuning the body-bias voltage, which enables a balanced pMOS-nMOS switching operation. Fig. 16 highlights the efficiency of this mechanism in correcting DCE, thus finding an optimal operating point, where image and LO rejections are improved up to ~60 dBc at 6 dB back-off (~52 dBc at peak output power). With respect to Fig. 11, we remark similar LO and image rejection characteristics, from which we could estimate the body-bias compensation range, corresponding to a clock duty-cycle error $|\Delta_{DCE}| < 0.05\%$.

Furthermore, it is seen that increased even-order harmonics are present in the output spectrum, due to the three-state output of the FIR-DAC, which is less effective for common mode rejection. Moreover, third order counter inter-modulation (CIM3) products at -49 dBc are present in the adjacent channel (Fig. 15), which is subject to stringent constraints in terms of spurious emissions. In [22] and [23], it is shown that CIM3 can be improved by canceling the signal third harmonic at $3*f_c-f_{BB}$, which intermodulates with the desired signal at f_c+f_{BB}, resulting in spurious emissions at f_c-3*f_{BB}, due to non-linearity.

The measured spectrum for LTE 10 MHz (LTE10) and 20 MHz (LTE20) transmitted signals with 6 dB peak-to-average power ratio (PAPR) is shown in Fig. 17. The average output power and ACLR for LTE10 are -1.2 dBm and -33/-43 dBc, whereas for LTE20 we obtained -1.5 dBm and -34/-43 dBc, respectively, with an overall consumption of ~38 mW at 1 V supply voltage. Baseband digital pre-distortion (DPD) could be studied further to improve ACLR, as it is widely used in literature to increase linearity and reduce spectral regrowth and unwanted emissions into

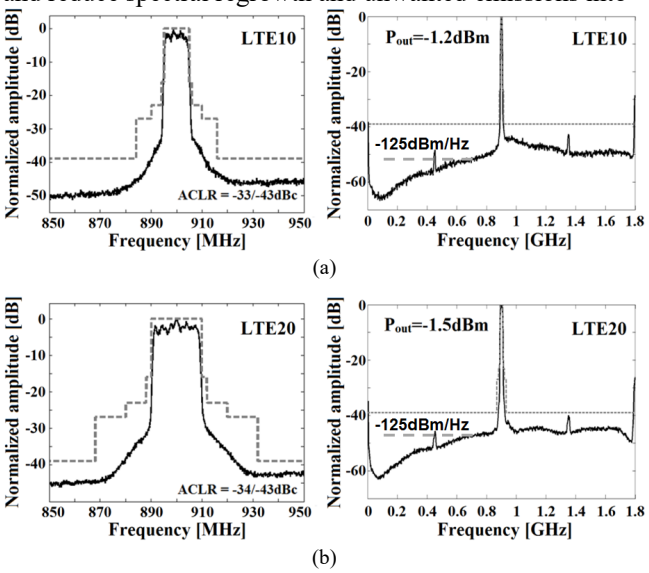


Fig. 17. Measured output spectrum: (a) LTE 10MHz; (b) LTE 20MHz.

	[2]		[4]	[5]		This work	
Architecture	Quadrature DRFC		10b ΔΣ + Mismatch Shaping 10b DAC	RQDAC + passive mixer		Digital Mixer + SC RF FIR-DAC	
Carrier Frequency [MHz]	800		900	900	2400	900	
Supply voltage [V] Output stage / Digital	1.1 / 1.1		1.5 / 0.9	0.9 / 1.1		1 / 1	
DAC Resolution [bits]	6 (physical)		10 (physical)	12 (physical)		1 (10 ENOB)	
Peak P_{out} [dBm]	13.9		1.2	3.5		4.6	
LO feedthrough [dBc]	-		-61	< -57		-59	
Image [dBc]	-		-36	< -42		-60	
CIM3 [dBc]	-		-67	< -50		-49	
Modulation signal	LTE10		LTE20	20MHz		LTE20	
Average P_{out} [dBm]	6.97		0.9	-3.5		-1.5	
ACLR [dBc]	-32.4 / -34.9		-60.7 / -61.6	-42 / -59	-47 / -59	-34 / -43	
Consumption [mW]	CW	LTE	LTE	20MHz	20MHz	CW	LTE
Output stage Digital	60.7 -	17.1 -	75 22 (w/o DSM)	11.1 -	24.8 -	12.3 26	8.8 29
Active area [mm²]	0.24		0.82	0.22		0.047	
Matching network	On PCB		On-Chip	On PCB		On BGA	
Technology	28nm		28nm	28nm		28nm FD-SOI	

Fig. 18. Performance summary and comparison with state-of-the-art.

adjacent bands [24]. Still, the DPD implementation would add extra cost in surface and power consumption for the dynamic correction feedback loop. Further description and comparison of existing DPD models can be found in [25].

The noise floor measured in a 3 MHz bandwidth is lower than -125 dBm/Hz at 200 MHz offset frequency, when transmitting both single-tone and LTE signals at the center frequency f_c = 900 MHz, and showed no dependency on the

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input signal amplitude. In addition, digital replicas appear at $f_c \pm f_c/2$, due to baseband sampling at $f_{data} = f_c/2$. The 28nm FD-SOI transmit chain performance is summarized and further compared with digital-intensive architectures in the same technology node (Fig. 18). In [2], a 6-bit switched-capacitor quadrature DRFC takes advantage of improved switching efficiency by disabling opposite cells. Next, mismatch shaping (MS) is introduced in [4] to minimize DAC static mismatch effects and reduce OOB noise by scrambling the order of conversion cells at each sampling instant. Furthermore, [5] describes a 12-bit incremental-charge based scheme to minimize dissipated power, while driving a 50 Ω load at 3.5 dBm peak output power.

The proposed digital transmit chain based on single-bit switched-capacitor RF FIR-DAC is very scalable, and the occupied silicon area can be drastically reduced, thanks to the tolerable mismatch of the unit cells. The total active area is 4 times smaller than the smallest previous design. The LO and image rejections compare favorably thanks to the body-bias-based duty-cycle correction, whereas the measured CIM3 is close to -50dBc. Delivering similar output power levels, the output stage of our system consumes less than [4] and [5], while the power consumption of the digital part is similar to [4]. Nevertheless, since the measured ACLR values are lower than in the two other designs, additional digital linearization techniques would be required, and add to the power consumption and area of the system.

Finally, the present FIR-DAC architecture is compatible with the PA design features detailed in [12], such as stacked transistors operating at twice the supply voltage, power combining, and on-chip matching to a very low output resistance ~3 Ω, and could achieve an output power level enabling operation as stand-alone 5G LTE-M compliant power amplifier. With a modest amount of additional circuitry, the Delta-Sigma modulators and FIR transfer function could also be reconfigured for different resolution and bandwidth requirements. As shown in [14] and [15], up to 160MHz of signal bandwidth is achievable for 802.11 specifications by a DSM associated to a FIR-DAC of similar complexity to the one described in this paper.

V. Conclusions

The present paper describes the system-level design of an all-digital transmitter based on a hybrid architecture, combining single-bit DAC stages in a 109-tap FIR filter, and the integration of the RF FIR-DAC output stage in 28nm CMOS FD-SOI. The general idea behind this concept is to rely only on basic circuit elements, inverters and capacitors, arranged in a straightforward matrix of unit cells, with only one cell to develop, in addition to digital library cells. Still, maintaining the output power level at low supply voltages requires the use of lower load resistances, which raises additional issues in terms of interfacing the circuit to the antenna.

The single-bit core digital transmitter offers an attractive alternative to both traditional design based on high-resolution DAC architectures, and digital-intensive transmitters up to date, by shifting analog processing towards the digital domain, and pushing the digital domain up to the antenna. The true digital nature of the proposed solution provides extensive design space for digital processing enhancement towards flexible software defined radio, making this architecture an ideal candidate for next generation IoT devices.

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