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A μ TCA back-end firmware for data acquisition and slow control of the CLaRyS Compton camera

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Abstract—With the aim to build a real-time controlled time-of-flight Compton camera for an improved ion-range dose delivery control on hadrontherapy, as defined by the CLaRyS collaboration project, a programming data acquisition and slow control back-end electronics is necessary. This paper presents the FPGA based firmware architecture, embedded software and associated tools for the back-end electronics of CLaRyS, that is able to provide multiple 3 Gb/s optical links for data acquisition, trigger distribution and slow control over its detectors. Performance of the system based on simulations and analysis of the results acquired during the characterization of a beam hodoscope will be presented. Experiments were performed with the 65 MeV proton beam of the medical cyclotron at the Mediterranean Protontherapy Institute, in Nice.

Index Terms—DSP, FPGA, Compton camera, hadrontherapy.

I. INTRODUCTION

PROTONTHERAPY and hadrontherapy using pencil beams of protons or carbon ions can deliver a dose more precisely as compared to traditional, X-ray based, radiotherapy. In practice, however, a major issue remains in the quality control of the treatment regarding the Bragg peak position and its alignment with the tumor volume.

Online monitoring of the Bragg peak position can be based on the detection of secondary radiation emitted after nuclear reactions of the incident particles within the tissues. It has been shown that the production rate of prompt-gamma ray emission, with an energy range of 1-10 MeV, is correlated to the range of the primary particles. For the purpose of range monitoring, different approaches for prompt gamma-ray imaging are currently being followed to monitor proton range. To explore these approaches, a mechanically collimated camera and a Compton camera allied with online control are proposed by the CLaRyS collaboration [1].

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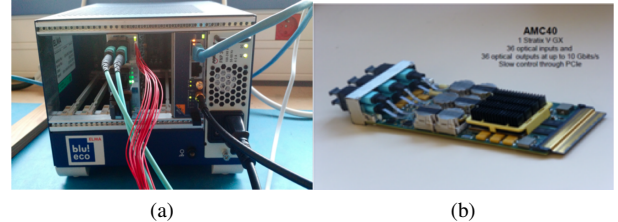


Fig. 1. 1a AMC40 DAQ board inside a μ TCA crate, along with the MCH and the clock module and 1b alone in the right.

The CLaRyS Compton camera is using three types of particle detectors: a BGO scintillation crystal absorber, a scintillating-fiber beam-tagging hodoscope and a silicon photon scatterer that must be all synchronized together by a control PC to ensure proper data acquisition, storage and analysis. To provide the necessary connectivity, physical data management, real-time slow control and low latency triggering between all these elements, programming data acquisition and slow control back-end electronics.

II. PROJECT SETUP AND ARCHITECTURE OF THE BACK-END FIRMWARE

The specifications for the back-end electronics of the experiment were set to fulfill the necessary needs for the physical performing of the Compton camera at a reduced beam-particles rate compared to clinical levels of 10^{10} protons/s. The reason for this comes from the fact that too many events detected at the time by the camera would make it impossible to see the Bragg peak as it was shown with Geant4 simulations [2].

The electronic setup of the back-end electronics, illustrated in Figure 1a, is composed of a commercial μ TCA crate [3], a micro-TCA carrier hub (MCH) with a Gigabit Ethernet switch and clock distribution support [4] and a custom in-house developed advanced mezzanine card (AMC) with a large FPGA and multiple optical links which is called AMC40 [5], illustrated in 1b. The AMC40 comprises essentially the following features:

- An Intel FPGA Stratix V SGXEA7N2F45C2 with 234 K logic cells;
- 36 optical fiber links and clock jitter cleaner;
- AMC backplane connector with support for a 1 Gigabit Ethernet link.

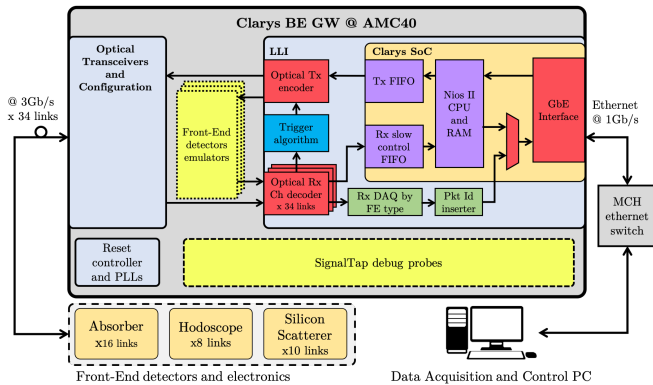


Fig. 2. Firmware architecture representation of the Back-End electronics of CLaRyS.

Following this setup, the bulk of this work is the implementation of the FPGA firmware and analysis of the performance of the Compton camera configuration. The block diagram on Figure 2 shows how the entire setup of the experiment is disposed, with the back-end on the central and top part, the three detector front-ends in the bottom left and the slow control and data acquisition PC on the bottom right.

The detectors are connected with the back-end FPGA on the AMC40 by 34 bidirectional optical links at a maximum data rate of 3 Gb/s per link, which represents a theoretical peak of 102 Gb/s in each direction. The connection with the PC is made by the 1 Gb/s Ethernet link. A 40 MHz clock signal synchronous along all the electronics elements of the chain is sourced by one of the Front-End boards through an SMA cable. Briefly the firmware is composed of VHDL code, QSYS and IP cores for the FPGA gateway part and by C/C++ code for the embedded firmware, which is divided in three datapaths: DAQ, for physical data acquisition, Slow Control for experiment control and monitoring of the detectors and electronics, and Trigger, to provide fast distribution of pre-trigger and trigger frames for the triggering procedure. There are 6 transceivers responsible for the 36 bidirectional optical links, where up to 34 are used on the project making room for a future 10 Gb/s Ethernet connections to the DAQ PC as an alternative to use the copper cable through the MCH.

Compilation information		
Software version	Quartus Prime Standard Edition 18.0 B614	
Device	Stratix V 5SGXEA7N2F45C2	
Resources utilization		
Logic utilization	114 601 / 234 720	49 %
Total block memory bits	18 533 876 / 52 428 800 bits	35 %
Total RAM blocks	1 166 / 2 560	46 %
Total DSP blocks	15 / 256	6 %
Total PLLs	45 / 92	49 %

TABLE I
COMPILATION SUMMARY OF THE FPGA PROJECT.

As most of the front-end detectors were not ready or available for tests during the framework of this project, there was a necessity to develop custom made detector emulators, on hardware (HDL), that could be embedded directly on the

chip. Detector emulators at frame format conformance and basic functional level were developed for the Hodoscope and Absorbers types, represented on Figure 2 by the blocks “Front-End detectors emulators”.

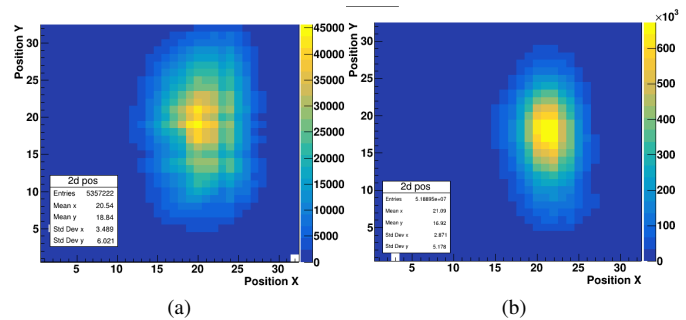


Fig. 3. 2D beam profiles with a coincidence rate of 1.3 MHz in Figure 3a and at the rate of 20 MHz in Figure 3b.

III. RESULTS AND ANALYSIS

The CLaRyS prompt gamma imaging project was tested with various partial setup assemblies during at two beam tests in Sep 2018 and Mar 2019, with the 65 MeV proton beam of the MEDICYC cyclotron of the Mediterranean Protontherapy Institute in Nice, France. Characterization of the detector’s performance is currently underway. Figures 3 presents a two-dimensional beam profile acquired in March 2019 for two beam intensities, achieving a triggering rate of 1.3 MHz.

On the measured features, the round-trip time (RTT) for Trigger operations is 26 clock cycles of 150 MHz, approximately 173.5 ns. Slow control operations are verified to be in the 1-100 ms range. Data on resource utilization of the FPGA are presented in Table I.

IV. CONCLUSION

The back-end DAQ and slow control electronics of the CLaRyS project proved to be mature, functional and conformant to the needs of trigger, physical data acquisition and slow control of the detectors during two beam tests with 65 MeV protons from the MEDICYC cyclotron of the Mediterranean Protontherapy Institute in Nice. Based on embedded emulator simulations and experimental measurements, the performance of the back-end DAQ and slow control is currently being thoroughly analyzed and characterized and will be presented shortly at the conference.

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