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Design Rules for Subthreshold MOS Circuits

Jorge Pérez Chamorro, Cyril Lahuec, Fabrice Seguin and Michel Jézéquel GET/ENST de Bretagne/PRACOM
 Technopôle Brest Iroise, CS 83818 - 29238, Brest CEDEX 3
 E-mail: jorge.perez@enst-bretagne.fr

Abstract—This paper proposes a set of useful criteria and rules to be used when designing subthreshold MOS analog decoders. The proposition is made for Gilbert-based circuits and the Sum-Product algorithm, though they are expected to work for subthreshold MOS circuits in general with minor modifications. The resulting architecture is simple, bias low-dependent and fully controllable. The nodes required by a decoder for the Sum-Product algorithm are designed as a proof of concept and interconnected together in an LDPC decoder.

Index Terms—Analog Decoding, Sum-Product Algorithm, Subthreshold MOS, Gilbert Cell.

I. INTRODUCTION

Lately many efforts have been focused in the development of analog circuits because of their advantages when compared to their digital counterparts. The main reason for using subthreshold MOS instead of forward-biased BJT to design analog decoders is to reduce the power consumption. Despite this fact, many problems have arisen when taking the circuits to work with low supply voltages and nano-currents, specially in commercial CMOS processes. For decoding, the Sum-Product Algorithm has been widely used. Analog decoders for this algorithm are built from simple four-quadrant multipliers based on the transistors' exponential behavior. Depending on the way they process the information, as Log Likelihood Ratios (LLRs) or as probability masses, there exist two approaches, the voltage and the current mode respectively. In the design process of such circuits, many relevant aspects have been usually underestimated. These include the transistor model used, various parameters of the fabrication process and proper biasing.

This paper presents a minimal set of rules and a simple architecture to successfully implement subthreshold MOS-based decoders. Following this rules allows to tackle some of the practical problems of subthreshold MOS circuits: the lack of controllability, the inaccuracy and the requirement of numerous voltage and current sources. The structure of the paper is as follows: in section II, design essentials for subthreshold MOS circuits are presented. According to them, a set of design rules is proposed in section III. Finally, in section IV, the basic cells required by the Sum-Product algorithm are constructed and an LDPC decoder is simulated using the designed nodes. Section V concludes the paper.

II. DESIGN ESSENTIALS FOR SUBTHRESHOLD MOS

Previous work on analog decoders [1,2] has provided information about the type of structures to be used when a subthreshold MOS topology is desired. However, the circuits' variables such as transistors' size, bias currents, reference

TABLE I
 AVERAGE ERRORS BETWEEN MEASUREMENTS AND SIMULATIONS[6]

| | Model | | BSIM3v3 | MM9 |
|-------------------|---------------------|---------------------|---------------|-------|
| | NMOS | subthreshold region | $V_{SB} = 0V$ | 11.6% |
| $V_{SB} \neq 0V$ | | | 17.6% | 17.0% |
| substrate current | | | 29.8% | 23.0% |
| PMOS | subthreshold region | $V_{SB} = 0V$ | 10.1% | 6.0% |
| | | $V_{SB} \neq 0V$ | 20.0% | 17.0% |
| | substrate current | | 50.3% | 25.0% |

and bias voltages, and power supply have not been justified. Thence such circuits have been found hard to control when implemented. In practical terms, it is shown that the following criterion have a great importance.

1) *Models for Circuit Simulation - BSIM3 and MM9:* The MOSFET model used for circuit simulation plays a fundamental role in the design process. Two of the most used are MOS Model 9 and BSIM3. The MM9 is an analytical model for analog applications developed by Philips [3,4]. BSIM3 is a public-domain set conceived at the University of California, Berkeley [5].

Table I presents the results of a comparison between the BSIM3v3 and MM9, in terms of the average errors between measurements and simulations of I-V data [6]. For two different substrate bias conditions in the subthreshold region, it is concluded that MM9 performs better than BSIM3v3. Note that the minimum errors are for PMOS transistors with $V_{SB} = 0V$ modeled by the MM9.

Due to the subthreshold exponential dependencies, small parameters' variations induce several changes, e.g., the large subthreshold diffusion current alterations due to the small effects of trapped surface or bulk charge upon the surface potential. Hence, simplified models may be used if they have precise relations to V_{DS} and V_{SB} . Such models should also reflect important subthreshold effects, e.g., the threshold voltage variation as a short-channel effect affects more the NMOS than the PMOS transistors [7–9]. The MM9 is the model used in the rest of the paper.

2) *Substrate Bias (V_{SB}):* Almost every single equation in the model is related to this variable. One of its effects is the shifting of the transconductance curves to higher gate voltages.

Fig. 1 shows that at high V_{GS} values, the whole family of I_{DS} curves begin to spread out and shifts to the right due to an increase in the threshold voltage. This effect is directly proportional to the channel doping, thus it affects differently the n-channel and the p-channel MOS [8].

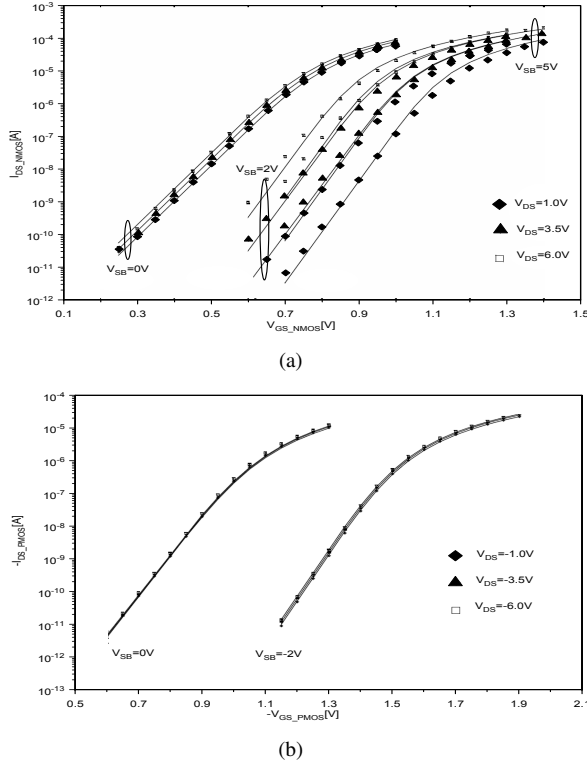


Fig. 1. Calculated (fully drawn lines) and measured (marks) subthreshold characteristics for a) NMOS @ $V_{SB} = \{0V, 2V, 5V\}$ and b) PMOS @ $V_{SB} = \{0V, -2V\}$ under different V_{DS} conditions [9].

3) *Subthreshold slope*: The subthreshold slope is tied up via the gate voltage to the variation of the depletion charge with respect to the surface potential. The latter affects the gate control of the potential barrier between source and channel [7, 9]. As it will be further seen, this parameter becomes constant if and only if $V_{SB} = 0$.

4) *Short Channel and V_{DS} variation effects*: The drain bias augmentation is linked to the increase of the depletion charge under the drain end of the channel. The latter is inversely proportional to the mobile carrier charge. Hence the drain current and its saturation voltage are sensitive to V_{DS} 's variations. For short channels, large values of V_{DS} cause the expansion of the drain depletion layer and hence affect the potential barrier between the source region and the channel area [8, 9].

5) *DIBL*: Another important effect is the drain-induced barrier lowering (DIBL), which basically implies a reduction in the threshold voltage V_T due to an increase of V_{DS} [10, 11].

6) *Mismatch*: According to [12], two factors contributing to transistor mismatch are the edge effects and random fluctuations. To be accurate, the offset voltage present in differential pairs should be taken into account for simulations.

III. DESIGN RULES PROPOSED

A. Equations

To accomplish the requirements imposed by the considerations of the precedent section, a basic set of design rules is

proposed. The following equations are presented first. Eq. (1) is the model of the subthreshold slope, eq. (2) is the surface potential at the source-side, eq. (3) gives the variation of V_T due to the DIBL effect, eq. (4) is the transistor's specific current, and eq. (5) determines the inversion coefficient:

$$m = 1 + m_o \left(\sqrt{\phi_b} / \sqrt{V_{SB} + \phi_b} \right)^{\eta_m} \quad (1)$$

$$\psi_{sS} = V_{gt2} / m \quad (2)$$

$$\Delta V_{T,DIBL} = -\gamma_{oo} \left(\sqrt{V_{SB} + \phi_b} / \sqrt{\phi_b} \right)^{\eta_\gamma} V_{DS} \quad (3)$$

$$I_S = 2m\mu_o C_{ox} (W_{eff} / L_{eff}) \phi_T^2 \quad (4)$$

$$IC = I_{DS} / I_S \quad (5)$$

where m_o is the MM9 subthreshold-slope parameter, η_m and η_γ are MM9's back-bias dependence parameters linked to if it is or not an implanted substrate, γ_{oo} is the MM9 DIBL parameter, ϕ_b is the surface potential in strong inversion, ϕ_T is the thermal voltage and I_{DS} the drain-source current.

For I_{DS} , eq. (6) is a simplified theoretical model, and eq. (7) is the one used in MM9 for circuits' simulations:

$$I_{DS} = \phi_T \mu \frac{W_{eff}}{L_{eff}} Q_{iO} \exp \left(\frac{V_{gt2}}{m\phi_T} \right) \times \left\{ 1 - \exp \left(-\frac{V_{DS}}{\phi_T} \right) \right\} \quad (6)$$

$$I_{DS} = \beta G_3 \frac{V_{gt3} V_{ds1} - \left(\frac{1+\delta_1}{3} \right) V_{ds1}^2}{1 + \theta_1 V_{gt1} + \theta_2 \left(\sqrt{V_{SB} + \phi_B} - \sqrt{\phi_B} \right)} \times \frac{1}{(1 + \theta_3 V_{ds1})} \quad (7)$$

where μ is the carrier mobility, Q_{iO} is the inversion charge per unit surface and V_{gt2} is the gate voltage. All other parameters in eq. (7) are just as in MM9 [9].

B. Setting V_{SB} to 0

Fixing $V_{SB} = 0$ brings many advantages. Table I, shows that it reduces the average error of the model. In terms of equations it implies the simplification of the eq. (1) and (3), to eq. (8) and (9) respectively. Eq. (3) and (7) become independent of both the surface potential ϕ_b , and the mobility reduction coefficient due to the back-bias θ_2 . Note that thereafter eq. (4) is only temperature dependent, and eq. (8) is only process dependent. Moreover, eq. (8) and (9) are then valid for any, implanted or non-implanted substrates.

$$m = 1 + m_o \quad (8)$$

$$\Delta V_{T,DIBL} = -\gamma_{oo} V_{DS} \quad (9)$$

C. Transistors' Size and Type

Considering that the parameter to optimise is the power consumption, the maximum current wanted through the transistors (I_{DSMAX}) and the inversion coefficient can be fixed to desired values. Then eq. (4), (5) and (8) lead to eq. (10), allowing to determine the transistors' aspect ratio for weak inversion circuits ($IC \ll 1$ in this mode of operation).

$$\frac{W}{L} = \frac{I_{DSMAX}}{2IC (1 + m_o) \mu_o C_{ox} \phi_T^2} \quad (10)$$

TABLE II
QUBiC4 CMOS TRANSISTORS' PARAMETERS

| Parameter names (units) | NMOS | PMOS |
|--|-----------|-----------|
| γ_{oo} (-) | 36.67E-3 | 18.11E-3 |
| C_{ox} (F) | 5.75E-3 | 5.57E-3 |
| m_o (-) | 374.60E-3 | 536.70E-3 |
| N_s (cm^{-3}), $a > 1$ | X | aX |
| Eq. (10) @ $IC = 0.03$, $I_{DS_{MAX}} = 1\mu A$ | 67.7 | 62.5 |
| Eq. (11) @ $L = 0.4\mu m$ | 4.78GHz | 4.78GHz |

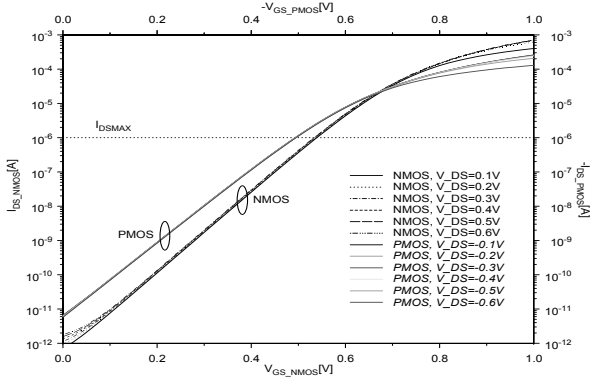


Fig. 2. Simulated subthreshold characteristics for NMOS and PMOS transistors sized according to Table II @ $V_{BS} = 0V$ for different V_{DS} values.

The selection of the transistor type and the fabrication process should be guided by two considerations: the process having the highest channel doping, as it will experience the minimum *spreading* effect [8], and the process allowing *independent* bulk-source connections ($V_{SB} = 0$) for all transistors. The latter condition may be accomplished by any standard CMOS process when PMOS architectures are used. Otherwise a costly Silicon On Insulator (SOI) process should be available for implementing an NMOS topology.

The parameters of the Philips Semiconductors' QUBiC4 $0.25\mu m$ CMOS transistors are presented in Table II, from where the architecture is determined to be PMOS because the channel doping is greater than in NMOS. Also note that the DIBL coefficient γ_{oo} is considerably smaller for the PMOS, which translates into a smaller variation of V_T due to V_{DS} .

Fig. 2 shows the subthreshold characteristics of the transistors whose W/L and V_{SB} are fixed according to the proposed rules. Thus for all transistors, the V_{SB} is 0. The length $0.4\mu m$ is 1.6 times the minimum size for reducing short-channel effects, and the width is $25.0\mu m$ for the PMOS and $27.1\mu m$ for the NMOS. The maximum frequency allowed by the transistors in weak inversion is determined by eq. (11) [13], which is also a guide to determine transistors' length.

$$f_{T_{max,weak}} < \frac{\mu_o \phi_T}{\pi L^2} \quad (11)$$

D. Currents and Voltages

To adequately limit the transistors' operation range, it is quite useful to constraint the current through the set of computing transistors. It guarantees that the whole circuit will

operate in the region it was designed for: neither the current will converge to zero, nor exceed the maximum value allowed by design.

It is concluded in [14] that the supply voltage required by transistors in weak inversion for an analog application should be greater than $10\phi_T$, and for a digital application it should be greater than $4\phi_T$. Based on this study, the recommended minimum voltage supply is:

$$V_{CC_{MIN}} \cong (10A + 4B)\phi_T \quad (12)$$

where A is the maximum number of computing transistors in a path between the power supply and ground, and B is the quantity of transistors whose current is static in the same path.

If the transistors' size is determined by eq. (10), and if some of the transistors are used as inputs, it is suggested to bias them according to:

$$V_{BIAS_i} \cong i(V_{CC} - 4B\phi_T)/A + j4\phi_T \quad (13)$$

where $i \in \{0, 1, \dots, A + B - 1\}$ is the transistor's number from ground to V_{CC} , and $j \in \{0, 1, \dots, B\}$ is the quantity of static transistors between the transistor i and ground. It is also highly recommendable to keep symmetry on the quantity of transistors in those paths, in order to have similar V_{DS} for all transistors and then force a limit. This minimises the current variations due to changes in the drain bias, which is specially important when working with NMOS circuits.

IV. MOS VOLTAGE-MODE GILBERT-CELLS

The principal modes to handle the information in analogue decoding are the *current* and the *voltage* mode. The current mode requires renormalisation stages and shows a strong memory effect [1]. Also, many domain changes (from I to V, from probabilities to LLR) are done in the processing of the soft information originally given by LLRs. However, current mode is easy to implement using MOS-only translinear loops [1] and consumes low power. Alternatively, in the voltage mode there is no need of renormalisation, only LLR information is processed [2] and there is a weaker memory effect [15]. It is functional when implemented using BJT-based Gilbert Cells [16], though they are power hungry. MOS-only architectures in this mode were shown to be inaccurate and hard to control [16], and the interconnection stages induced several errors because of biasing requirements [2]. Using the proposed design rules, the computing nodes required by the Sum-Product Algorithm are constructed.

1) *Equality and Parity-Check Nodes*: From the discussion of the precedent section it was concluded that a PMOS topology is the most appropriate for the QUBiC4 process. The minimum supply and the bias voltages required by the Gilbert-based circuits are determined by eq. (12) and eq. (13) respectively, where $A = 3$ and $B = 1$. To accomplish symmetry on the transistor's quantity, no dummy currents are short circuited directly to ground or to V_{CC} , but to a diode-connected MOS. Fig. 3 presents the schematic of the PMOS equality node. The check node schematic is easily obtained by changing the connections accordingly. Fig. 4 shows post-layout simulations of the Equality Node's performance. The achieved responses

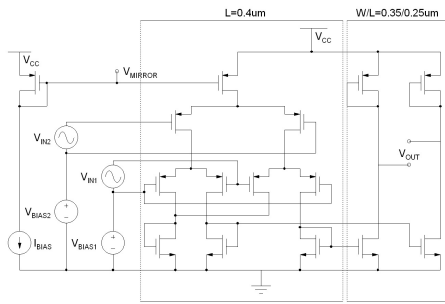


Fig. 3. Schematic of the PMOS Equality Node designed using the proposed criteria

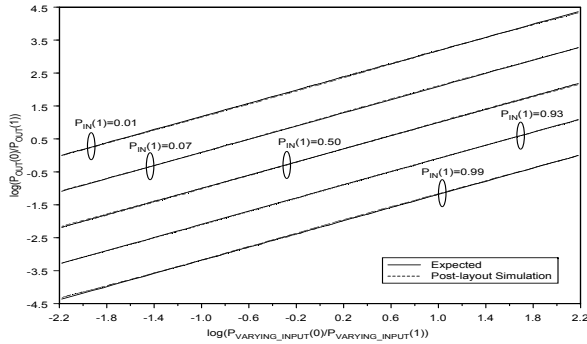


Fig. 4. Performance of the designed PMOS Equality Node using the proposed criteria. Expected and Simulated curves for several typical configurations are plotted.

are practically attached to the ideal regardless of which input is varying. The format used to present the results is similar to that in [17].

Any quantity of nodes can be interconnected taking into account the bias required by the inputs. It is important to say that the bias have supported, in simulations, variations up to 25% without affecting considerably the circuit's response. This fact gives great flexibility to the interconnection stages (as four MOS level shifters may be used) and guarantees the interoperability. Composed nodes for the required multi-directional exchange of information are obtained by interconnecting basic nodes appropriately.

2) *The Decoder*: Fig. 5 shows the convergence to a new codeword for a simple LDPC decoder [18] using the proposed nodes. The hard inputs from bit 1 through 10 were {1011001001}. An error occurred on the first bit. The hard outputs are {0011001001}, where it is seen that the error was corrected. The decoder only uses one current and one voltage source, and a reset clock. The reset is applied to every differential I/O pair at the composed nodes to fix initial probabilities to $\frac{1}{2}$.

V. CONCLUSION

A CMOS-only voltage-mode circuit solution for analog decoders using the sum-product algorithm has been successfully designed and simulated using the proposed set of rules. It is shown how to properly control subthreshold MOS circuits, reaching a truly simplified MOS model. High performance of the circuits and high accuracy in their coupled response were reached. No additional circuits or sources were used.

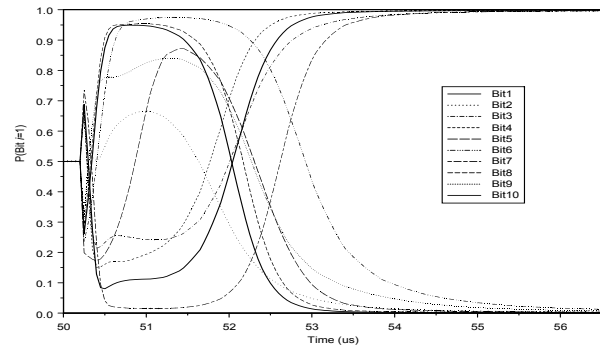


Fig. 5. Convergence of the LDPC decoder to a new codeword, SNR=3dB.

REFERENCES

- [1] C. Winstead, "Analog iterative error control decoders," Ph.D. dissertation, University of Alberta, 1996.
- [2] F. Lustenberg, "On the design of analog iterative VLSI decoders," Ph.D. dissertation, Swiss Federal Institute of Technology, 2000.
- [3] (2005) MOS model 9. Royal Philips Electronics. [Online]. Available: http://www.semiconductors.philips.com/Philips_Models/mos_models/model9/
- [4] D. K. R. Velghe and F. Klaassen, "Compact MOS modeling for analogue circuit simulation," *velghe_mm9_iedm1993.pdf*, Philips Research, Tech. Rep. IEDM Techn. Digest, 1993. [Online]. Available: http://www.semiconductors.philips.com/Philips_Models/mos_models/model9/
- [5] (2005, July) Bsim3 homepage. The Device Group Department of EECS UC Berkeley. [Online]. Available: <http://www-device.eecs.berkeley.edu/~bsim3/>
- [6] K. M. S. Healey and D. Klaassen, "Comparison of BSIM3v3 and MOS MODEL 9," *ur027.97.ps*, Philips Research, Tech. Rep. Nat. Lab. Unclassified Report 002/97, 1997. [Online]. Available: http://www.semiconductors.philips.com/Philips_Models/mos_models/model9/
- [7] E. Vittoz and J. Fellrath, "CMOS analog integrated circuits based on weak operation inversion," *IEEE J. Solid-State Circuits*, vol. SC-12, no. 3, pp. 224–231, June 1977.
- [8] S. L. P. Chan, R. Liu and M. Pinto, "A subthreshold conduction model for circuit simulation of submicron MOSFET," *IEEE Trans. Computer-Aided Design*, vol. CAD-6, no. 4, pp. 574–581, July 1987.
- [9] *MOS Model, level 903*, m903.pdf, Philips Semiconductors, Oct. 2004. [Online]. Available: http://www.semiconductors.philips.com/Philips_Models/mos_models/model9/
- [10] M. Jamal and Z. Yan, "Substrate bias effects on drain-induced barrier lowering in short-channel pmos devices," *IEEE Trans. Electron Devices*, vol. 37, no. 7, pp. 1707–1713, July 2001.
- [11] R. Troutman, "VLSI limitations from drain-induced barrier lowering," *IEEE Trans. Electron Devices*, vol. ED-26, no. 4, pp. 461–469, Apr. 1979.
- [12] M. Cohen and A. Andreou, "Current-mode subthreshold MOS implementation of the herault-jutten autoadaptive network," *IEEE J. Solid-State Circuits*, vol. 27, no. 5, pp. 714–727, May 1992.
- [13] W. S. R. van de Plassche and J. Huijsing, Eds., *Analog Circuit Design - Low-Power Low-Voltage, Integrated Filters and Smart Power*. Kluwer Academic Publishers, 1995, ch. Low-Power Low-Voltage Limitations and Prospects in Analog Design, pp. 3–16.
- [14] E. Vittoz, "Weak inversion in analog and digital circuits," in *Competence Center for Circuit Design Workshop 2003*, Oct. 2003.
- [15] V. G. C. Winstead, N. Nguyen and C. Schlegel, "Low-voltage CMOS circuits for analog decoders," in *3rd International Symposium on Turbo Codes & Related Topics*, 2003.
- [16] M. Moerz, "An analog 0.25μm BiCMOS tailbiting MAP decoder," in *IEEE International Solid State Circuits Conference*, 2000, paper WA 21.5, pp. 356–357.
- [17] H. L. P. Merkle and M. Frey, "Measurements and observations on analog decoders for an [8, 4, 4] extended hamming code," in *2nd Analog Workshop*, Zurich, Sept. 2003. [Online]. Available: <http://www.isi.ee.ethz.ch/adw/>
- [18] A. Snoeren, "On the practicality of Low-Density Parity-Check codes," *MIT Lab for Computer Science*, pp. 1–14, June 2001.