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Benefits of GaN transistors and embedding in PCB laminates

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Abstract: More electrical vehicles, either automotive or aeronautics, should benefit of the electrical performances of GaN power transistors. High-speed switching opens the possibility for higher switching frequency and the consequential benefit on the size of passive components. Efficiency and power density should be improved by overcoming some strong challenges. Reducing the parasitic components within the switching cell is a prime concern. Embedding transistors has been experimented, with a special care given to the issue of thermal management. Multiple chips per switch may be necessary to address medium power applications but paralleling GaN transistors is not straightforward. A multi-phase converter architecture may circumvent the latter problem, as PCB technology is especially suited to managing complex interconnects. Embedding not only the active devices, but also the passive components may introduce additional degrees of freedom. If a proper design approach is considered and some limitations are reasonably taken into account, combining the advantages of GaN transistors and their embedding technologies is promising solution. The paper proposes a review of the state of art and discusses some specific results to support the pros and cons of mixing GaN transistors and embedding in printed circuit board.

Keywords: high temperature power conversion, wide-band-gap semiconductors, magnetic devices, dielectric devices, polymer substrate, embedding.

1. Introduction

Electrical vehicles (EV or HEV), including aircraft and ships, are the grounds for advanced developments in terms of electrical network. Advances are comparable in diversity, constraints and objectives as those related to smart grids. An electrical network is an assembly of software and hardware components (Fig. 1, [1]). Different schematics may be appreciated depending on the issues to highlight. In Fig. 2, the network aspect is more obvious with the exchanges of information and energy between components. Buried in many places inside such a network are power electronic converters, either DC/DC or AC/DC, or any combinations. There is a considerable momentum towards more efficient converters within a lower volume or lighter technologies with a target of cost and easiness of design.

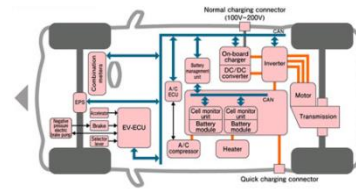


Figure 1: Possible schematic of the electrical network in an electrical vehicle [1].

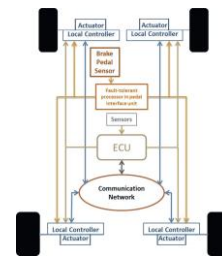


Figure 2: Example of brake-by-wire network point-of-view [2].

Gallium-Nitride transistors are supplanting Silicon-Carbide transistors in automotive applications as an acceptable cost of these devices is foreseen. Further, multiple manufacturers are pushing for better performances to circumvent possible limitations like a questionable ruggedness or smaller lifetime than their silicon counterparts.

GaN transistors enable a higher frequency of operation with a benefit on the size of passive devices. A GaN High Electron Mobility Transistor (HEMT) is capable of very fast switching. This capability comes with now well-known issues. The switching cell configuration must exhibit the lowest possible parasitic components, mainly the inductive stray inductance, the effect of magnetic coupling or the common-mode capacitances. When stimulated, these parasitic components create over-current and over-voltage stresses along with high di/dt and dV/dt . Electro-Magnetic Interferences are exacerbated and filters must be implemented, increasing the cost of the power density and weight.

The paper summarizes several activities performed at Ampere-lab about GaN-based power conversion. Section 2 introduces a simple example to show the benefits of GaN HEMTs but also inherent limitations. Section 3 introduces the issues related to paralleling of GaN transistors. Embedding of active devices and passive devices appear then as a possible degree of freedom to alleviate critical limitations. Section 4 describes what can be achieved when using embedding of interconnects and devices. To save cost and be compliant with conventional fabrication

tools, a specific design approach is necessary that is introduced in Section 6.

2. A textbook example

A test vehicle is presented to highlight the interest of GaN HEMTs compared to their silicon counterparts [3, 4]. The vehicle explores a standard dual-active-bridge (DAB) for a low voltage application (Table 1)

Parameter	Unit	value
V_{in}	V	30
V_{out}	V	30
P_{out}	W	150
F_{sw}	kHz	500-750

Table 1: Main specification for the vehicle in Fig. 6.

A N-MOSFET implementation is shown in Fig. 3. A conventional transformer is selected but it is not the limiting component regarding losses. Transistors are subject to large switching losses at 500 kHz and a maximum efficiency of 92.2% could not be exceeded, regardless of the optimization effort.

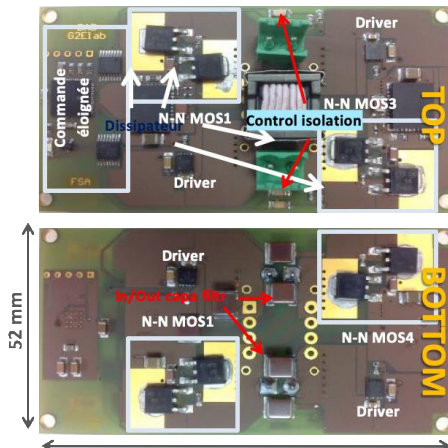


Figure 3: N-MOSFET DAB on a two-layer FR4 board.

A GaN HEMT version is characterized with no particular layout strategy, except a sufficient convection area underneath each transistor (i.e. a thermal-option limited design) (Fig. 4). Schottky diodes are inserted and reverse conduction of transistors is avoided. Efficiency is thus improved even at 1 MHz, a frequency only limited by the magnetic material and transformer design (Fig. 4, Table 2).

Reverse conduction of GaN HEMT may be introduced. Schottky diodes are removed at the expense of some additional losses (Table 3). At low voltage a diode-less converter may be safely considered.

If a galvanic insulation is not mandatory in the application, the magnetic transformer may be replaced by a series resonant impedance (Fig. 5).

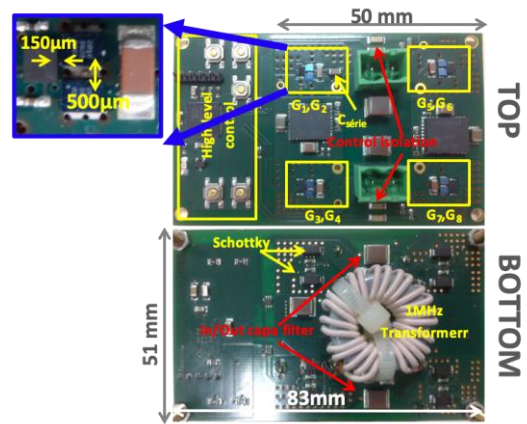


Figure 4: GaN HEMT DAB with Schottky freewheeling diodes on a two-layer FR4 board

Parameter	Unit	Value	
P_{max}	W	150	
Power density	$V_{in}=30.4V/V_{out}=29.5V$ $P_{out}=121.25W@500kHz$	kW/lit	4.75
	$V_{in}=30.39V/V_{out}=29.5V$ $P_{out}=119.48W@1MHz$		4.7
Efficiency	@500kHz/ $P_{out}=121.25W$	%	94.5 (7W losses)
	@1MHz/ $P_{out}=119.48W$		93.8 (7.85W losses)

Table 2: Performance indicators of the converter in Fig. 4.

Parameter	Unit	Value	
$P_{out\ max}$	W	150	
Power density	$V_{in}=30.33V/V_{out}=29.5V$ $P_{out}=138.4W@500kHz$	kW/lit	5.42
	$V_{in}=30.33V/V_{out}=29.5V$ $P_{out}=122.43W@1MHz$		4.8
Efficiency	@500kHz/ $P_{out}=138.4W$	%	94.64 (7.8W losses)
	@1MHz/ $P_{out}=122.43W$		93.44 (8.6W losses)

Table 3: Performance indicators of the converter in Fig. 4 without Schottky diodes.

Parameter	Unit	Value	
$P_{out\ max}$	W	150	
Power density	$V_{in}=30.35V/V_{out}=29.5V$ $P_{out}=142.2W@500kHz$	kW/lit	12.36
	$V_{in}=30.34V/V_{out}=29.5V$ $P_{out}=136.6W@1MHz$		11.87
Efficiency	@500kHz/ $P_{out}=142.2W$	%	95.95 (6W losses)
	@1MHz/ $P_{out}=136.6W$		94.6 (7.8W losses)

Table 4: Performance indicators of the capacitive-coupling converter in Fig. 5 without Schottky diodes.

Table 4 lists the performance indicators and both the power density and efficiency are improved. At this stage a possible optimization is to reduce the footprint of the bridges using a quad driver instead of two phase-leg drivers. When pre-designing the quad driver, an electrothermal simulation indicates a limitation due to the convection approach to cool the HEMTs: the driver is directly in the thermal flow. An alternative layout must be considered or a high-temperature quad driver.

One other major limitation has not been mentioned so far: the fast switching of GaN HEMT (50 V/ns) introduces a lot of EMI issues that disturb the drivers and finally limit the operating frequency [5].

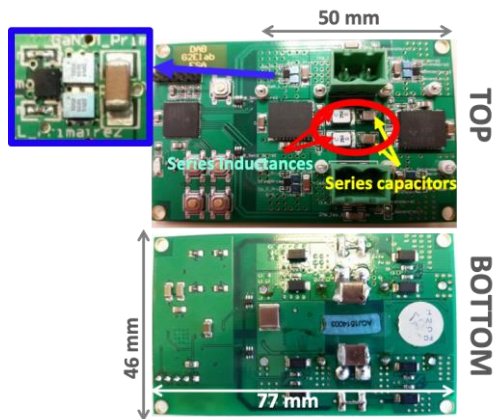


Figure 5: Diode-less, GaN HEMT DAB without a magnetic transformer.

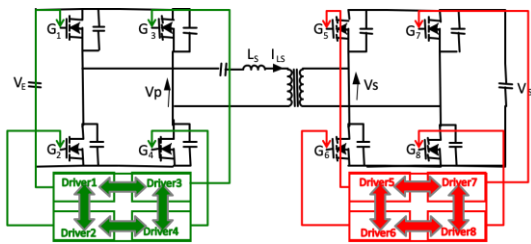


Figure 6: Schematic of a quad driver for synchronous operation of the GaN HEMTs.

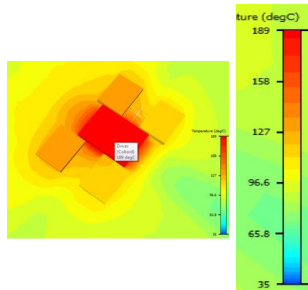


Figure 7: Electro-thermal simulation of the quad driver environment.

Parasitic components along the power switching loop (switching cell) is a well-known issue. The distance between devices causes stray inductances, which in turn are stimulated by the electromagnetic energy they capture. The minimal loop area is quickly obtained in a planar configuration (Fig. 8a) [6]. The concept of orthogonal loop is the other strategy to reduce the loop area, i.e. the electromagnetic energy stored in the loop during operation. Options in Fig. 8b and 8c have been explored in [6]. The thickness of the polymer substrate is the limitation in Fig. 8b, while an application specific polymer substrate may be considered in Fig. 8c. Embedding of active devices is in fact exploring the same idea but with more degree of freedom, as layers of interconnection are managed underneath and above the active devices. The HEMT gate loop is affected by the same limitation as illustrated in Fig. 9. The energy is exchanged between the decoupling capacitor of the driver, the driver and

the gate-source path. The area of this loop must be minimized as well. Some options of interconnection are illustrated in Section 4. The next section discusses the issue with respect to paralleling GaN HEMT, i.e. the antagonism between a reduction of switching loop area and multi-chips per switch for a higher current rating.

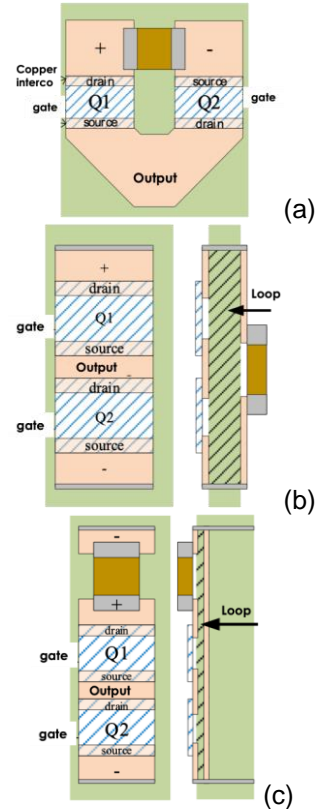


Figure 8: Power loop in a half-bridge configuration: planar (a), orthogonal (b) and (c)[6].

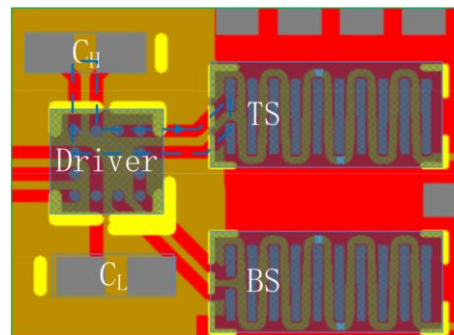


Figure 9: Schematic of the HEMT control loop (dashed blue).

3. Paralleling GaN HEMTs

The main concerns related to paralleling GaN transistors are based on the package and board level design. Layout arrangement of many parallel devices can affect the current distribution among them. A simple H-bridge circuit (as the schematic diagram in Fig. 10) is implemented to investigate the parallelization of four GaN HEMTs in a single switch.

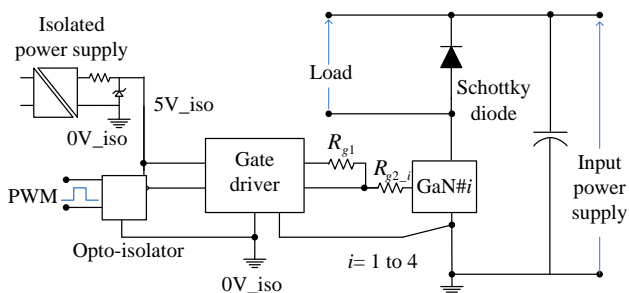


Figure 10: Schematic diagram of the test prototype.

The layout is designed to take advantage of the footprint of the GaN transistor packages. The package used here (GS66516T, GaN Systems) is suited to a line configuration. However, current distribution among GaN devices is subject to parasitic components in each power trace. In a line configuration as shown in Fig. 11, the distance to drain input of the far-end GaN device from a single-point power supply is noticeably longer than for the devices in the middle. If all transistors use the same gate signal for their operation, devices may not handle the same level of stress. At turn-on, the device with low impedance in the path handles more stress than the rest. And at turn-off the device with high impedance remains active a longer time, hence carrying more current stress.

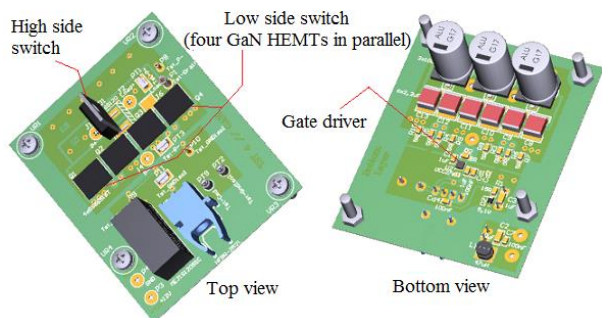


Figure 11: Case 1: four GaN HEMTs in parallel configuration. HEMTs are laid in a line.

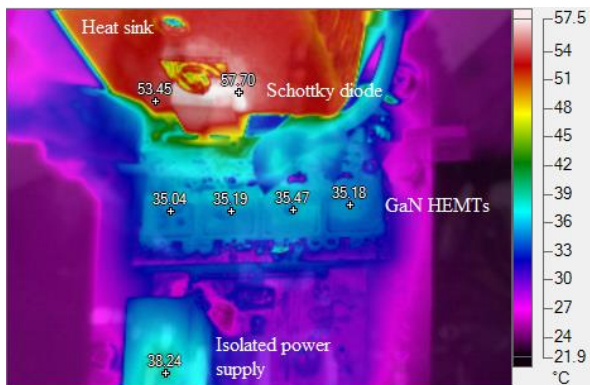


Figure 12: Thermography of the Case 1. Input voltage 80 V, load current about 27 A, switching frequency 200 kHz.

As observed in the thermography of Case 1 (see Fig. 12), a quite fair distribution of temperature is observed but some discrepancy is installed with higher input voltage and higher output current.

A more symmetrical layout may be considered where the GaN HEMTs are arranged on both sides of the PCB as illustrated in Fig. 13. This arrangement is possible as the thermal pads of GS66516T devices are on the top side of the package.

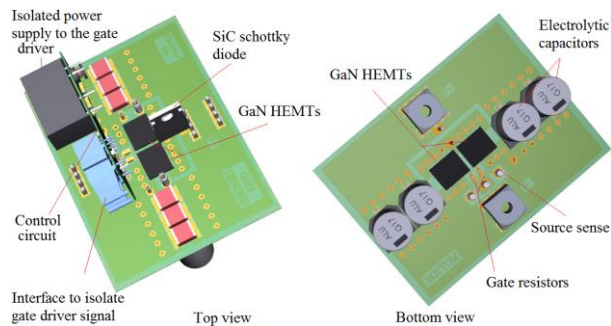


Figure 13: Case 2: four GaN HEMTs in parallel configuration. Two HEMTs are laid on each side (i.e. top and bottom).

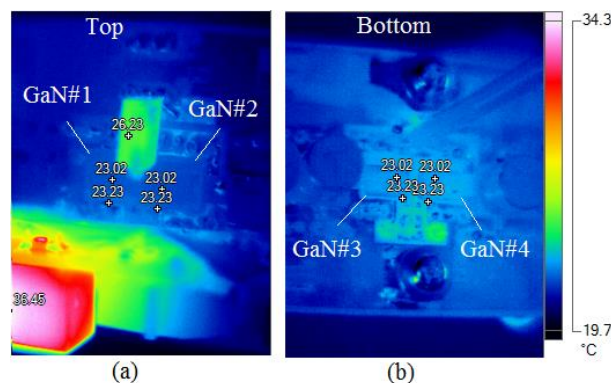


Figure 14: Thermography of the Case 2: (left) top side and (right) bottom side of the PCB. Input voltage 80 V, load 27A.

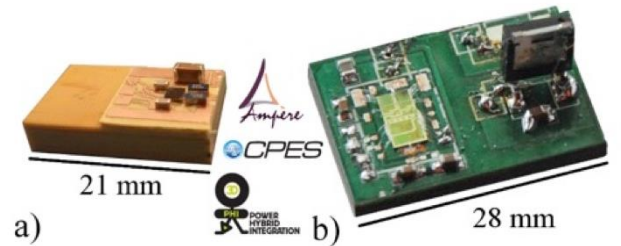
The power path can be optimized further by a more compact layout of the components. Though the thermal distribution among the components in the circuit is fairly equal, the parasitic components in the gate control path seems to trigger high frequency oscillations in the current and voltage waveforms. The switch transient current of each device at high frequency operation could be measured using high bandwidth coaxial shunts. However, the approach adds more parasitic elements to the power path and degrade the quality of the final results. A detailed analysis of the optimizing board level parasitic components can be found in [9].

So far the results tend to demonstrate that a standard planar substrate is somewhere a limitation in power device arrangement. This is the reason why embedding in the polymer substrate has received a large attention.

4. Embedding in polymer substrate

Fig. 15 gives a tentative schematic for a half-bridge configuration (650 V, 25 A) with a fair power density. Looking at the various functions, it appears that the auxiliary power supply (i.e. the power supply of the gate drivers) becomes a limiting factor. A resonant flyback configuration with an active clamp has been explored in [7] with high temperature capability. One practical solution to meet the footprint specification has been to limit the operating frequency of the flyback converter but to embed the coupling inductances in the polymer substrate, including the magnetic material. A zoom on a cross section of the magnetic core is pictured in Fig. 16, with the substrate obtained from laminated pre-preg from Panasonic, dedicated for continuous operation at +200°C.

Embedding gives a degree of freedom in terms of geometry and the coupling inductors were designed for a minimal capacitive coupling (0.85 pF @ 1.2 MHz) to enable a dynamic isolation up to 75 kV/μs at the driver level [8]. Such immunity to fast voltage transients is required to take full advantage of the GaN power transistors. Two flavors of the converter have been characterized: one is using low-voltage GaN HEMT (Fig. 17a) and the other one encompasses a silicon power ASIC (Fig. 17b). The silicon counterpart is limited in frequency but the efficiency is somewhat higher at the expense of a larger footprint. The GaN HEMT based converter could be optimized for a similar targeted efficiency without losing on the footprint area.



Sample No.	Temperature Max. /°C	Switching frequency /MHz	Efficiency (1 W)	footprint /cm ²	C _{1/2} /pF
(a)	125	2.3	68%	4.1 (0.6 in ²)	0.7
(b)	200	1.2	75%	6.4 (0.9 in ²)	0.9

Figure 17: Resonant flyback with an embedded magnetic device and performance indicators.

5. A tentative design approach

While embedding is a very attractive solution to increase power density, reduce circuit parasitics and provide suitable thermal management to PCB-mounted power electronics, it is currently complex to implement. Despite the research efforts invested in modelling and simulation, the design of a power electronics converter still pretty much relies on trial-and-error on hardware prototypes.

The reason for this may be found in the heterogeneity of power electronics, which are an assembly of custom, semi-custom and off-the shelf components supplied from many vendors, most often assembled together using a variety of technologies (PCB, busbars, loose wires...). This is depicted in Fig. 18. As a consequence, there is no unified software description of the converter (complete virtual prototype). In many cases, not all models are compatibles, and only a small subset of the converter can be simulated at a time. This is quite different from the situation in microelectronics, where monolithic integration is standards, and electronic design automation (EDA) software allows advanced simulations and design verification prior to manufacturing.

PCB embedding may help to improve the situation (Fig. 19): this is a unified manufacturing technology which can provide satisfying thermal performance (at least up to a few tens of kilowatts [10]), can manage complex interconnects (multilayer circuits, high density interconnects technologies), and which builds upon an existing base of advanced design software tools and a mature PCB industry. Therefore, it becomes possible to build a performant converter using a single technology, and the entire converter can be described and modelled from the data available in the PCB layout software. There is still a long way to go, but PCB embedding may offer the first opportunity to demonstrate a full “virtual prototype” in power electronics. This will become a necessity, because embedding tends to make prototyping more complex (it is a new technology, so a lot of preparation work is required prior to manufacturing) and its high

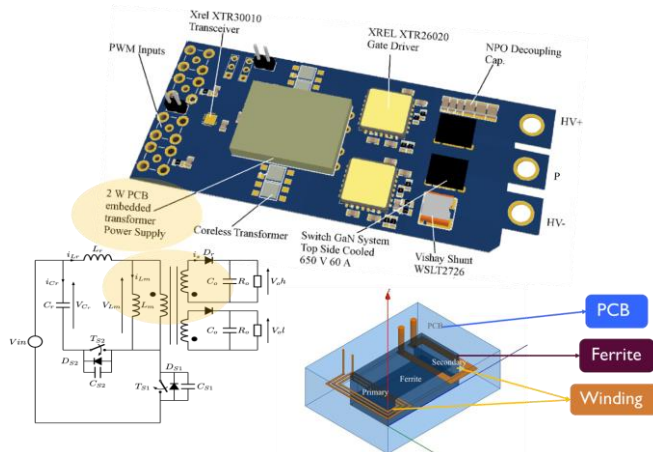


Figure 15: Footprint of the gate driver power supply inside a tentative half-bridge configuration.



Figure 16: Cross section of the embedded flyback transformer, showing the magnetic core and the copper windings.

level of integration makes measurements and debugging more difficult (and this is not to mention circuit repair or modifications which are near to impossible).

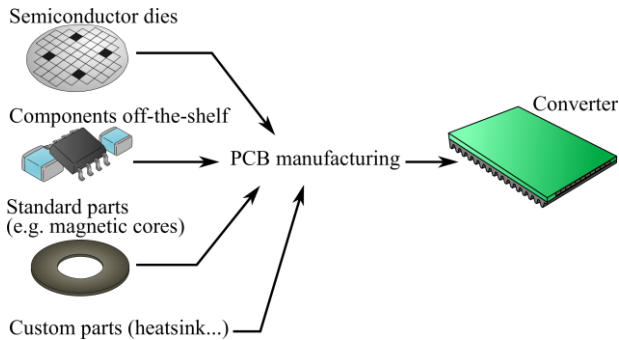


Figure 19: Rationalized manufacturing flow, where all the assembly is taken care of using PCB embedding (as well as standard PCB assembly) [11].

6. Conclusion

GaN HEMTs open a degree of freedom to the power electronic engineer but with large constraints. Other degrees of freedom must be considered to solve issues regarding interconnects to and from the power transistors and to and from the passive devices. Embedding in polymer substrate is one candidate technology to take full advantage of the performances of GaN devices.

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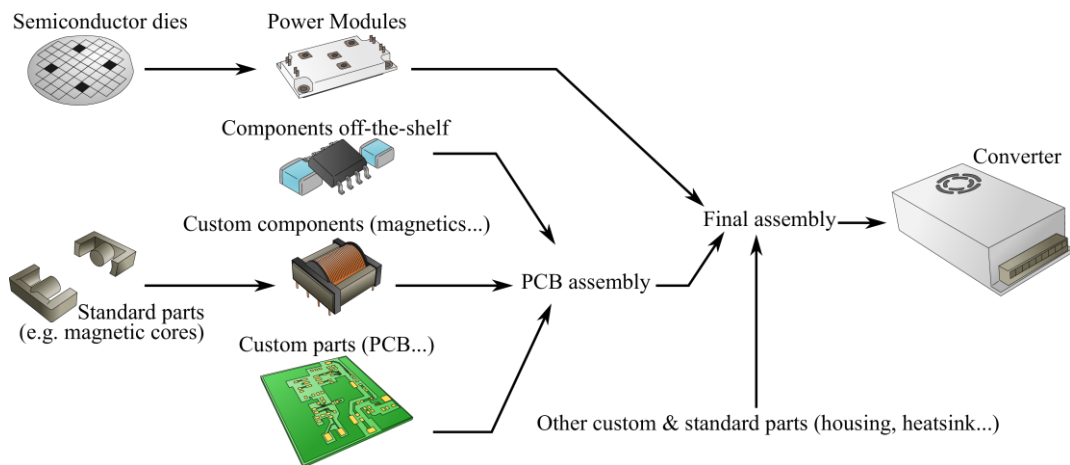


Figure 18 : Usual manufacturing flow of a converter, involving various level of packaging, and making use of different assembly technologies [11].