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Thermal Considerations of a Power Converter with Components Embedded in Printed Circuit Boards

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Abstract—Printed-Circuit-Board (PCB) technology is attractive for power electronic systems as it offers a low manufacturing cost for mass production. Integration technologies such as device embedding have been developed to take advantage of the inter-layer space in multi-layer PCBs and to increase the performances (Electrical, Thermal). However, the PCB technology offers limited power dissipation due to the low thermal conductivity ($\approx 0.3 \text{ W}/(\text{m}\cdot\text{K})$) of its composite substrate.

In this paper, we consider PCB embedding for a 3.3 kW AC/DC bidirectional converter. We describe the integration of not only the power dies, but also the gate drive circuits and the power inductor, with a special focus on the thermal management. The manufacturing processes of the boards are presented. Two thermal models based on finite elements (FE) of this converter stage are introduced. The accuracy of these models is validated against experiments. The results show that a simplified FE model offers satisfying accuracy and fast simulation, even considering the relatively complex structure and layout of the PCBs.

I. INTRODUCTION

OVER THE LAST DECADES, evolution in power electronics has mainly been driven by improvements in the switching components. Since 2001, semiconductor devices made out of wide band-gap materials have been commercially introduced: first Silicon Carbide (SiC) and more recently Gallium Nitride (GaN) [1]. However, their performances are currently limited by their packaging. Nowadays, the next driver for progress is considered to be better integration and packaging technologies [2, 3]. In particular, future packaging technologies should offer better electrical and thermal performances and low cost.

Among the possible integration technologies, Printed-Circuit Board (PCB) is especially attractive: because it is a mature technology, many advanced design tools are available, as well as a complete supply chain. It allows a high density of interconnects, and uses relatively inexpensive materials. Many manufacturing steps of a PCB rely on batch processes, allowing a large number of interconnects to be processed at once. Its main limitation is the low thermal conductivity of its base material (most commonly a glass-epoxy composite). Even the best materials have thermal conductivities lower than $10 \text{ W}/(\text{m}\cdot\text{K})$ [4], a fraction of that achieved by the ceramic materials used in power electronics (e.g. $150 \text{ W}/(\text{m}\cdot\text{K})$ for AlN). As a consequence, multilayer PCBs are mainly used for low-power converters ($< 100 \text{ W}$). For higher power levels,

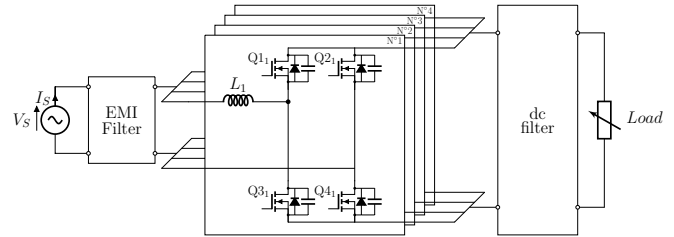


Figure 1: Circuit diagram of the converter. The topology includes an EMI filter, a Power Factor Corrector (PFC) and a dc filtering stage. The PFC uses 4 interleaved cells [15, 16].

Insulated Metal Substrates (a single-layer, thin PCB bonded onto a thick metal plate) or ceramic substrates are preferred.

With the ever increasing need for more compact electronic systems, integration technologies have been developed to take advantage of the inter-layer space in multi-layer PCBs by embedding components in the substrate [5]. Embedding the devices in the PCB allows to overcome some of the thermal limitations (by reducing the thickness of low-conductivity composite between the components and the thermal management system). Some signal electronic systems were produced with almost all components embedded in PCB [6], but for power electronics, the research has mainly been focused on embedding the active devices only [7, 8]. The embedding of passives has also been investigated for low power converter (1-100 W) with the embedding of Surface Mount Technology (SMT) components (Resistors, Capacitors, ICs) [9], of magnetic cores [10, 11], or of formed components using capacitive or resistive layers [12]. It is worth noting that aside from the scale, this vertical stacking of flat structures (also called “2.5D”) is very close to the “chip stacking” concept. Chip stacking is commonly used in microelectronics, and the thermal modeling of such structures have been explored in papers such as [13] or [14]. However, these advanced models require a considerable implementation effort.

In this paper, we investigate the embedding of all components of an AC/DC converter (semiconductor power devices, corresponding gate driver, and inductor), rated at 3.3 kW, with a special focus on thermal aspects. In section II, some details are given regarding the components to be embedded and the chosen physical implementation. The manufacturing process is described in section III. Then, in section IV, two thermal

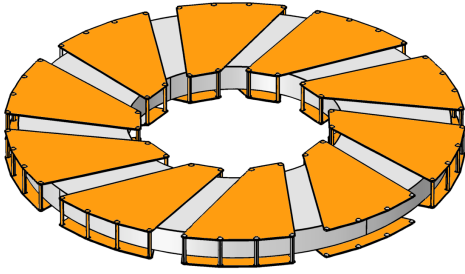


Figure 2: Drawing of an "Embedded Toroidal" inductor. The dielectric layers are not show.

models are presented, while the acquisition of experimental temperature data is presented in section V. Finally, the results are compared and discussed in section VI.

II. DESIGN OF A PFC CELL

The converter topology to be implemented is presented in Fig. 1. It includes an EMI filter, several interleaved Power Factor Corrector (PFC) cells and dc filtering stage. The components of this circuit have been selected using an optimization procedure to achieve the best power density/efficiency ratio [15, 16]. The optimized circuit is composed of 4 PFC cells (each handling a power of 825 W, for a total of 3.3 kW). In the remaining of the paper, we will focus on a single PFC cell, for which the input (ac) voltage is 240 V, 50 Hz, the output (dc) is 400 V and the input current 4 A RMS.

A PFC cell is composed of 4 SiC MOSFETs (CPM2-1200-0080, Wolfspeed) in a full bridge configuration, driven by 2 half-bridge gate drive circuits (based on an IRS21864 IC, Infineon, with their peripheral components – resistors, capacitor, diodes in SMT package –) and an inductor (34.7 μ H). The inductor uses an "Embedded Toroidal" structure which corresponds to an embedded annular magnetic core with a winding formed around by PCB tracks and vias (Fig. 2) [17]. Note that both half-bridge operate at different frequencies: in Fig. 1, Q1 and Q3 control the current in L1, and switch at high frequency (180 kHz), while Q2 and Q4 are only turned-on or off with respect to the polarity on the mains (i.e. at 50 Hz).

These 3 sets of elements (power semiconductor devices, gate drive circuit and inductor) are embedded in different PCBs which are stacked on top of a heatsink to form a compact assembly. Each PCB is separated by a layer of Thermal Interface Material (TIM). The TIM chosen is a thin (200 microm), electrically insulating (breakdown voltage 3000 V) elastomeric material which is soft enough to conform to the PCB patterns (Bergquist Sil-Pad 1500ST). The board-to-board interconnections are done with wires soldered in metallized through holes. A schematic view of the assembly is given in Fig. 3, and a photograph of the exploded PFC cell is visible in Fig. 4.

With the chosen approach, the empty space created around each component is filled with resin, as compared to air in a standard converter. The replacement of air by resin allows a better conduction of the heat from the components to the heatsink [18] and allows easier interconnection. However, the

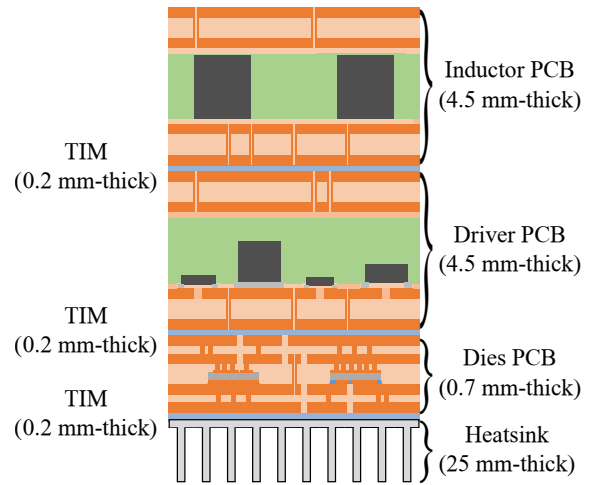


Figure 3: Cross section of a PFC cell. The PCBs thicknesses are exaggerated with regard to the heatsink thickness and of the width of the boards. The components and layout in the drawing are only illustrative..

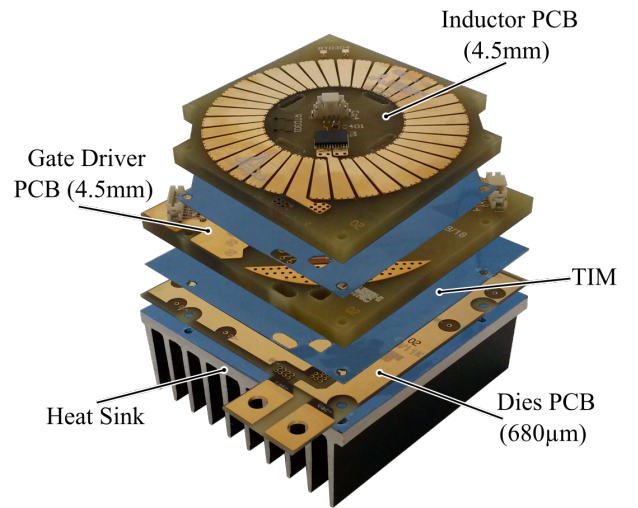


Figure 4: Exploded view of a PFC cell.

thermal conductivity of the FR-4 (Epoxy resin – fiberglass composite) which composes the substrate of the PCB remains low (0.3 W/(m·K)). With the thick structure presented in Fig. 3 (more than 1 cm), investigations are required to ensure no component will exceed its maximum operating temperature.

III. MANUFACTURING OF THE BOARDS

As depicted in Figs. 3 and 4, 3 boards are used to form the PFC cell. While two of them have similar structure ("inductor board" and "driver board", both 4.5 mm-thick), this is not the case for the "Dies board", which is much thinner (0.7 mm). From a manufacturing point-of-view, this requires the production of two different panels, each with a different manufacturing process. For the "Dies board", a "thin panel" is processed, while the "inductor" and "driver" PCBs correspond to a "thick panel". Both of these panels have 4 copper layers (numbered 1 to 4, top to bottom).

1) *Thin Panel:* Only bare SiC dies are embedded in the "Thin PCB" panel, between both inner layers. The process

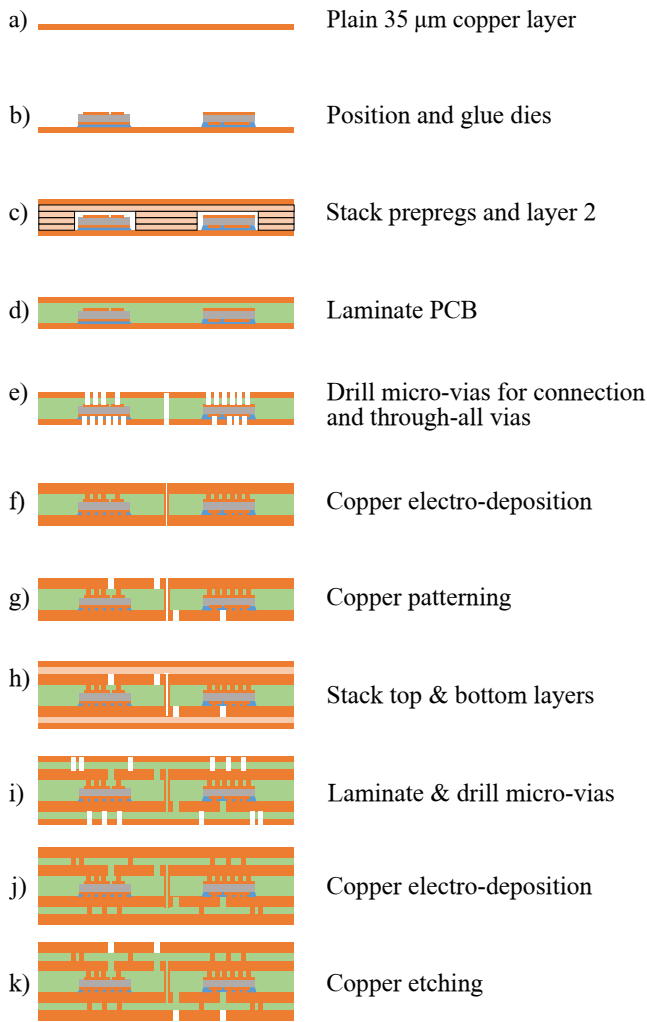


Figure 5: Manufacturing step for the panel with embedded dies: "Thin PCB". Dark orange denotes copper; light orange denotes prepreg, i.e. un-cured glass-epoxy layers which are cured during the lamination process; green denotes cured glass-epoxy layers.

is presented in figure 5. It starts with a 35 μm plain copper sheet (Fig. 5a) on which the dies are accurately positioned and bonded with non-conductive glue. Some dies are mounted "bottom up" (flip-chip, Fig. 5b) so that interconnects with fast voltage transient (i.e. the middle points of the full-bridge structure) are away from the heatsink, thus reducing common-mode noise. On the contrary, dc voltage potentials (the drain of Q1 and Q2, or the source of Q3 and Q4 in Fig. 1) are routed on large planes close to the heatsink to foster capacitive coupling to ground while providing an electrostatic screen between fast switching potentials and the heatsink.

Sheets of glass-fiber pre-impregnated with resin (so-called "prepregs") are then stacked to compensate for the die thickness (Fig. 5c) and to isolate the dies from the copper layer above. This stack is laminated (Fig. 5d) to form a solid part.

The dies interconnections ("track to dies" vias) are drilled on both sides using a laser ("microvias", Fig. 5e). The laser power is calibrated using sacrificial dies, so that the vias extend all the way through the insulating material (25 μm for the bottom glue layer and 50 μm for the top laminated sheet) and stop

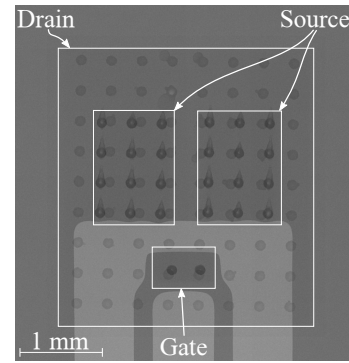


Figure 6: X-ray image of an embedded SiC die (white outline of the die and pads added for clarity), showing the microvias drilled on both sides.

when reaching the pads of the dies (finished with 8 μm copper, a value recommended by the PCB manufacturer). Copper is then electro-plated to fill the vias (Fig. 5f). After the copper electro-deposition, the thickness of the copper layers is 70 μm . They are then etched to form the PCB tracks (Fig. 5g). The X-ray image of an embedded die is visible in Fig. 6. The via positioning accuracy with respect to the dies is theoretically estimated at 100 μm (practically, it was found to be 33 μm in the worst case), thanks to accurate manufacturing equipment and monitoring of board deformation.

Finally, the external layers (layers 1 and 4) are added, using similar steps (Figs. 5h to 5k). These two layers are required so that the final panel is rigid enough for handling, has a symmetrical structure (to prevent bowing), and for routing the interconnects.

2) *Thick Panel*: For this panel, components are no longer glued. Soldering is used instead, as it is compatible with standard SMT packages. This requires to pattern the copper layer 3 before populating it with components. The process begins with a double-sided laminate with 70 μm thick copper (Fig. 7a). Through-all vias are mechanically drilled (Fig. 7b) and electro-plated. The copper is then etched to form the circuit on both sides (Fig. 7c). Some solder paste is deposited on the board by stencil-printing, with a pattern matching the footprint of the components. The components are placed on the paste and soldered using a reflow oven (Fig. 7d).

Two prepreg layers are then placed, with cut windows matching the components location and size (Fig. 7e). The aim of these prepreg layers is to provide adhesion for additional layers and to isolate the magnetic cores from copper layer 3. A spacer, composed of several PCB cores and prepregs layers is placed on top (Fig. 7f).

Finally (figs 7g and h), two more prepreg layers are placed on top to isolate the magnetic core from copper layer 2 and to bond the laminate forming the layers 1 and 2 (which was manufactured similarly to figs. 7a to c). Through-all vias are then manufactured to interconnect all four layers.

IV. THERMAL MODELS

With the complex structure depicted in Fig. 3, it is important to ensure that all embedded components operate below their maximum temperature. Here, we present the thermal models

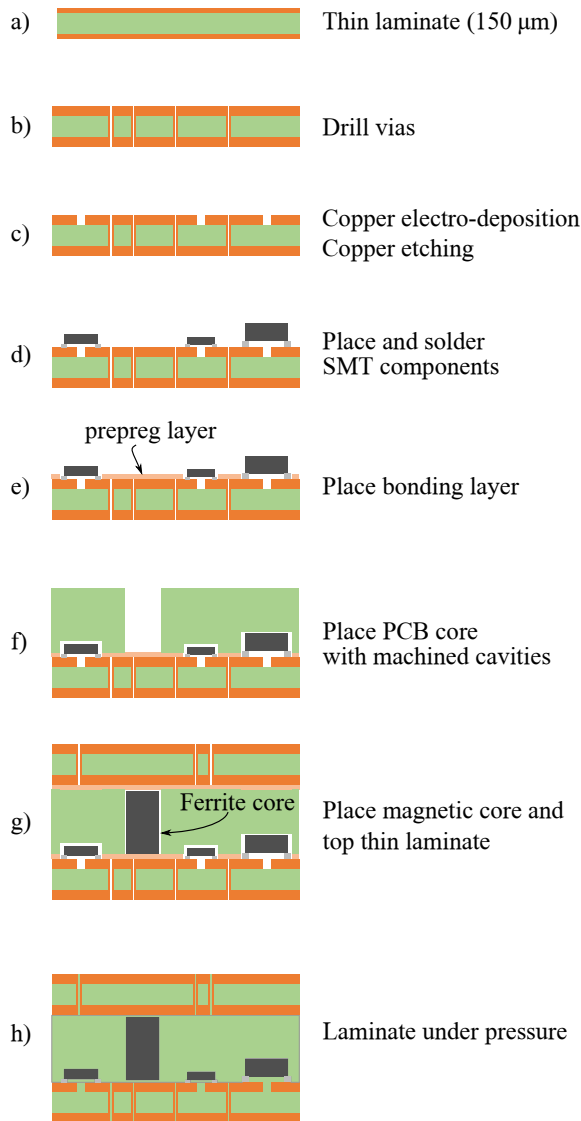


Figure 7: Manufacturing step for the panel with both embedded SMT components and magnetic cores: "Thick PCB".

which are used to compute the temperature distribution in the cell. First, a simple model is presented for the convective heat transfer from the heatsink. In a second time, two models are proposed for the heat conduction in PCB stack, and are compared regarding their complexity and computation time.

A. Heatsink Model

While the heatsink used here is fairly simple (a piece of extruded aluminium with straight fins), its Finite Element Model (FEM) is relatively complex: not only does it require many elements to mesh the heatsink itself, but the surrounding air must also be meshed so Computational Fluid Dynamics (CFD) can be applied. This is very important as the air movement (convection) dictates the heat exchange between the heatsink (i.e. the heat flux between the converter) and its environment. To keep the thermal simulations of the converter simple, a two-step approach is used: first, a detailed heatsink model is built, and simulated in a variety of conditions; then a

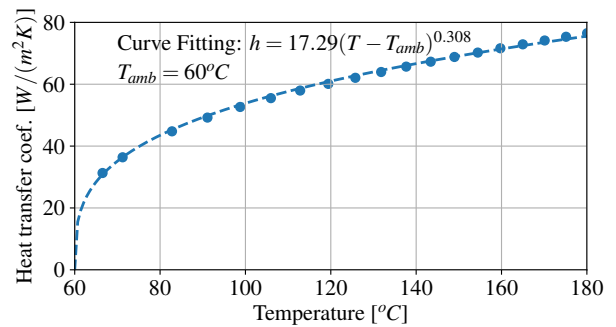


Figure 8: Simulation results of the heat transfer coefficient as a function of the temperature of the heatsink, considering convection and radiation effects, for an ambient temperature of 60 °C.

simple equation is fitted to the results of these simulations. For converter simulations, which are performed with a different FE simulator for practical reasons, this equation is used as a boundary condition, in place of the FE heatsink model.

The detailed heatsink geometry is drawn in 3D using the Icepack software (Ansys). The heatsink is placed inside a "cabinet", which represents a large volume of air around the heatsink. The cabinet dimensions need to be larger (twice, in our case) than the heatsink dimensions so its boundaries do not disturb the airflow. Air flow is only allowed to cross the top and bottom boundaries of the cabinet. Gravity is taken into account. In addition to convection phenomena, the simulator also calculates the heat exchanged by radiation. The ambient air temperature is 60 °C (maximum ambient temperature specified in our application).

A uniform power dissipation is applied on top of the heatsink baseplate. The temperature of the heatsink (considered uniform) is the result of the simulation. Several simulations are run for power dissipation levels ranging from 1 W to 50 W. The heatsink temperature is extracted for each simulation. It then becomes possible to calculate an equivalent heat transfer coefficient h at baseplate-level such as:

$$h = \frac{P}{A_{base} \cdot \Delta T} \quad (1)$$

with P the power dissipation, A_{base} the top surface area of the baseplate and ΔT the temperature difference between the heatsink and the ambient air. The heat transfer coefficient as a function of the heatsink temperature is presented in Fig. 8.

Finally, an equation of the form $h = \alpha(\Delta T)^\beta$ is fitted to the data from Fig. 8. This equation is used in the PCB-stack model as a boundary condition for the converter area which is in contact with the heatsink. This way, CFD is no longer necessary in the thermal simulations of the converter. This approach, however, can only apply to steady-state conditions (it does not consider the "thermal mass" of the heatsink), and is only valid over the power/temperature domain for which it was identified.

B. PCB-Stack Models

To some extent, a model of the PCB-stack described in Fig. 3 is simple to build: the stack has flat external surfaces;

Table I: Thermal conductivities of the different layers for the "Approximated Stack-up" thermal model.

Layer Name	Thermal Conductivity (x,y,z) (W/(m·K))
Copper Layer : Plane	$\lambda = (400, 400, 400)$
Copper Layer : PCB Traces	$\lambda = (0.3, 0.3, 400)$
Substrate layer : Standard	$\lambda = (0.3, 0.3, 0.3)$
Substrate layer : Vias	$\lambda = (0.3, 0.3, 50)$
TIM (Sil-Pad 1500 ST, Bergquist)	$\lambda = (1.8, 1.8, 1.8)$
Baseplate	$\lambda = (237, 237, 237)$
Ferrite	$\lambda = (5, 5, 5)$

Table II: Losses in each power element of a PFC cell for the converter at nominal power (as estimated during the circuit design stage [15]).

Dissipating element	Losses (W)
High Frequency Die (Per die, 2 dies per cell)	5.83 W
Low Frequency Die (Per die, 2 dies per cell)	0.81 W
Inductor (One inductor per cell)	8.25 W

the side surfaces can be considered adiabatic, heat only being exchanged through the bottom (heatsink) and top surfaces. In this way, only heat conduction has to be considered, with heat exchange coefficients as boundary conditions on the top and bottom surfaces. Here, the complexity comes from the internal structure, which is an intricate pattern of parts with different heat conductivities and thicknesses. Overall, there are 12 copper layers in the stack, many copper vias through the substrate layers, and large parts of ferrite material.

The complete FEM model of such a structure would require a very fine mesh (with many elements measuring only a few microns). Two approaches are proposed below to generate models: the first only uses a coarse approximation of the copper layout, with the objective to offer acceptable results with a low computation time, while the second considers the actual copper layout (albeit with the finer features removed). Both models are built and simulated using COMSOL.

1) *Approximated layout model*: Here, each layer of the PCB stack is represented by a unique prismatic block, with an in-plane thermal conductivity set depending on the layout of that layer. Two cases are considered here: either a layer mainly comprises large copper planes, or it mainly contains thin tracks. Indeed, heat is going to spread much more over a plain copper layer (in this case, in-plane conductivity is considered to be that of copper, 400 W/(m·K)) than in the case of a copper layer with thin PCB tracks covering only a small part of the surface (in-plane conductivity set at 0.3 W/(m·K), that of the substrate). For the substrate layer, an area with a high concentration of copper vias will increase the thermal conductivity in the z-axis. This model has a relatively low number of elements (300 000).

The thermal conductivity of the substrate layer is 0.3 W/(m·K). For a substrate layer with a high concentration of vias, the z-axis thermal conductivity is increased to

Table III: Temperature comparison for both models.

Name	Approximated Layout	Detailed Layout
HF Die	129.1 °C	128.2 °C
LF Die	115.8 °C	115.6 °C
Magnetic Core	121.4 °C	125.5 °C

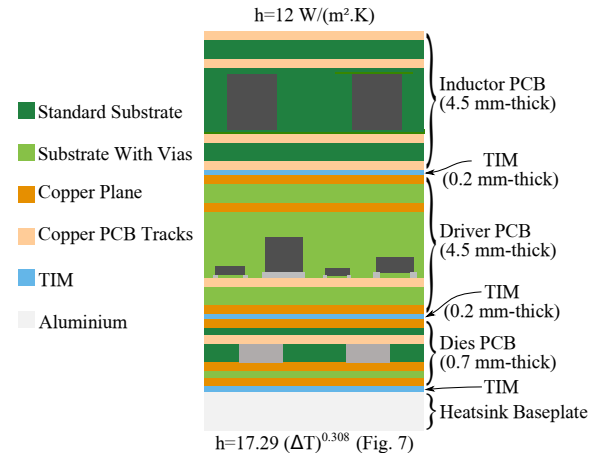


Figure 9: Stack-up used in the "Approximated layout" model.

50 W/(m·K) [19], while the thermal conductivities in the x-axis and y-axis remain the same. The thermal conductivity of the copper is 400 W/(m·K) in all directions for a plain layer. For a layer with only thin PCB tracks, the in-plane conductivities are considered to be those of the substrate layer (0.3 W/(m·K)). The heatsink is only represented by its aluminium baseplate (4 mm-thick with $\lambda = 237$ W/(m·K)). These anisotropic thermal conductivities are summarized in table I.

The boundary conditions are: a constant heat exchange coefficient on the top ($h=12$ W/(m²·K), calculated as the sum of natural air convection on a horizontal plane and heat radiation, for a 7×7 cm surface at 125 °C [20]); the heat exchange coefficient from Fig. 8 on the bottom; adiabatic condition on the sides; an ambient temperature of 60 °C. Heat is dissipated in the high and low frequency SiC dies and in the inductor. The power dissipated in each element is given in Tab. II (the calculation of these values is presented in [15]).

The structure of the model is presented in Fig. 9. Some results are presented in Fig. 10.

2) *Detailed layout model*: For this model, we directly import the detailed layout description (ODB++ file format generated from the PCB design software – Altium Designer) to build a 3D model in COMSOL. In order to simplify the model, the tracks and corresponding vias associated with the driver board are removed (the thermal vias of this board are kept). This model has 1 500 000 elements. The copper areas for the power and ground net are represented with their real layout. In this model, all thermal conductivities are isotropic.

As for the approximated layout mode, the baseplate of the heatsink and the different TIM layers are added to the model. All other simulation parameters (boundary conditions, material properties, etc.) are identical. Some results are given in Fig. 11.

C. Simulation Results

The results are listed in Tab. III. Both models predict that the junction temperature of the high frequency dies is close to 129 °C, while that of the low frequency dies is close to 115 °C (in this converter topology, half of the semiconductor dies are switching at 180 kHz while the second half only switches at the mains frequency, i.e. 50 Hz). For the inductor, the detailed

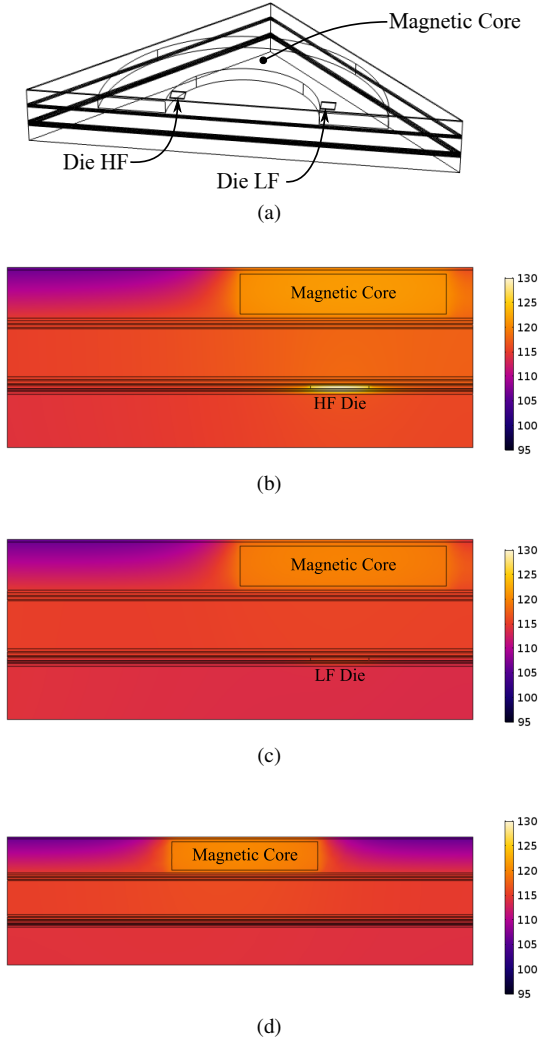


Figure 10: (a) Geometry of the "Approximated layout" model. A symmetry is used to reduce the computation time. Temperature plots over planes cutting through (b) the HF die and the center of the PCB, (c) the LF die and the center of the PCB and (d) the diagonal of the PCB.

layout model tends to predict slightly higher temperatures (125.5 °C vs. 121.4 °C), probably because the driver board only offers high conductivity only where thermal vias could be inserted (the approximated layout model considers a uniform, relatively high conductivity in the z-axis over the entire driver board).

V. THERMAL EXPERIMENT

The objective of the thermal tests presented here is to assess the accuracy of the thermal models. In these tests, a set amount of power is dissipated by the SiC dies and the inductor, and the corresponding temperature inside the PCB stack is monitored using Resistance Temperature Detectors (RTDs) embedded in the PCBs. The experiment is performed in two stages: first a calibration step allows to set the dissipated power level for the inductor, for which it is difficult to directly measure the dissipated power. In a second stage, a complete PFC cell is submitted to the same power dissipation, and its internal temperature is recorded using the RTDs.

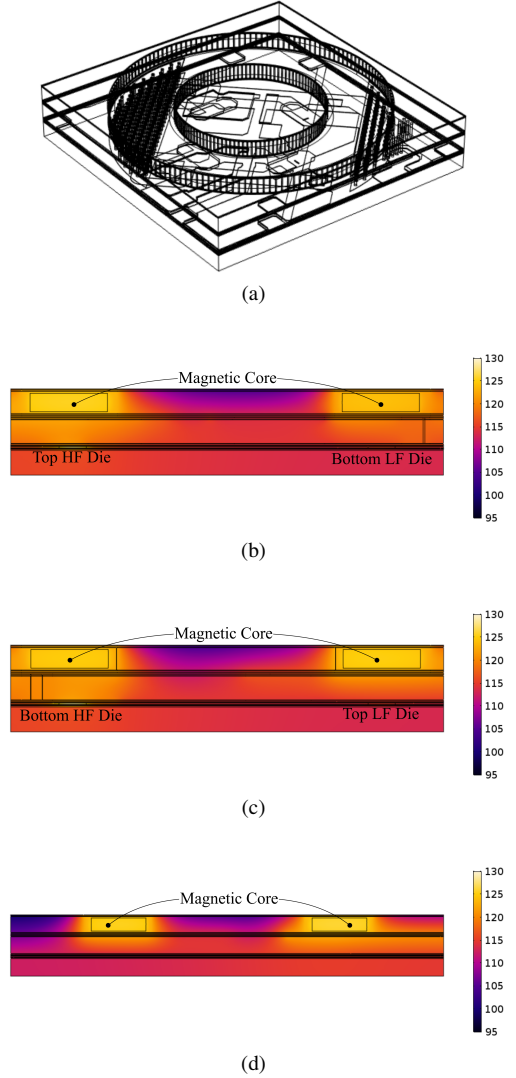


Figure 11: (a) Geometry of the "Detailed layout" model. Temperature plots over planes cutting through (b) the top HF die and the bottom LF die, (c) the bottom HF die and the top LF die and (d) a diagonal of the PCB.

A. Calibration of the Dissipated Power

The test circuit diagram used to dissipate power in the dies and inductor is presented in figure 12. Wires are soldered to the drain, source and gate of each die. The gate and the drain of each transistor are shorted together, so they can be considered as dipoles. This configuration allows to easily control the power dissipation in a transistor with a single power supply (in our case, two Source and Measure Units – references 2636 and 2602 – from Keithley, each having two independent channels as well as precision ammeters and voltmeters). Furthermore, as the transistors have a threshold voltage of around 3 V, a realistic power dissipation can be achieved with the moderate current level the sources can supply (3 A), which also has the advantage of limiting joule heating in the interconnects.

For the inductor, because (active) power dissipation is very small compared to the (mostly reactive) power involved, direct measurement of the dissipated electrical power would not be accurate. Instead, an indirect approach is chosen: calorimetry.

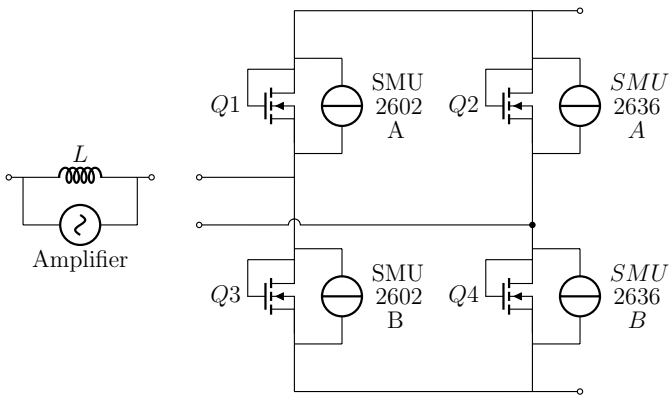


Figure 12: Circuit diagram of the thermal experiment.

Calorimetry is a simple and accurate way to measure losses. For that, the inductor is placed in a calorimeter (Figs. 14a and 14b) and supplied using an amplifier (AE Techron 7226) with a 70 kHz sinewave. This frequency is chosen to obtain the highest possible power dissipation, considering the limitations of the amplifier. The calorimeter is composed of an enclosure which ideally should be adiabatic (in our case a Dewar jar with a plastic lid). A calibration resistor, the Device Under Test (DUT) and a RTD (connected to a Keithley 2700 precision multimeter) are placed in the enclosure, and immersed in a dielectric liquid (Novec 7500, 3M). This fluid is chosen because of its relatively low toxicity, its high boiling point (128 °C), its chemical and electrical compatibility with power electronics, and because it does not leave any residue after drying. A stirrer ensures a homogeneous temperature distribution of the bath.

The principle of this measurement setup is first to estimate the total heat capacity $\sum(m_i \cdot C_i)$ of the liquid bath and all the elements it contains by dissipating a set amount of energy using the calibration resistor and measuring the corresponding temperature rise of the bath. After this calibration phase, the DUT is operated for a set amount of time, and the corresponding temperature increase of the bath is measured again, this time to calculate the losses P . Figure 13 presents an example of the bath temperature during the losses measurement step. For both steps (calibration and measurement), eq (2) is used.

$$P = \sum(m_i \cdot C_i) \cdot \frac{\Delta T}{t} \quad (2)$$

The measurement error with this setup is estimated at 4.49 %, and mainly comes from the manual control of the heating time (± 1 s). This is considered sufficient in our case. In addition, note that calorimetric measurements are performed at a bath temperature of ≈ 30 °C, and that inductor losses will increase with temperature for a constant excitation signal. This effect, however, is not taken into account here.

B. Measurement of the Internal temperature

For the thermal test, a PFC cell is assembled and raised a few centimeters above the work surface to allow air flow in the heatsink placed on the bottom. The ambient temperature is 30 °C. The Board-to-Board interconnects are replaced with thin wires to connect the dies and inductor according to

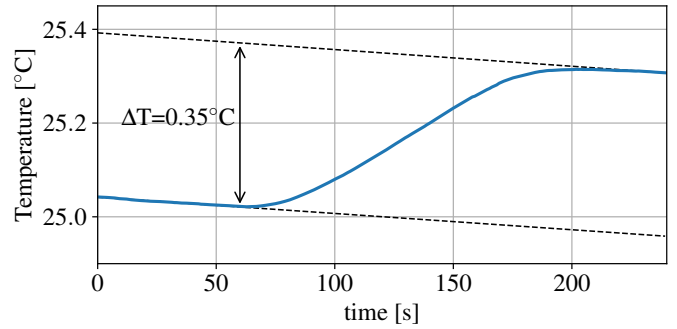


Figure 13: Bath temperature as a function of the time for the losses measurement step. The temperature difference between the two dashed lines corresponds to the temperature increase due to the operation of the DUT; the downward slope of the dashed lines is caused by heat leaks of the “adiabatic” enclosure.

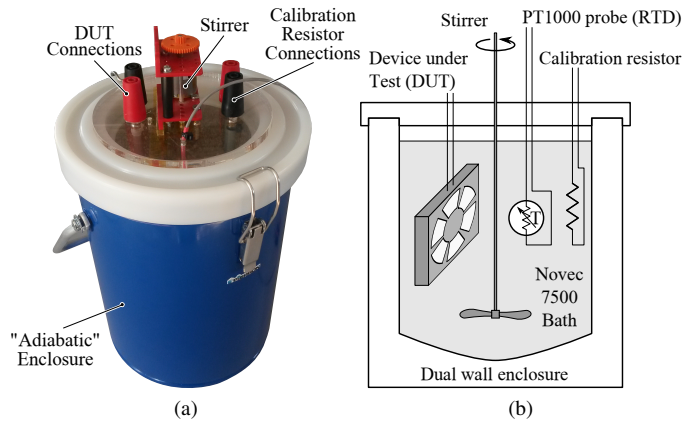


Figure 14: (a) Photograph and (b) diagram of the calorimeter. The (blue) dual wall enclosure has a diameter of 17 cm and a height of 22 cm.

Fig. 12. The power sources (in particular the AC amplifier) are set as for the calibration phase. The RTDs are monitored using a Keithley 2700 multimeter, and the temperature values are recorded after a 30 min delay.

C. Experimental Results

The losses generated in each element are presented in Tab. IV. These values are lower than those estimated during the circuit design stage (Tab. II) due to limitations with the amplifier and the SMUs.

The temperatures inside a PFC cell are measured with 6 RTDs (PT1000 in this case). 4 RTDs are placed in the driver board, directly above the MOSFET dies. The 2 remaining RTDs are placed in the inductor PCB, one in the center and the other at the exterior of the inductor. The measured ΔT (temperature difference with the ambient temperature, measured at

Table IV: Losses generated in each power element of a PFC cell for the thermal tests.

Dissipating element	Losses (W)
High Frequency Die (per die)	4.00 W
Low Frequency Die (per die)	0.81 W
Inductor	2.00 W

Table V: Comparison of the temperature difference (ΔT) between the RTDs and the ambient obtained by experiment and simulation.

RTD location	Experiment	Approximated Layout	Imported Layout
HF Die RTD	36.8 °C 35.3 °C	35.2 °C	37.6 °C 37.1 °C
LF Die RTD	33.8 °C 33.3 °C	33.6 °C	34.1 °C 34 °C
Outer Ind. RTD	27.3 °C	32.2 °C	30.9 °C
Inner Ind. RTD	30.2 °C	32.8 °C	31.2 °C

30 °C) are presented in Tab. V, along with the values calculated in the same conditions (same power dissipation, same ambient temperature) using the thermal models described above.

VI. DISCUSSION

Overall, the results given in Tab. V show a very good agreement between experiment and simulation. In particular, the ΔT for the RTDs above the dies (LF and HF) falls in-between the values predicted by both models. The maximum error for both models is 1.8 °C, which can be considered small in comparison with ΔT (>30 °C).

For the RTDs located around the inductor, there is more difference between measured and simulated values (up to 4.9 °C). Furthermore, simulation results tend to systematically overestimate the temperature. This is particularly true for the "Approximated layout" model. This model does not consider the vias which form the inductor winding (Fig. 2). This may explain the higher temperature predictions. Also, for both models, a constant heat exchange coefficient value is considered on top of the PCB stack. This coefficient, however, is highly dependent on the temperature difference with the ambient.

The "Detailed layout" model tends to give results which are closer to the experiments, despite the simplifications which were performed to obtain an automated mesh. The computation time is 30 min. An advantage of this model is the ease to describe the geometry of the board, as it is directly imported from Altium Designer. However, a manual alteration of the layout is still required to remove the finest tracks and some vias to make it compatible with automated meshing. The "Approximated layout" model tends to result in slightly larger errors, which remain acceptable for the dies. Its computation time is smaller (2 min). An advantage of this model is that its generation can be automated (by calculating the copper fraction of each layer and the density of vias from the layout files).

In conclusion, both models generate satisfying results. The "Approximated layout" model is especially attractive. Indeed, it makes it possible to compute the accurate temperature distribution of a complex PCB stack in a few minutes. A possible refinement of this model is to consider subdivisions of each layers (for example 1 cm² areas), each with their own thermal conductivities (to better match the layout of the boards). This would not require more elements in the mesh (for this model, the element size is dictated by the layer thickness,

so that the element form factor remains acceptable), and would therefore not take longer to simulate.

Regarding the simulations presented in section IV-C (i.e. with the power dissipation level predicted by the circuit simulation and a worst case ambient temperature of 60 °C), the thermal models predict that all components remain at acceptable temperatures. The high frequency dies, which are the hottest points in the structure, are far from their quoted maximum junction temperature (175 °C). The gate driver IC, which has a maximum temperature of 125 °C, runs closer to its limits, with a calculated temperature of 123.8 °C. Running so close to the limit might be an issue, as it removes any safety margin for overload operation. A design iteration could be performed, based on the FEM simulations, to move the gate drivers to a milder place on the same PCB. In our case, in the absence of specifications regarding overload or other extreme operation cases, we consider that the current design meets the specifications.

VII. CONCLUSION

A 3.3 kW AC/DC bidirectional converter stage has been implemented using 3 different boards: one for the semiconductor dies, one for the gate drive circuits, and one for the inductor. The manufacturing process has been described. To form a converter, all three boards were stacked on top of a heatsink.

Two modeling approaches were proposed for the stack: one is based on a simple approximation of each layer of the board, while the second considers a more accurate description of the board layout. Both models have been compared to experimental results, and show a good accuracy, especially for the dies). Regarding the inductor, the error is larger (up to 4.9 °C difference between simulation and experiment).

Applying these models to the expected operating conditions of the converter show that the components temperatures should remain within specification. This is true despite the poor conductivity of the PCB substrate material and the thickness (\approx 1 cm) of the PCB stack. This demonstrates that with careful implementation, PCB embedding technology may be used for medium-power converters.

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