A Compact Active Phaser with Enhanced Linearity of Group Delay for Analog Signal Processing

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Abstract— **This paper presents a wideband compact phaser with a linear group delay, a key block to many Analog Signal Processing applications as Real-Time Fourier Transforming systems (RTFT). The phaser, designed in a 130 nm BiCMOS technology, presents a group delay dispersion of 3 ns, a layout area of only 30 µm by 330 µm and power consumption of 7.2 mW. Between 300 MHz and 2.5 GHz, the linearity error of the group delay is lower than 5%. The enhanced linearity of the group delay has been obtained thanks to an association of active first-order all-pass filters and active second-order all-pass filters. The benefit of using exclusively active components are the reduced layout area and the signal amplification achieved by the phaser.**

Keywords— **phaser; dispersive delay line; group delay; Analog Signal Processing;**

I. Introduction

Most of the receivers and transmitters nowadays are built on the idea that they are only dedicated to digital signal processing. In this context, the analog front end is only reserved to the signal conditioning before the analog-to-digital conversion (low noise amplifiers, mixers, analog-to-digital converters) or to the amplification before transmission (digital-to-analog converter, power amplifier). However, a new research trend consists in rethinking the transceiver architectures in order to include Analog Signal Processing (ASP) [1]. The signal processing operations that can be achieved directly in the analog domain are: time-compression, time-expansion, and Real-Time Fourier Transformation (RTFT). The key component for any of these signal processing applications is the phaser. The phaser, sometimes also referred to as Dispersive Delay Line (DDL) or chirp filter, is a device presenting an arbitrary group delay characteristic in a certain range of frequencies. Most of the ASP applications require a linear group delay characteristic. Many implementations of phasers have been published in [2-8]. Among these implementations, only a few have been implemented using a monolithic integrated circuit approach. The main difficulties encountered when designing a device with linear group delay characteristics are: cumbersome resulting devices due to passive components, nonlinear group delay characteristic and trade-off between the group delay dispersion and the bandwidth.

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In this paper, a new approach is proposed to obtain a compact integrated phaser with improved linearity of group delay characteristic. The idea is to massively use first-order active all-pass filter with increased bandwidth. Contrary to common use, these all-pass filters will be used in the frequency range having a dispersive group delay. This dispersive group delay is not linear versus frequency. Then, in order to compensate this nonlinearity, active second order filters are added.

The paper is organized as follows. Section II presents the proposed methodology based on high level considerations to obtain a highly linear group delay characteristic. Section III describes the proposed architecture of the phaser at transistor level. Section IV presents the layout, post-layout simulation results, comparison with other work and results obtained with the phaser at transistor level in a frequency discriminator.

II. Proposed Methodology to Obtain a Linear Group Delay Characteristic

The methodology proposed here is based on the principle that all delay cells (first-order and second-order) are matched. This assumption is true if the real and imaginary parts of the input/output impedances of the cells have about the same value (approximately match). In that case, the total group delay is simply the sum of each group delay.

A. All-pass first-order cell

The idea here is to use first-order all-pass filters not in their constant delay part but at higher frequencies where the group delay is dispersive. The first-order all-pass filter has the following transfer function:

$$H_{1st}(j\omega)=\frac{j\omega-\omega_0}{j\omega+\omega_0}, \quad (1)$$

where ω_0 is the cutoff pulsation of the low-pass term. The group delay of this filter is:

$$\tau_{1st}(\omega)=\frac{2\omega_0}{\omega_0^2+\omega^2}. \quad (2)$$

B. All-pass second order cell

The generic second order all-pass filter has the following transfer function:

$$H_{2nd}(j\omega)=\frac{-\omega^2-\frac{\omega_0}{Q}j\omega+\omega_0^2}{-\omega^2+\frac{\omega_0}{Q}j\omega+\omega_0^2}, \quad (3)$$

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where ω_0 is the resonance pulsation and Q the quality factor. And it can be demonstrated that the group delay of this filter is:

$$\tau_{2nd}(\omega) = \frac{2}{Q} \frac{\omega_0^2\left(\omega^2 + \omega_0^2\right)}{\omega_0^4 + \omega_0^2\omega^2\left(\frac{1}{Q^2} - 2\right) + \omega^4} \quad . \tag{4}$$

C. *Linear group delay filter*

To obtain the required characteristic of group delay, first-order all-pass filters (N_{1st}) are cascaded with a couple of second order all-pass filters (N_{2nd}). In that case, the resulting group delay is simply the sum of each group delay:

$$\tau_{total}(\omega) = \sum_{i=1}^{N_{1st}} \tau_{1st\_i}(\omega) + \sum_{i=1}^{N_{2nd}} \tau_{2nd\_i}(\omega) \, . \tag{5}$$

If we consider the ideal linear group delay characteristic with a gradient k in a certain frequency range:

$$\tau_{ideal}(\omega) = \tau_0 - k\omega \ , \tag{6}$$

and if all first-order filters and all second order filters are identical, it is possible to find the parameters α, ω_0 and Q to minimize the criteria:

$$J = \sum \left| \tau_{total}(\omega) - \tau_{ideal}(\omega) \right|^2 \, . \tag{7}$$

In what follow we will use this principle to design a phaser integrated with the technology 130 nm from STmicroelectronics.

III. PROPOSED ARCHITECTURE OF THE PHASER

The phaser is composed of sixteen first-order time-delay cells and two gyrator circuits. The choice and the design of these cells are justified in the two next sections.

A. *First-order cell*

The time delay circuit proposed in [9], [10] presents the advantage of an extended bandwidth. It has been selected for implementing a part of the phaser. In what is proposed here, and contrary to common use, these time-delay cells will be used in the frequency range having a dispersive group delay characteristic. The transfer function of the time delay cell is:

$$\frac{V_{out}}{V_{in}} = \frac{-j\omega + \frac{g_m}{C}}{j\omega + \frac{g_m}{C}} , \tag{8}$$

where g_m is the transconductance of the PMOS transistor on the left of the first-order all-pass cell presented (c.f. Fig. 1); and C is the total capacitance on the gate node (referred as node A in schematic). In our case no extra capacitors will be added to the design, so C will be composed of parasitic capacitances only. The group delay associated to Eq. (8) is:

$$\tau_{1st}(\omega) = \frac{2\frac{g_m}{C}}{\left(\frac{g_m}{C}\right)^2 + \omega^2} \, . \tag{9}$$

This expression of the group delay is coherent with the one expected from Eq. (2). Figure 1 presents the schematic of two first-order delay cells with a bias stage and an amplifier stage. As presented in [10] only one bias stage is needed at the beginning of the cascade, with an AC-coupling capacitor to the input RF signal. Each first-order all-pass cell has a gain smaller than one. Due to the large number of cells mandatory to reach the required group delay dispersion, an amplifier stage is added every two cells to avoid the attenuation of the signal. This amplifier stage is composed of a transistor and a resistor. Transistors sizes are W_p = 6 µm, W_n = 1.5 µm, W_{bias} = 150 nm and $C_{coupling}$ = 1 pF. In this part of the circuit, all gate lengths have been chosen equal to 200 nm.

B. *Second order cell*

For the second-order time-delay cell a gyrator is proposed to obtain a transfer function close to Eq. (3). The proposed gyrator circuit is the first stage of the circuit presented in Fig. 1. The transistors and resistor M1, R_{gyr}, M2 and M3 consist in a positive transconductance circuit (G_{m1}). M4 and M5 consist in a negative transconductance circuit (G_{m2}). For this circuit, the transfer function is:

$$\frac{V_{out}}{V_{in}} = \frac{\frac{G_{m1}}{C_{par1}C_{par2}R_{out2}} + j\omega\frac{G_{m1}}{C_{par1}}}{-\omega^2 + j\omega\left(\frac{1}{C_{par1}R_{out1}} + \frac{G_{m1}G_{m2}}{C_{par2}}\right) + \frac{1 + G_{m1}G_{m2}R_{out2}}{C_{par1}C_{par2}R_{out1}R_{out2}}} , \tag{10}$$

where R_{out1} and R_{out2} are the output resistances of G_{m1} and G_{m2} and C_{par1} and C_{par2} the output parasitic capacitances at the output of G_{m1} and G_{m2}. From Eq. (10), and considering identical values of G_m, R_{out} and C_{par} for the two stages, we can calculate the group delay as:

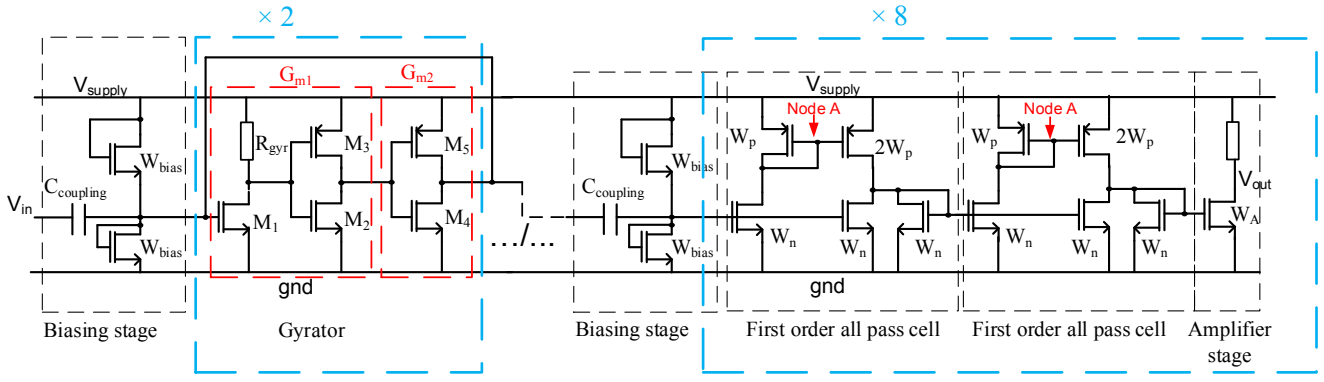

Fig. 1. Complete phaser circuit.

$$\tau_{2nd}(\omega)=\frac{\mu\beta+\omega^2(3B\beta-\mu\gamma)+B\gamma\omega^4}{\beta^2+\omega^2(\mu^2+2\beta\gamma)+\omega^4(2\mu\beta+\gamma^2)+\omega^6B^2}, \quad (11)$$

where the variables μ, β, γ, and B are:

$$\begin{cases}\mu=\dfrac{G_m^3(1-R_{out})}{R_{out}C_{par}^3}\\ \beta=\dfrac{G_m(1+G_m^2R_{out}^2)}{R_{out}^3C_{par}^4}\end{cases} \text{ and } \begin{cases}\gamma=\dfrac{G_m^2}{C_{par}^2}\\ B=\dfrac{G_m}{C_{par}}\end{cases} . \quad (12)$$

Sizes of transistors have been determined to obtain a G_m around 8 mS. This value provides the required group delay characteristic to improve the linearity of 16 first-order delay cells. The W/L of transistors in μm/μm are: M1: 1/0.13, M2: 9.2/0.13, M3: 19.8/0.13, M4: 9.2/0.13. The value of R_{gyr} is 8.4 kΩ.

IV. Performances and Application in a Frequency Discriminator

A. Performances and comparison with other works

Figure 2 presents the total group delay characteristic obtained at transistor level and post-layout level. At transistor level, the range where the linearity error is lower than 5% is comprised in the range 300 MHz up to 2.5 GHz. At post-layout level dispersion is increased (up to 4ns) and linearity bandwidth slightly reduced. The voltage gain characteristic of the phaser is presented in Fig. 3 at transistor level and post-layout level. It shows that the phaser behaves like a voltage amplifier between 2.5 MHz and 3 GHz, with a maximum gain of 40 dB. Post-layout results could still be made closer to transistor level (for gain and group delay) by slightly modifying the dimensioning.

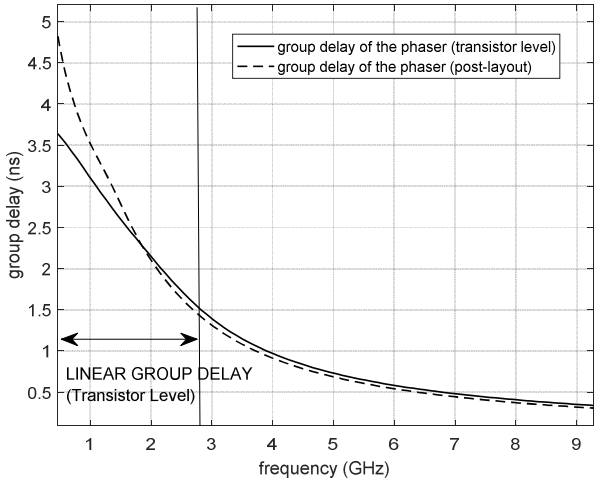

Fig.2 Total group delay resulting from the cascades of gyrator with all-pass first-order time delay circuits at transistors level and post layout level.

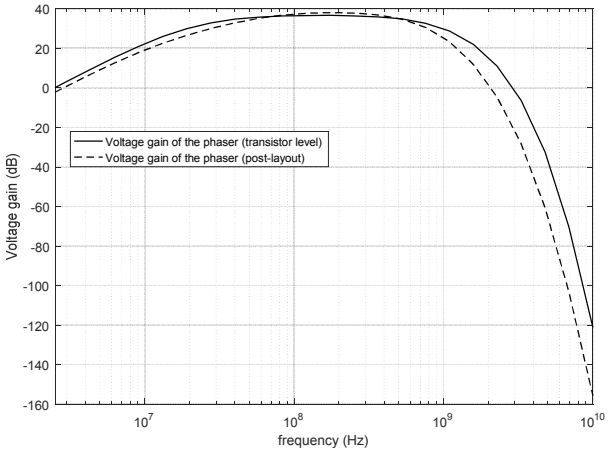

Fig. 3. Voltage gain characteristic of the phaser at transistors level and post layout level.

The circuit layout is presented in Fig. 4. The total area is 30 μm by 330 μm. The total power consumption is 7.2 mW. Power consumption of each gyrator is 1.2 mW, and each two-stage first-order pass cell followed by an amplifier consumes about 0.6 mW. To the authors' knowledge, this is the most compact implementation of a phaser, and the power consumption remains low compared to other designs. In Table I, other performances are also considered: frequency range, group delay dispersion, linearity of the group delay characteristic and power consumption. Compared to previously published implementations, excluding technologies like SAW (Surface Acoustic Wave) filters and optical devices, the dispersion of group delay obtained in this work is greater than in other implementations. Group delay linearity has not been quantified in the previous works, despite its importance in analog signal processing applications.

B. Application of the designed phaser: a frequency discriminator

Among the possible applications of the phaser, there is the frequency discriminator, also referred to as Real-Time Fourier Transformer as presented, for example, in [3]. The principle of such a device is to separate frequency components from a stationary signal by measuring the delay for each of the components. To do so, the signal considered for analysis is multiplied by a triangular window. The resulting signal is then applied to the phaser. If the phaser has a group delay decreasing with frequency as it is the case in this paper, then the higher frequencies will arrive before the lower frequencies. In the present case, the triangular signal has a width of 3 ns (1.5 ns rise time, 1.5 ns fall time) to be able to analyze signals from 500 MHz up to few GHz. The delay obtained for 800 MHz (c.f. Fig. 5) is 3.2 ns, and the delay obtained for 2.5 GHz (c.f. Fig. 6) is 1.7 ns.

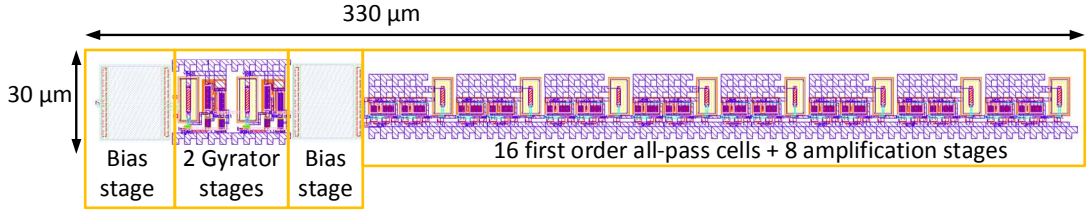

Fig. 4. Layout view of the complete phaser.

It demonstrates that the behavior of the phaser is in adequation with the group delay characteristic presented in Fig. 2 and that it can be used in an analog signal processing application.

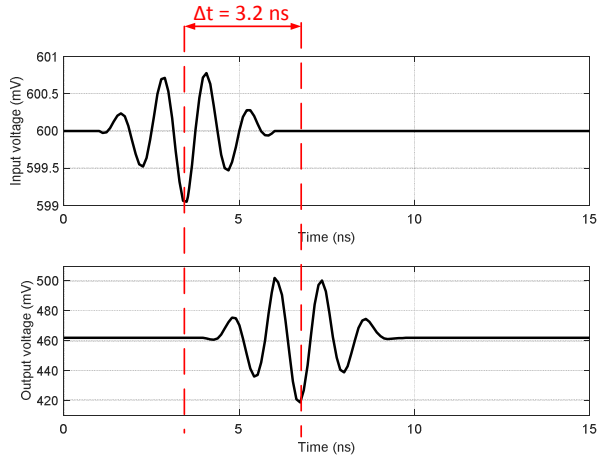

Fig. 5. Input and output voltage of the frequency discriminator for a 800 MHz input signal.

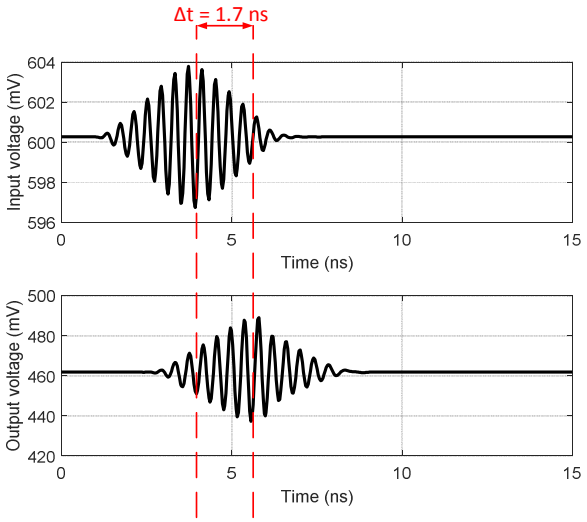

Fig. 6. Input and output voltage of the frequency discriminator for a 2.5 Ghz input signal.

V. Conclusion

This paper has presented the design of an active compact wideband phaser, which is a key block in many Analog Signal Processing applications. The design has been made with a ST 130 nm BiCMOS technology. Power consumption is 7.2 mW. The phaser circuit is composed of an optimized cascade of first-order and second-order delay cells to obtain a linear group delay characteristic. The circuit is simulated in a frequency discriminator to prove its efficiency for analog signal processing applications.

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TABLE I. Simulation Results Summary and Comparison

Reference	[3]*	[4]*	[5]*	[9]*	[10]*	This Work
Freq. range (GHz)	4-8	0.4-4	11-15	1-5 and 1.6-2.6	8-12	0.5-4
Technology	PCB	0.13 µm CMOS	0.13 µm CMOS	PCB	GaN-on-SiC 0.25 µm	0.13 µm BiCMOS
Size	Several mm^2	1.6 × 5 mm^2	1.5 × 4.7 mm^2	Several mm^2	3.7 x 4.2 mm^2	30 × 315 μm^2
Group delay dispersion	2.1 ns	1.2 ns	≈1 ns	1 ns and 7 ns	0.6 ns	3 ns
Groud delay slope	-0.5 ns/GHz	0.5 ns/GHz	≈0.25 ns/GHz	≈0.2 and 7 ns/GHz	NA	≈ -1 ns/GHz
Group delay linearity	NA	NA	NA	Highly linear**	Quadratic	5% error max. in 0.8 to 2.5 GHz
Power consumption	passive	450-750 mW	NA	passive	2.47 W	7.2 mW

*design with measured values, **no numerical value for linearity