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# Process-Voltage-Temperature Analysis of a CMOS-MEMS Readout Architecture

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**Abstract**—Thermal drift is one of the main issues limiting the performance of resonant MEMS sensors. Their impact may be minimized at several levels, such as specific system-level solutions (e.g. differential sensing) or mechanical design (e.g. privileging suspended structures). While solving these issues is essential, one should not overlook the temperature-dependence of the readout and oscillation-sustaining electronics associated to the resonators. Considering monolithic CMOS-MEMS devices, thermal drift of the electronics becomes the main challenge, when off-the-shelf building-blocks are used over a large temperature range (from  $-40^{\circ}\text{C}$  to  $175^{\circ}\text{C}$ ). In this paper, a process-voltage-temperature analysis of electronics readout is carried out to illustrate this issue. Proposed analysis shows that the phase-difference between the motional signals decreases monotonically with temperature. In extreme voltage-temperature conditions for  $-3\sigma$  variability, phase-difference achieves  $-7.2^{\circ}$  at  $175^{\circ}\text{C}$ ,  $V_{DD} = 1.62\text{ V}$ ; and  $5^{\circ}$  at  $-40^{\circ}\text{C}$ ,  $V_{DD} = 1.98\text{ V}$ . This result highlights the need of CMOS / MEMS co-design and optimization tools, for improving the thermal stability of resonant sensors in high-end, extreme environments such as automotive applications.

**Index Terms**—Thermal stability, CMOS-MEMS, resonant sensors, differential sensors

## I. INTRODUCTION

Thermal drift is one of the main issues limiting the performance of resonant MEMS sensors in high-end applications, where temperature stability is essential. The temperature-dependence of Young's modulus, axial stress and, more generally, of the mechanical properties of materials are well-known causes of thermal instability. Research is actively conducted to address these issues such as specific solutions from system- to mechanical-level. A common solution in system-level is differential sensing. Most of published works addresses differential sensing solutions by using: two coupled [1], [2] or uncoupled resonators [3], [4]. In this case, such resonators should have a matched or well-known resonance frequencies and temperature coefficients [5]. To avoid such drawbacks, some works use a single resonator with two vibrational modes [6]. In mechanical-level, resonators' temperature compensation may also be: actively enforced with a micro-oven [7], achieved with linear or nonlinear electrostatic tuning [8], [9], with specific mechanical design as privileging suspended structures, fabrication and packaging steps [10].

While solving these issues is essential, one should not overlook the temperature-dependence of the readout and oscillation-sustaining electronics associated to the resonators. In high-end and automotive applications, off-the-shelf electronic building-blocks do not often have the required ther-

mal stability for resonant sensors. Electronic sensitivity to environment variations is indeed high when process-voltage-temperature (PVT) variations are considered. Recent works have been interested in: the implications of small geometry effects [11], process-variability mitigation techniques for digital gates [12], the variation of comparator's delay over temperature [13], defining process-voltage-temperature (PVT) tolerant circuits [14], and minimizing thermal noise in CMOS amplifiers [15]. Furthermore, aforementioned system-level solutions require a differential architecture which are affected by mismatch issues between paths [16].

To illustrate the importance of thermal stability in monolithic CMOS-MEMS devices, this work proposes a PVT analysis of the CMOS readouts and the oscillation-sustaining electronics commonly associated to a family of differential weakly-coupled resonators [2]. This study focuses on the loss of sensor accuracy resulting from PVT variations, when off-the-shelf components are used. All circuit design is carried out using SOI 180 nm process technology from the XFAB Silicon Foundries. Being a standard in high-end and automotive applications, XFAB's technology possess transistor models for  $V_{DD} = 1.8\text{V} \pm 10\%$  and temperature variation from  $-40^{\circ}\text{C}$  to  $175^{\circ}\text{C}$ . Post-layout (PSL) simulations of the readout architecture are presented.

In Sec. II of the paper, the system-level architecture of the sensor is presented. The electronic design of the readout and oscillation-sustaining electronics is given in Sec. III. Section IV is dedicated to the analysis of PSL simulation results. Finally, concluding remarks and perspectives are drawn.

## II. SENSOR ARCHITECTURE

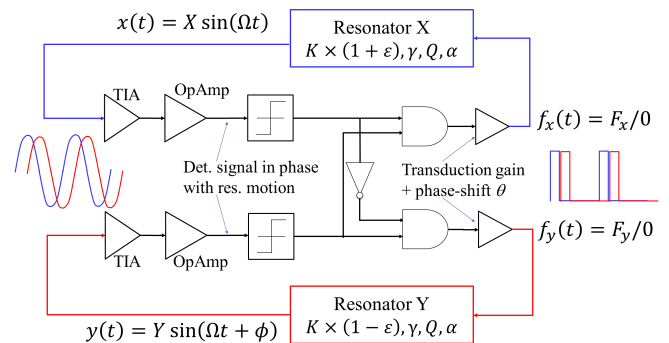


Fig. 1. CMOS-MEMS readout architecture: system-level illustration.

The architecture is based on two ideally identical, frequency-matched resonators, with matched temperature coefficients and quality factors. The relative stiffness mismatch between the resonators is denoted by  $\varepsilon$  (see Figure 1), and is proportional to the physical phenomenon one seeks to measure. The MEMS resonators are actively coupled through a nonlinear mixer. With the proper amount of phase-shift between the output of the resonator readouts and the mixer outputs [2], the phase difference  $\theta_x - \theta_y$  (in radians) between the resonators  $x$  and  $y$  is equal to

$$\phi = \frac{\pi}{2} \cdot (1 + 2Q\varepsilon), \quad (1)$$

where  $Q$  is the resonator quality factor. Thus,  $\phi = \frac{\pi}{2}$  when  $\varepsilon = 0$ , and the deviation of the phase difference from this value can be used as a highly sensitive output metric for sensing stiffness mismatch  $\varepsilon$ .

Induced by thermal mismatch in the differential branches, the phase-shift in (1) may become slightly off by an amount  $\Delta\theta = \theta_x - \theta_y - \frac{\pi}{2}$  (expressed in radians). Thus, the above relation becomes

$$\phi = \frac{\pi}{2} \cdot \left( 1 + 2Q \left( \varepsilon + \frac{\sqrt{2}}{2Q} \cdot \Delta\theta \right) \right). \quad (2)$$

So that, the (input-referred) phase error increases linearly with  $\Delta\theta$  and is inversely proportional to  $Q$ . For resonators with moderate quality factors minimizing the fluctuations of  $\Delta\theta$  with temperature becomes critical to limit thermal drift.

In the following sections, similar resonators to the ones in [2] are considered (see Fig. 2(a)). Original resonance frequency is 3.79 MHz and quality factor in air is 120. Resonators can accurately be modeled with a simple Butterworth Van-Dyke model (see Fig. 2(b)). Electrical model is here scaled from [2] to consider vacuum operation and a higher bias voltage  $V_b$ . The resonators have the following electrical parameters corresponding to  $f_0 = 3.62$  MHz and  $Q = 2700$ , i.e.  $R_m = 64.4$  k $\Omega$ ,  $L_m = 7.7$  H, and  $C_m = 250$  aF. Additionally,  $C_{ft} = 500$  aF and  $C_{elec} = 4.6$  fF to consider the effects of feedthrough and parasitic in a monolithic integration.

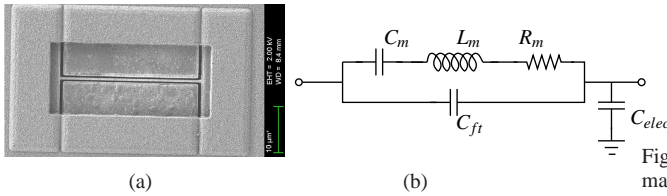


Fig. 2. MEMS sensor based in a 30  $\mu\text{m}$ -long clamped-clamped beams (CCB): (a) microscope photograph, (b) Butterworth Van-Dyke model[2].

### III. CMOS READOUT ARCHITECTURE

CMOS readout architecture, illustrated in Figure 1, is implemented by: a TIA, a Op Amp, a comparator, and a mixer; for each branch of the differential sensing [2]. Off-the-shelf Miller OTAs are used to implement the transimpedance amplifiers (TIA), voltage amplifiers (OpAmp), and comparators; standard

cells are used to implement the digital mixer. Transistor-level design is carried out using XFAB SOI 180 nm technology to reach the following specification: DC gain is 74 dB; the unity-gain frequency is 316 MHz; the slew rate is 231.5 V/ $\mu\text{s}$ ; the power consumption is 707  $\mu\text{W}$ ; and the dynamic range is 1.3 V peak-to-peak.

SOI 180 nm process technology from the XFAB Silicon Foundries is ideal for system-on-chip (SoC) applications in the automotive market such as control devices inside combustion engine compartments or electric engine housings with temperature range up to 175  $^{\circ}\text{C}$ , as well as embedded low-voltage applications in the communications, consumer and industrial market [17]. Such technology is a SOI process, which uses a deep-trench buried oxide that leads to a very low junction leakage current even at high temperatures. According to foundry models, it is reported 3 pA of leakage current for measured transistors with 10 nA of drain-to-source bias current and 100 pA leakage for 80  $\mu\text{A}$  bias current at 175  $^{\circ}\text{C}$ .

Even using a specific technology for high-temperature operation off-the-shelf devices suffers from PVT variations. Considering the Miller OTA under study, one may verify that the phase characteristics of such block is not constant at resonator frequency for all operating conditions. Figure 3 illustrates what may happen when off-the-shelf Miller OTA operates, considering 101-points Monte Carlo simulation for process mismatch  $3\sigma$  Gaussian distribution, 21-points temperature variation from -40  $^{\circ}\text{C}$  to 175  $^{\circ}\text{C}$ , and  $V_{DD} = 1.8\text{V} \pm 10\%$  (i.e. 3-points) voltage variation. Typical performance is illustrated in black ( $\mu$ , 1.8V); worst-case conditions are in blue ( $\mu + 3\sigma$ , 1.62V) and in red ( $\mu - 3\sigma$ , 1.98V). Indeed, expected phase at 3.6 MHz varies from 90.5 $^{\circ}$  to 91 $^{\circ}$  in typical conditions, but it may vary from 89 $^{\circ}$  to 92.5 $^{\circ}$  in worst-case conditions.

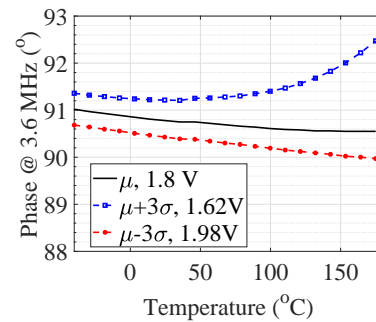


Fig. 3. Off-the-shelf Miller OTA phase shift at 3.6 MHz. Typical performance is illustrated in black ( $\mu$ , 1.8V); worst-case conditions are in blue ( $\mu + 3\sigma$ , 1.62V) and in red ( $\mu - 3\sigma$ , 1.98V).

### IV. PSL SIMULATION RESULTS

Fig. 4 illustrates the final layout CMOS-MEMS MILO architecture having an area of 207 x 106  $\mu\text{m}^2$ . Process-Voltage-Temperature analysis is carried out using transient and steady-state simulation. Phase-shifts  $\theta_x$  and  $\theta_y$  are estimated through the readout. When  $\varepsilon = 0$ ,  $\theta_x = 0$  and  $\theta_y = 90^{\circ}$ , thus and ideal  $\Delta\theta = \theta_x - \theta_y - 90^{\circ} = 0$  is obtained. Following results are presented in terms of  $\theta_x$ ,  $\theta_y - 90^{\circ}$ , and  $\Delta\theta$  in degrees

to improve readability. Process variation is analyzed using a 101-points Monte Carlo simulation for process mismatch  $3\sigma$  Gaussian distribution. Temperature variation is analyzed using a 21-points simulation from  $-40^\circ\text{C}$  to  $175^\circ\text{C}$ . Voltage variation is analyzed at  $V_{DD} = 1.8\text{V} \pm 10\%$  (i.e. 3-points).

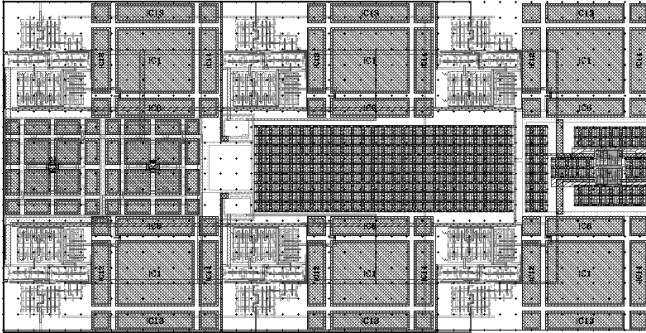


Fig. 4. CMOS-MEMS MILO architecture: layout area of  $207 \times 106 \mu\text{m}^2$ .

Root-mean-squared power consumption is found at  $6.7 \text{ mW}$  during steady-state operation with nominal  $V_{DD}$  and at  $27^\circ\text{C}$ . Voltage-temperature analysis is then carried out. Figure 5 shows a decreasing power consumption with temperature for all  $V_{DD}$ . This is hardly an advantageous behavior. In fact, it means that the performance of the off-the-shelf Miller OTAs is degraded at high temperatures, due to gain decrease, transition frequency reduction and phase shift (see Sec. III). Addition simulations (not presented) show that the delay of the digital standard-cells increases over voltage-temperature variations confirming the results presented in the literature [12], [13].

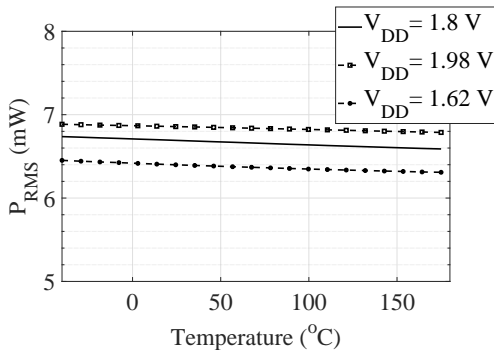


Fig. 5. Readout post-layout result: power consumption for 21-points temperature, voltage variation at  $V_{DD} = 1.8\text{V} \pm 10\%$  (i.e. 3-points) and typical process model simulations.

Figure 6, obtained with steady-state analysis, illustrates the combined effect of these trends on the phase difference output metric. Phase-shift  $\theta_x$  decreases quasi-linearly with temperature by  $10^\circ$  over the temperature range, mainly as a result of performance degradation in the off-the-shelf devices. On the other hand,  $\theta_y$  decreases quasi-linearly with temperature by  $6^\circ$  over the temperature range. In high-voltage ( $V_{DD} = 1.92 \text{ V}$ ) and low-temperature ( $T \leq 0^\circ\text{C}$ ),  $\theta_y$  presents a non-linear variation  $3^\circ$  below the values in other conditions. The different

phase shift of  $\theta_x$  and  $\theta_y$  is due to the extra logical gate (see Fig. 1), which is detrimental to the symmetry of the system. MILO architecture, here presented, uses of a back-to-back inverter latch circuit as comparator charge followed by a larger inverter to minimize the propagation delay to and gates. Consequently, the decreasing  $\Delta\theta$  is worse than  $-3^\circ$  in high-temperature ( $T \geq 70^\circ\text{C}$ ) operation. Besides the non-linear behavior in low-temperature ( $T \leq 0^\circ\text{C}$ ) results in a  $\Delta\theta$  is worse than  $-2^\circ$ .

Process-temperature analysis is then carried out. Figure 7(a) highlights a  $\theta_x$  decreasing with temperature similar to VT-analysis. The  $\theta_x$  variability is in the interval from  $-1^\circ$  to  $-3^\circ$  in high-temperature ( $T \geq 70^\circ\text{C}$ ). Figure 7(b) shows that the average value of  $\theta_y - 90^\circ$  is also decreasing with temperature. For the  $\theta_y - 90^\circ$ , the worst-case is in the interval from  $-4^\circ$  to  $-5^\circ$  in high-temperature ( $T \geq 70^\circ\text{C}$ ). Comparing  $\theta_x$  and  $\theta_y - 90^\circ$  results, one may conclude that the estimated  $\sigma$  is constant over temperature. Such characteristic is reinforced under process mismatch, where  $\Delta\theta$  presents a worst-case result of  $-5^\circ$  (see Fig 7(c)). However, Monte Carlo results considering global variations would require an additional  $V_b$  bias tuning to guarantee the MEMs lock-in. Presented analysis thus highlights a temperature range ( $0^\circ\text{C} < T < 70^\circ\text{C}$ ) limitation in agreement with reported results [1], [2].

One may compare the error in (2) caused by the variation of  $\Delta\theta$  over the temperature range to the error resulting from thermomechanical noise in the resonators. When these oscillate with their amplitude equal to 5% of the gap, the input-referred rms error (expressed in terms of relative stiffness mismatch  $\epsilon$ ) from thermomechanical noise at  $175^\circ\text{C}$  integrated over the oscillator bandwidth ( $f_0/2Q$ ) is equal to  $2.8 \cdot 10^{-9}$ . On the other hand, a change of only  $1^\circ$  in  $\Delta\theta$  results in an input-referred error equal to  $137.8 \cdot 10^{-9}$ . In extreme voltage-temperature conditions for  $-3\sigma$  variability,  $\Delta\theta$  achieves  $-7.2^\circ$  at  $175^\circ\text{C}$ ,  $V_{DD} = 1.62 \text{ V}$ ; and  $5^\circ$  at  $-40^\circ\text{C}$ ,  $V_{DD} = 1.98 \text{ V}$ . Increasing the resonator quality factor, as suggested in this paper, decrease both of these errors in the same proportions, so that the sensor could be more accurate. However, thermal stability still is the limiting factor; and the input-referred error is still dominated by  $\Delta\theta$  variations. Furthermore, the suggested increase of the quality factor (i.e. by operating the resonators in vacuum) will result in other practical issues to heat evacuation at the packaging level and at the system level.

## V. CONCLUSIONS

Thermal drift is one of the main issues limiting the performance of resonant MEMS sensors. Their impact may be minimized at several levels, such as specific system-level solutions or mechanical design. This work has highlighted the fact that thermal stability issues in resonant sensing applications should not be envisioned from the point of view of the mechanical structure only. By using off-the-shelf building-blocks for electronic design, readout may suffer of an increasing thermal drift limiting sensors operation in high-end applications. Temperature-aware readout design should then be considered, and, in differential architecture as discussed in the paper, signal path calibration techniques [16].

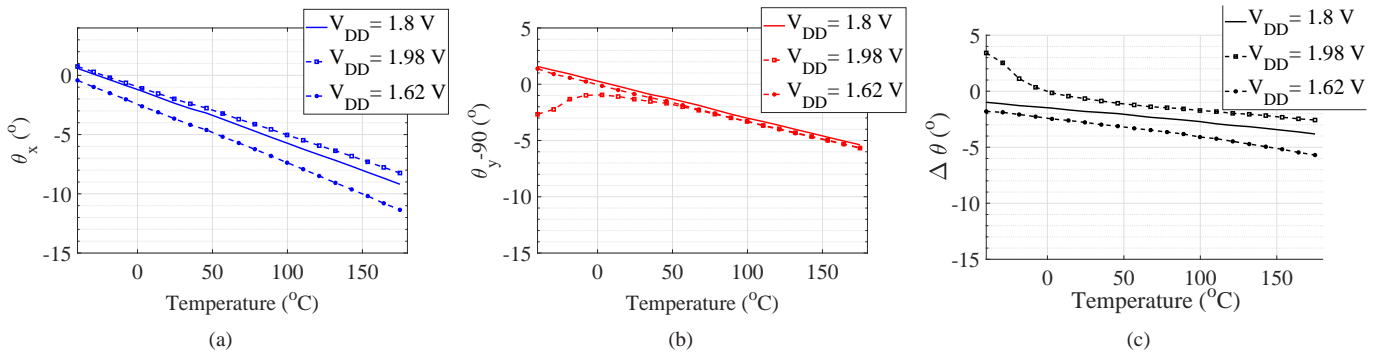


Fig. 6. Readout post-layout result: PVT analysis for 21-points temperature, voltage variation at  $V_{DD} = 1.8V \pm 10\%$  (i.e. 3-points) and typical process model simulations:(a)  $\theta_x$ , (b)  $\theta_y - 90^\circ$ , and (c)  $\phi - 90^\circ$ .

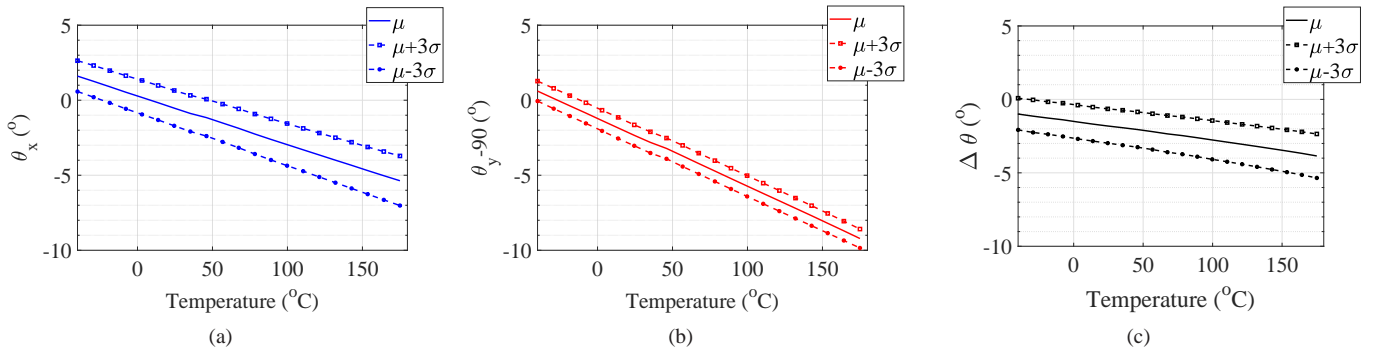


Fig. 7. Readout post-layout result: PVT analysis for 21-points temperature,  $V_{DD} = 1.8 V$ , and 101-points Monte Carlo simulations:(a)  $\theta_x$ , (b)  $\theta_y - 90^\circ$ , and (c)  $\Delta\theta$ .

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