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# Ka BAND TEST FIXTURE WITH DC BIAS CIRCUIT FOR ACTIVE DEVICE CHARACTERIZATION

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## ABSTRACT

*This paper presents the S parameter measurements of PHEMT chip transistors in the Ka band. The transistor is mounted on an alumina substrate on which the DC bias circuit is included using a multilayer technology. This is an interesting solution because the bias circuit is used to improve the stability of the active device especially in the low frequency range by implementing SMC resistors and capacitors.*

## INTRODUCTION

New millimeter-wave applications (Brière (1)) need the characterization and modelling of both active and passive devices. Accurate modelling of basic components and circuits is very important to achieve more complex and integrated function design. In the high frequency range, i.e. millimeter and submillimeter-wave, systems are fabricated using an MMIC technology (Sasaki et al (2)), quasi-optical techniques (Steup et al (3)) or even hybrid (MIC or MHMIC) technology for lower frequencies (Ka band).

The characterization of active devices is achieved with a Vector Network Analyzer (VNA) for S parameter measurements or with a specific setup such as a load-pull test bench (Bouysse et al (4)). An electrical equivalent circuit of the device can be extracted from S parameters over a wide frequency range (from some MHz up to millimeter frequency ranges) depending on the VNA capabilities. On a load-pull system, a large signal characterization can provide the load impedances of the active device for optimum output power or optimum power added efficiency. The behavior of the device depends on the operating conditions : input power, fundamental frequency, bias voltages as well as harmonic terminations.

For all these characterization techniques, the DC power supply of the active device is one important point. S parameter measurements can be achieved using VNA internal DC bias tees because these are usually very broadband tees. A coaxial technology is therefore used from the VNA output ports to the device test fixture. If internal DC bias tees are not available with the VNA configuration, these have to be implemented on the device test fixture and should be transparent under RF operation.

This paper presents the S parameter measurements of a chip transistor in the Ka band. The transistor is mounted and bonded on a coplanar printed alumina substrate on which the DC bias circuit is included using a multilayer technology. The coplanar test fixture is compatible with an RF probe station. The DC bias circuit design and measurements are also presented.

## DC BIAS CIRCUIT

The basic circuit for DC biasing at high frequencies is the well known structure shown in fig. 1. This structure can be used either with microstrip or coplanar technology. The lines are each  $\lambda_g/4$  long,  $\lambda_g$  is the guided wavelength, one having a low characteristic impedance, the other having a high one. With this configuration, any impedance can be connected at the midpoint (point A - see fig. 1) of the two lines without perturbations at point B, that is, a very high impedance is seen at this point according to the following equation:

$$Z_B = \frac{Z_{C1}^2}{Z_A}$$

where  $Z_{C1}$  is the characteristic impedance of the narrow width line and  $Z_A$  is the impedance at the point A (as shown in fig. 1). A DC bias voltage is then applied at the midpoint A using a bond wire without any perturbation on the RF operation.

However, a drawback of this technique is its small band frequency response because of the  $\lambda_g/4$  lines. It is only used in narrow band circuit design such as amplifiers with a 15 to 20% frequency bandwidth.

To achieve broadband operation of the DC bias circuit, a very high lumped impedance, here an inductance called "choke" inductance, has to be used. The ideal circuit is depicted in fig. 2-a. To improve the DC bias decoupling, a capacitor can also be added, in series with the inductance, providing a very low impedance (short-circuit) in the frequency range. This inductance is made with a bond wire whose length gives the inductance value. The capacitor is a Metal-Insulating-Metal (MIM) capacitor using a multilayer technology. Then a DC bias voltage can be applied at the midpoint of the two lumped elements. The implemented structure in our multilayer technology is given in fig. 2-b.

Circuits of figs. 1 and 2b were tested on a probe station from 45 MHz up to 20 GHz with a HP8510B VNA and in the Ka band (26.5-40 GHz) with an ABmm VNA (Goy and Gross (5)). The results are shown in fig. 3-a and 3-b. Both structures are well matched over a wide frequency range, that is, the DC bias circuit does not degrade the line matching. But, as one can see from fig. 3, a broader frequency range is achieved with the lumped circuit of fig. 2-b, the circuit showing few losses ( $S_{21}$  better than -0.5 dB) and being well-matched ( $S_{11}$  better than -20 dB from 20 GHz up to the end of the Ka band and beyond).

The measured and simulated data are compared for the distributed and lumped circuits and are in very good agreement as shown in fig. 3. The extraction of the inductance value was carried out in the 0.045-20GHz frequency range for the lumped circuit. The resonance frequency is about 2.5 GHz for both simulation and measurement. This leads to an inductance value of about 1.35 nH (according to the formula :  $F_r = 1 / 2\pi\sqrt{LC}$ ) with a 3 pF MIM capacitor computed with  $C = \epsilon_0\epsilon_r S/e$ , where S is the metal surface (1mm<sup>2</sup>), e the dielectric layer thickness (30  $\mu$ m) and  $\epsilon_r$  its relative permittivity (10). The 1.35 nH inductance value was obtained with a 2.45 mm semi-loop wire diameter. The inductance value is large enough because the impedance magnitude is greater than 220  $\Omega$  at 26 GHz. It was first evaluated using the formula (6) :

$$L(\mu\text{H}) = 0.01257 * a * \left[ 2.303 * \text{Ln}\left(16 \frac{a}{d}\right) - 1.936 \right] / 2$$

where a (in cm) is the loop radius, d (in cm) is the gold wire diameter. It leads to an approximate value of 1.8 nH.

With this DC bias circuit, a transistor test fixture was fabricated on a coplanar printed Alumina substrate and measurements were performed in the Ka band.

## TRANSISTOR S PARAMETER MEASUREMENTS

The transistor was mounted and bonded with a thermal compression technique (with 25  $\mu$ m gold wire) in the test fixture. A major problem when biasing an active device is its potential instability which can damage or destroy the component when not controlled. The potential instability often occurs at low frequencies because of the device's high gain. Then, the DC bias circuit can be used to improve low frequency stability by adding resistors (about 50  $\Omega$ ) which will not perturb the high frequency operation owing to the choke inductance and the MIM capacitor. These resistors can be SMC0805 components or a resistive layer. However, parasitic elements of the SMC components will degrade the behavior of the stabilization circuit for frequencies above 5 GHz, depending on the SMC size. A resistive layer should improve the stability of the active device over the whole frequency range. The designed test fixture is depicted in fig. 4.

The transistor is a PHEMT (Litton LP7612) and S parameters were measured with a probe station under different DC bias voltages in the Ka band with an ABmm VNA. The basic configuration of the VNA (see fig. 5) is modified by the user to ensure a small incident power on the transistor for small-signal parameter measurements and low power measurement is also required for the linearity of the detectors. As there is no internal DC bias tees, the previously described test fixture was used. Because of the Ka rectangular waveguide technology of the measurement setup (couplers, mixers, generators) and coaxial access of the RF probes, a

rectangular to coaxial transition is used so that no series decoupling capacitor is needed. The transition is a DC blocking and an open circuit at very low frequency.

After a TRL autocalibration, S parameter measurements were performed. To validate the measurement configuration and the test fixture, another transistor was measured at the same bias voltages using a classical VNA over the 0.1-40 GHz range. The internal bias tees of this VNA were used because the inductance value is not high enough to ensure proper decoupling at frequencies under 26 GHz. As there are no integrated DC bias tees, the transistor test fixture is simplified. The compared measurements are presented in fig. 6. The agreement is very good in the Ka band although the two measured transistors are different as well as the bonds of the chips.

The small signal equivalent circuit of fig. 7 was extracted from measured S parameters (10 to 26 GHz). S parameter measurements in the Ka band were compared with simulated S parameters showing very good agreement. Fig. 8 shows the comparison between measured and simulated S parameters in the 1-40 GHz frequency range. As a result, the equivalent circuit of fig. 7 can fit measured data in the full band with very good precision.

A one stage amplifier was designed using the DC bias tees. The simulated gain is about 5 dB at 30 GHz. The circuit fabrication is underway and measurements will be presented at the conference.

## CONCLUSION

Ka band S parameters of a PHEMT transistor have been presented. The transistor chip is mounted on a coplanar printed Alumina substrate. The test fixture including DC bias circuit is compatible with a probe-station which allows S parameter measurements up to 60 GHz, depending on active devices currently available in this high frequency range. An active load-pull setup for large signal characterization of active devices (GUNN diode and transistor) is under study in the Ka band using rectangular waveguide technology.

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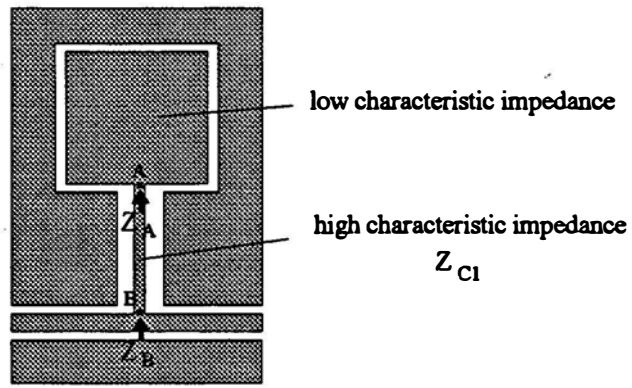


fig.1: DC bias circuit in coplanar technology

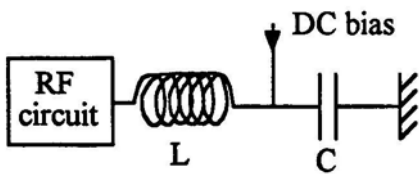


fig.2-a: ideal DC bias circuit ( $L\omega$  : very high impedance and  $1/C\omega$  short-circuit)

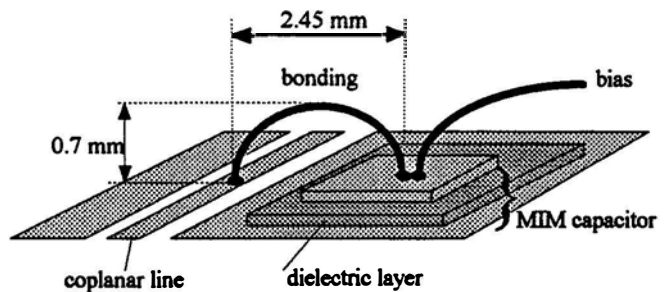


fig.2-b: DC bias circuit implemented in multilayer technology

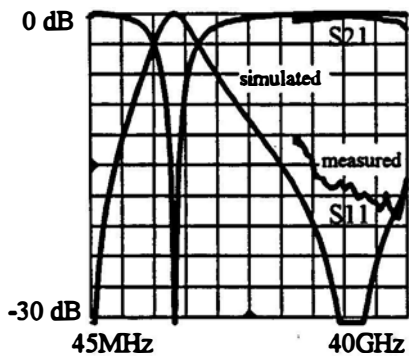


fig 3-a: measurement and modelling of the DC bias circuit of fig. 1

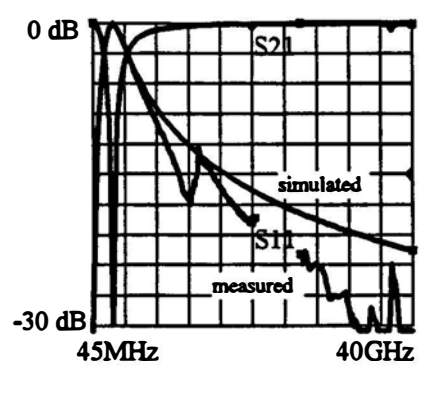


fig 3-b: measurement and modelling of the DC bias circuit of fig. 2-b

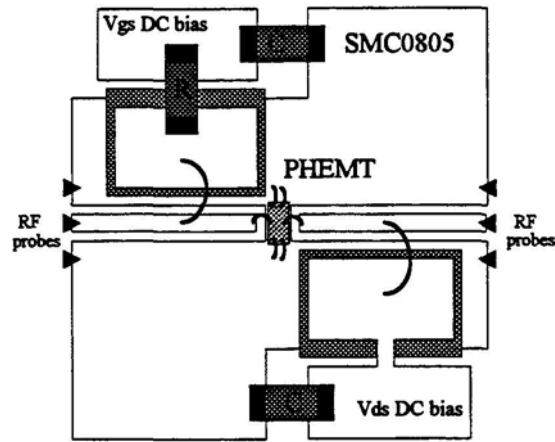


fig 4 : Ka band test fixture layout

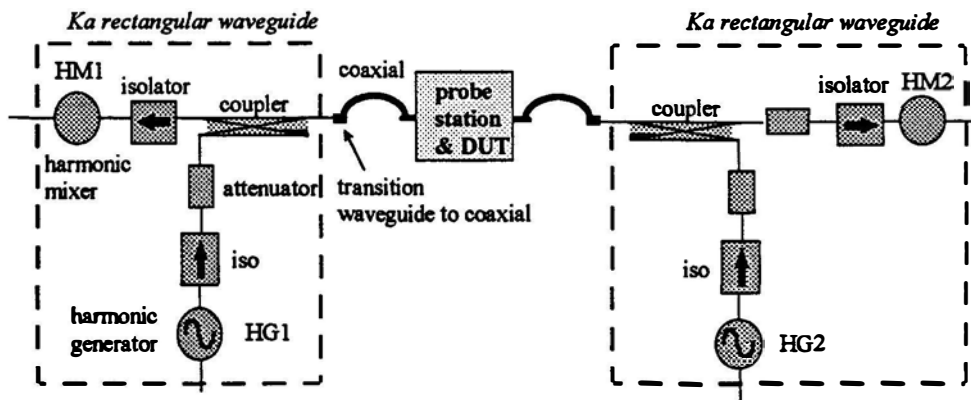


fig 5 : ABmm VNA configuration for small signal S parameter measurements

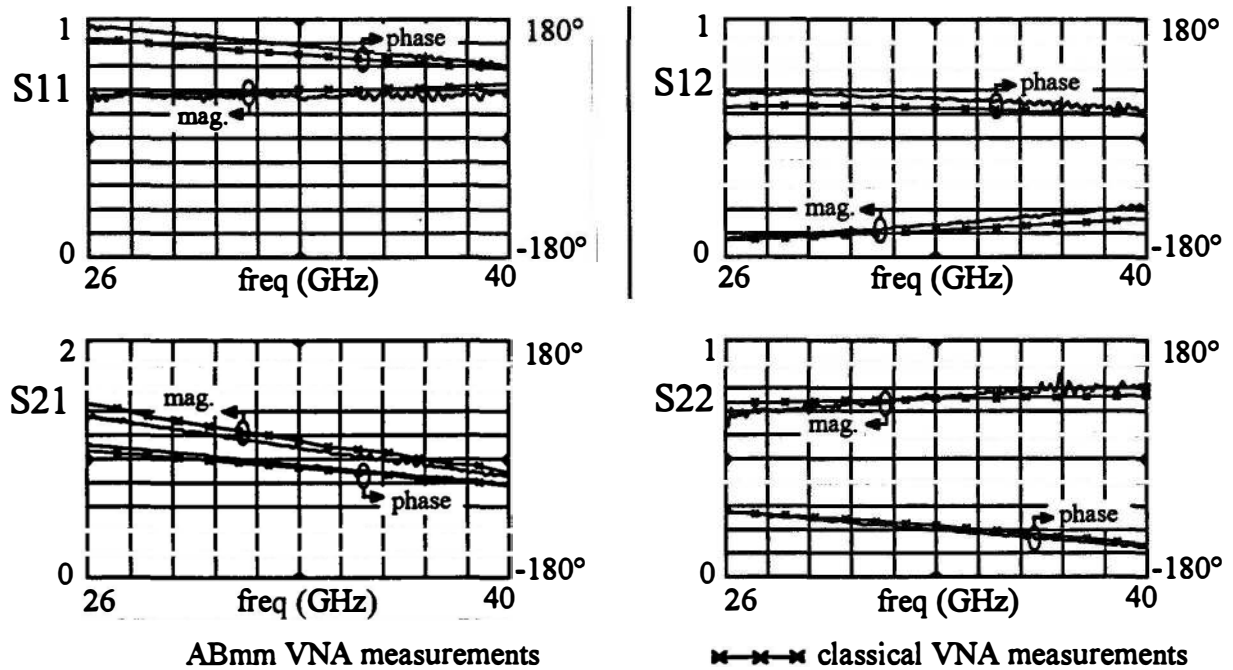
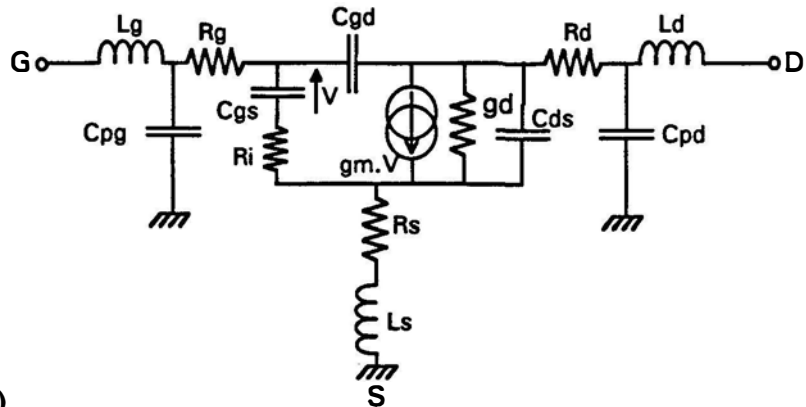


fig 6 : Comparison of the S parameter measurements performed with the two VNA (see text)



$$gm = gm_0 \exp(-j\omega\tau)$$

Cgs (pF)	Cgd (pF)	Cds (pF)	Cpg (pF)	Cpd (pF)	gm <sub>0</sub> (mS)	gd (mS)	τ (pS)	Ri (Ω)	Lg (pH)	Ld (pH)	Ls (pH)	Rg (Ω)	Rd (Ω)	Rs (Ω)
0.400	0.011	0.022	0.100	0.046	99.21	1.47	2.2	0.100	178	62.3	61.31	3.66	4.0	5.7

fig 7 : small signal equivalent circuit of the PHEMT transistor

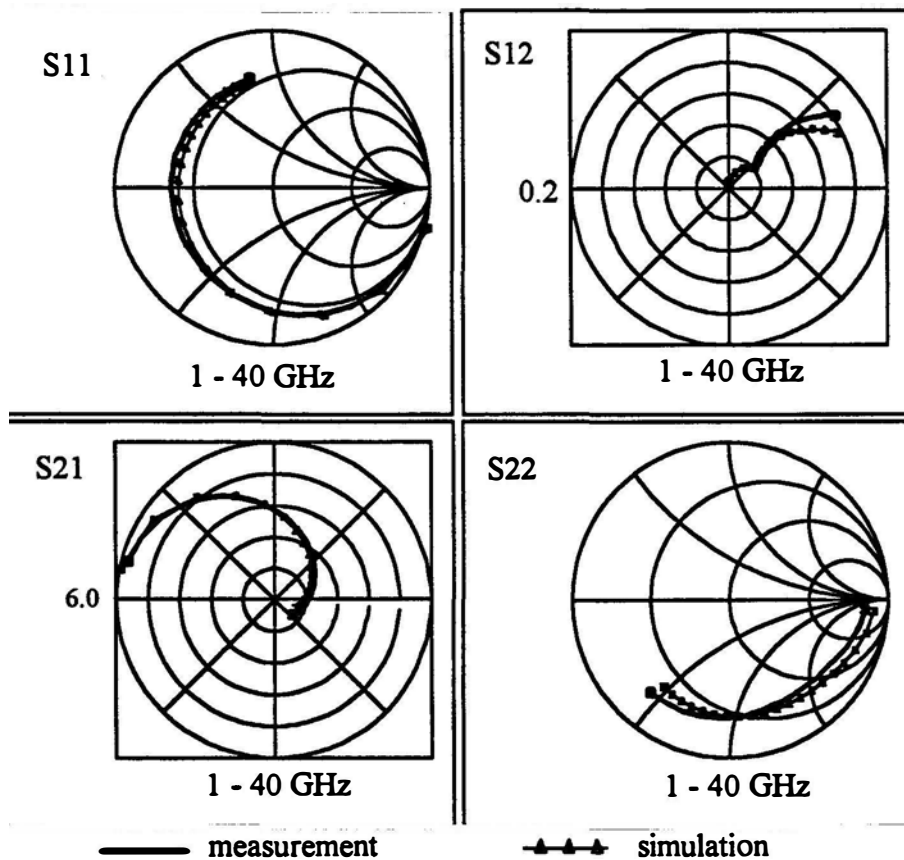


fig 8 : Comparison of the simulated and measured S parameters of a PHEMT transistor biased at 5V, 34 mA