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# Study of the Breakdown Voltage of Protected or Non-Protected 6H-SiC Bipolar Diodes by OBIC Characterisation

K. Isoird, L. Ottaviani, M.L. Locatelli, D. Planson, C. Raynaud, P. Bevilacqua and J.P. Chante

CEGELY (UPRES-A CNRS n°5005), Bat. 401, INSA de Lyon, 20 avenue A. Einstein, FR-69621 Villeurbanne, Cedex, France

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**ABSTRACT** The OBIC (Optical Beam Induced Current) method and its application to study SiC implanted diodes protected or not by JTE are presented in this paper. These measurements associated to the simulation results illustrate the effects of the periphery emitter doping profile on the electric field distribution and give information concerning the operation of the Boron implanted JTE on the breakdown voltage.

# 1. INTRODUCTION

Silicon carbide presents electrical properties suitable for many applications especially for high power devices. In addition to the semiconductor's high critical electric field, the breakdown voltage depends on the protection used for the junction termination. The JTE (Junction Termination Extension) technique is a potentially efficient protection to prevent premature breakdown for high voltage SiC devices. The OBIC (Optical Beam Induced Current) technique is a powerful method to investigate the electric field distribution in periphery of high voltage planar diodes and to study the operation of the junction termination [1]-[3]. This work presents electrical and OBIC characterisation results obtained from experimental 6H-SiC bipolar diodes protected or not by Boron implanted JTE and compared to the simulation results with ISE simulation software.

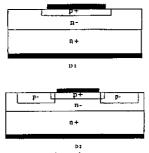
# 2. EXPERIMENTS

# 2.1 Device structures

The p<sup>+</sup>nn<sup>+</sup> diodes are realised on a n<sup>+</sup>-type 6H-SiC substrate doped at  $3\times10^{18}$  cm<sup>-3</sup>. Five successive implantations of Aluminum at 300 °C (at energies ranging from 25 keV up to 300 keV) into the n-type epilayer (thickness = 10 µm, doping level =  $3\times10^{15}$  cm<sup>-3</sup> confirmed by C-V measurement) create the emitter (depth =  $0.5 \, \mu m$ , target-doping level =  $4\times10^{19}$  cm<sup>-3</sup>). JTE (depth =  $0.7 \, \mu m$ , target-doping level =  $2\times10^{17}$  cm<sup>-3</sup>) is realised by 11 Boron implantations realised at 300°C. The samples were annealed at 1700 °C during 30 minutes [4], and metallized for anode and cathode ohmic contacting at the end. No passivation layer covers the semiconductor surface. We have tested two types of diodes: D1 diodes without JTE, D2 diodes protected by JTE (Fig.1). OBIC and electrical characterisations have been performed on these devices.

# 2.2 OBIC Setup and method

Fig. 2 shows the experimental setup that we use to perform OBIC measurements. An Ar<sup>++</sup> laser produces an UV beam at different wavelengths (from 363.8 nm to 300 nm) which is focused on the sample and modulated at 70 Hz by a chopper. A lock-in amplifier detects the local variation of the photocurrent induced by the 3.3 µm incident light spot on the reverse biased device. A computer controls 2 stepper motors to ensure the horizontal moving of the device under test and records current measurements as a function of the light spot position.





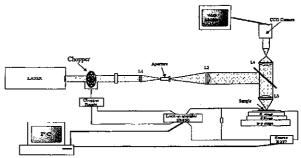


Fig. 2: OBIC setup.

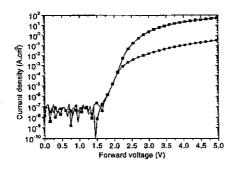
# 3. RESULTS AND DISCUSSION

# 3.1 I-V characteristics and breakdown voltage

Breakdown voltage measurements were made in 2 different ambients (air and silicone oil) at room temperature. Though a quite wide range of breakdown values (Tab. 1) is obtained, we can first note the influence of the ambient nature. Breakdown voltages are slightly better in the higher dielectric strength ambient (oil). That indicates that the breakdown takes place in the ambient, confirmed by the arc occurrences observed between the edge of the ptn junction SCR and the anode contacting probe (well visible during tests in oil). Moreover, contrary to air-testing, the results in the oil indicate a JTE presence effect, allowing the observation of Vbr values up to 1700 V for D2 protected devices (Theoretical breakdown value = 1640 V). Besides, all experimental breakdown voltages for D1 diodes are higher than the expected value (360 V) obtained by simulation, taking into account a box profile shape of p+ emitter and the ionisation coefficients given by Konstantinov et al. [5]. Moreover we observe that the highest voltage sustaining structures often exhibit elevated voltage drop under high forward current. Fig. 3 presents 2 typical kinds of forward characteristics at room temperature. The different reverse characteristics present the same non linear behaviour, with typically  $J_r = 1 \times 10^{-6} \text{ A/cm}^2$  at  $V_r = -600 \text{ V}$  at 300 K. Among the possible explanations of such inhomogeneous results is the p+ doping profile, as confirmed by the different Al impurity profiles over the wafer obtained from SIMS measurements (Fig. 4). The different Al profiles are due to the surface etching during post-implantation annealing. The use of OBIC measurements is aimed at completing the analysis by studying the influence of the emitter doping profile and the surface charges on the electric field distribution at the device periphery.

Ambient	Air	Oil
Breakdown voltage for D1	400 V - 1100 V	700 V – 1200 V
Breakdown voltage for D2	600 V – 1100 V	600 V – 1700 V

Tab.1: Values of breakdown voltage in different ambients.



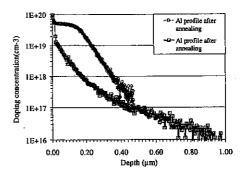


Fig. 3: Two typical forward characteristics at 300 K

Fig. 4: Two different SIMS Al profiles at different places on the wafer

#### 3.2 OBIC Measurements

Fig. 5 shows the OBIC signals simulated and measured on 2 non protected D1 samples along one half diameter line at  $\lambda$  =333.6 nm or  $\lambda$  =351.1 nm, corresponding respectively to light penetration lengths of 5  $\mu$ m and 10  $\mu$ m in 6H-SiC, with a spot diameter of 3.3  $\mu$ m and an optic power density of 1 W/cm<sup>2</sup>. For simulation, the p<sup>+</sup> emitter profile has a constant doping level of  $4\times10^{19}$  cm<sup>-3</sup> up to 0.35  $\mu$ m depth; and we neglected any surface charge density.

Fig. 5a shows D1 experimental results exhibiting the same behaviour as the simulated ones presented on Fig. 5b. A constant photocurrent is induced when the UV spot scans the emitter region, non-covered by the anode metal. This current increases with the voltage due to the space charge region (SCR) spreading. Moving towards the structure periphery an OBIC peak occurs at the edge of the p<sup>+</sup>n junction SCR, which grows with increasing voltage. This peak is caused by the local carrier multiplication (essentially holes multiplication) produced by the high electric field at the p<sup>+</sup>n junction. Outside the SCR, the current decreases exponentially due to photogenerated hole diffusion ( $L_p = 4 \mu m$  for the simulation and 9  $\mu m$  for the measurements). The laterally non abrupt Al concentration profile, the  $L_p$  value, and the spot diameter uncertainty, can explain the wider experimental OBIC signals compared to the simulated ones. The fact that we do not detect any OBIC signal far outside the diode at low voltage, indicates no significant presence of surface charges. So the higher experimental breakdown values for D1 (compared with the simulation) may not be explained by the effect of surface charges.

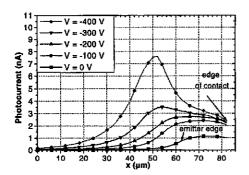


Fig. 5a: OBIC signal on D1 at  $\lambda = 333.6 \text{ nm}$ 

Fig. 5c shows a second type of experimental behaviour. In that case, the photocurrent increases with applied voltage and saturates when the epilayer is totally (depleted width =  $10~\mu m$  depleted at  $V_r = 280~V$ ). But no peak arises at the periphery. This result means that the electric field distribution at the junction periphery is different. That can be explained by the periphery emitter doping profile. In fact for experimental acceptor doping profiles as presented on Fig. 4, the simulation results show that lower electric fields are obtained for a given reverse bias as compared with the theoretical Al profile case.

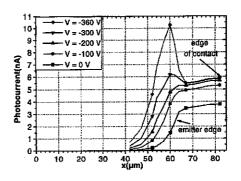


Fig. 5b: OBIC simulation at  $\lambda = 333.6 \text{ nm}$ 

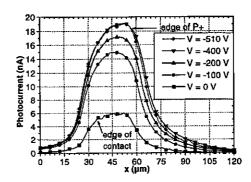
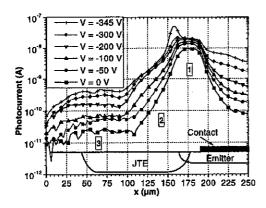


Fig. 5c: OBIC signal on D1 at  $\lambda = 351.1$  nm

We expose the OBIC measurements obtained from JTE D2 diodes on Fig. 6, using semi-logarithmic scales. Fig. 6 allows to observe 3 distinct zones in the OBIC signal obtained at the periphery of the anode contact. First we recognise the OBIC signal due to the  $p^+$  region, as for D1 diodes. Then the photocurrent decreases versus the distance from the emitter region edge. At this position, OBIC signal is due to the extension of SCR on both sides of the JTE pn junction. The presence of a peak at the emitter edge reveals a total depletion of the JTE near  $p^+$  region. The third zone on Fig.6 corresponds to the external side of JTE. For the reported reverse biases, the SCR extension in the n-type epilayer remains weak, leading to small current. Such a behaviour requires a low doped JTE region. Fig.7 shows the simulated equipotential line repartition in a structure assuming a  $1\times10^{16}$  cm<sup>-3</sup> doped JTE with a 1.4  $\mu$ m deep gradual junction, in agreement with the effective Boron profiles checked by SIMS analysis. Such a too low doping level of the JTE protection allows to explain the weak difference in breakdown voltages between D1 and D2 diodes.



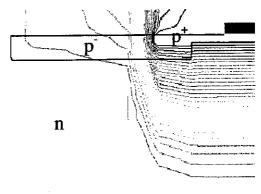


Fig. 6: D2 OBIC measurement at  $\lambda = 351.1$  nm with Popt = 1.5 W /cm<sup>2</sup>(semi-logarithmic scale)

Fig. 7: ISE simulation of equipotential repartition for a diode with JTE at reverse bias voltage of 450 V

## 4. CONCLUSION

This paper shows that the OBIC measurements performed on our planar 6H-SiC bipolar diodes, combined with the electrical characterisations and the simulations, allow to analyse the device behaviour under reverse biases. The examination of both experimental and simulated OBIC signal versus the position of the localised photogeneration zone can give information concerning the place of the breakdown region, the effect of the junction doping profiles (emitter or JTE) and the presence of surface charges. From the presented results, the effective operation of the Boron doped JTE protection and the reasons for its poor efficiency could be evidenced.

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