Optimization of a DC/DC dual active bridge converter for aircraft application

Maximin Blanc, Yves Lembeye, Jean-Paul Ferrieux, Corentin Rizet, Arnaud Mahe, Taoufik Bensalah

Optimization of a DC/DC dual active bridge converter for aircraft application

Maximin Blanc[a,b], Yves Lembeye[a], Jean-Paul Ferrieux[a], Corentin Rizet[c], Arnaud Mahe[b] and Taoufik Bensalah[b]

[a]Univ. Grenoble Alpes, Grenoble, France; [b]THALES AES, Chatou, France; [c]SIREPE, Montailleur, France

ABSTRACT

Avionics is intended to become more and more efficient in terms of energy saving thanks to increased efficiency of embedded system. Today, electricity is presented as the best energy vector compared to hydraulic or pneumatic. This is why current researches aim to focus on power electronic converters in order to meet the future electrical power demand in aircraft networks. In this article, the authors investigate a DC/DC dual active bridge converter which is expected as the best candidate to meet the complex requirements of an aircraft environment, especially the high-voltage dynamics. This persuaded the researchers to study the structure and modulations which are explained and brought face to face with a low-power prototype in order to validate the theoretical assumptions. The next step, is a 3.75 kW demonstrator specification with high integration (2 kW/kg). Semiconductor, magnetics and thermal management selection are presented to reach the specifications. Special care has been provided in an original capacitance calculation method and thermal considerations for heatsink choice. The originality of this work is to build active conversion system to prove it suits to aircraft specifications (high voltage dynamics, overload).

KEYWORDS

Power electronics; more electrical aircraft; dual active bridge; reversible DC/DC converter; ZVS modulation

1. Introduction and basics of dual active bridge

The main constraints in avionics system are the weight, size, standards and efficiency. Related to this, the electrical conversion must provide reversibility, galvanic insulation, and high efficiency. Previous work has highlighted the dual active bridge (DAB) as the best choice to meet our specifications [1–3]. Composed of two full bridges, an AC inductor and a high-frequency (HF) transformer, completed with capacitor filter, the reduction of stored energy is expected to minimize size and cost of the system [3]. Presented first in 1991, recent work has been done on DAB converters to present a different way to control the structure but above all to highly increase efficiency when the input and output voltages do not match well [4–12] .

The converter has to be efficient when input and output voltage is operating under high dynamics. The HVDC side is in the range [500 V and 650 V] and the LVDC voltage has to be regulated between [26 V and 32 V] for a nominal power of 3.73 kW. The converter is able to accept an overload of 50% lasting 10 s. The basic operation principle is as follows. Each full bridge inverts DC voltage and creates a voltage drop across the AC inductor which leads to a current variation. This shape can be controlled thanks to phase shifting between legs (duty cycles D_1 and D_2 adjustment) and bridges (commonly named Phase-Shift φ). The switching frequency is another free parameter but here it is assumed to be set constant at 100 kHz. The link between the two full bridges is inductive and can be seen as a current source filtered with capacitor. The simplified representation of DAB converter is as follow.

2. Modulation of dual active bridge

In literature [5–12], researchers have shown the different modulations which are able to control the DAB. Among them there is three classical forms named phase-shift, triangle and trapezoidal modulations. By adjusting duty cycles and phase-shifting, the shape of the current is drawn in order to meet some objectives: ZVS, ZCS... Exhaustive and detailed overview of every control possibility of DAB cannot be performed in few paragraphs. This is why the authors highly recommend to refers to literature references presented before for their high quality and detailed analysis.

2.1. *Classical modulations: triangle, trapezium and phase-shift*

Thanks to adjustment of D_1, D_2, and φ, the transferred power is controlled from one bridge to the other. The easiest modulation is the so-called phase-shift because the duty cycle of each bridge is set to

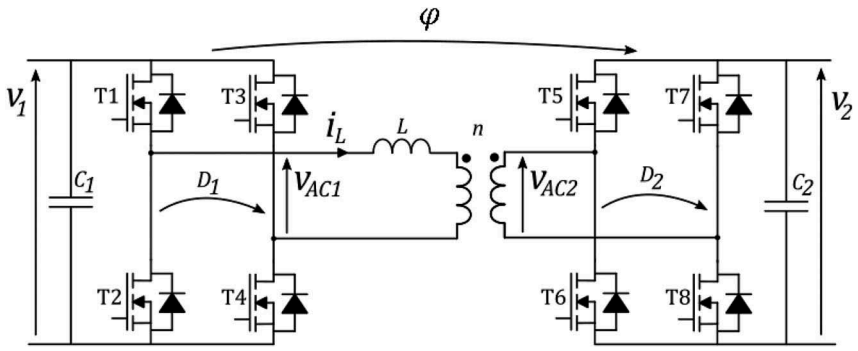


Figure 1. Dual active bridge basic structure.

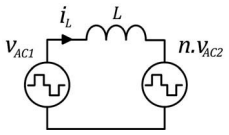


Figure 2. Simplified representation of DAB.

maximum and φ is the only parameter used to vary the power. Triangle modulation acts like a diode rectifier when D_1, D_2, and φ are carefully selected to switch the secondary side at zero current. Eventually the trapezoidal modulation allows the controller to extend the triangle modulation to a higher power level. Figure 1-3 illustrates schematics and waveforms of DAB structure for those three controls.

Equations for all are well known but the study can go further by letting the parameters D_1, D_2 and φ change freely. This leads to 12 modulations in which those examples are a particular case. The first step was the selection of the best candidates with an energetic approach.

2.2. *1st harmonic approach*

A first harmonic study has been performed and has demonstrated in Figure 4 that we shall always keep the phase-shift below $\pi/2$. An increase of the phase-shift results in an increase of RMS current and reactive power transmission which must be avoided.

Equation can be deducted in complex domain with:

$$P = \mathrm{Re}\left(\overline{V_{1,\sim}}.\overline{I_{L,\sim}}^{*}\right) = \frac{\left|\overline{V_{1,\sim}}\right|\left|\overline{V_{2,\sim}}\right|\sin(\varphi)}{L\omega} \quad (1)$$

$$Q = \mathrm{Im}\left(\overline{V_{1,\sim}}.\overline{I_{L,\sim}}^{*}\right) = \frac{\left|\overline{V_{1,\sim}}\right| - \left|\overline{V_{1,\sim}}\right|\left|\overline{V_{2,\sim}}\right|\cos(\varphi)}{L\omega} \quad (2)$$

$$\left|\overline{I_{L,\sim}}\right| = \frac{\left|\overline{V_{1,\sim}}\right| + \left|\overline{V_{2,\sim}}\right| - 2\cos(\varphi)\left|\overline{V_{1,\sim}}\right|\left|\overline{V_{2,\sim}}\right|}{(L\omega)} \quad (3)$$

With, $\overline{V_{1,\sim}} = \frac{4V_1}{\pi\sqrt{2}}\sin(\pi D_1)$ $\overline{V_{2,\sim}} = \frac{4nV_2}{\pi\sqrt{2}}\sin(\pi D_2)e^{-j\varphi}$ $\overline{I_{L,\sim}} = \frac{\overline{V_{1,\sim}} - \overline{V_{2,\sim}}}{jL\omega}$ which denote the RMS value of the fundamental of square AC voltage $v_{AC1}(t)$, $n.v_{AC2}(t)$ and trapezoidal current $i_L(t)$ referenced on HVDC side

It has been demonstrated that the maximum error in phase-shift modulation between this approach and the real signal is smaller than 20% and the addition of the third harmonic reduces this error below 10%. Figure 5 shows the results. The power is derived as follow considering the k first harmonics.

$$P_{1..k} = \sum_{n=1}^{k} \frac{1}{n^3}\frac{\left|\overline{V_{1,\sim}}\right|\left|\overline{V_{2,\sim}}\right|\sin(n\varphi)}{L\omega} \quad (4)$$

According to this study, we consider the fundamental approach to be representative enough of DAB electrical behaviour. It is now relevant to look for the best set of parameters for each operating point. With the high-speed high-efficiency calculator available on the market, it becomes possible to imagine a real-time change of control strategy. For instance, a change from triangle to phase-shift modulation during operation.

2.3. *Minimization of RMS current*

Eventually, thanks to the energetic approach, the analytic work is reduced from 12 to 6 modulations. Based on these six remaining modulations, the choice is to study,

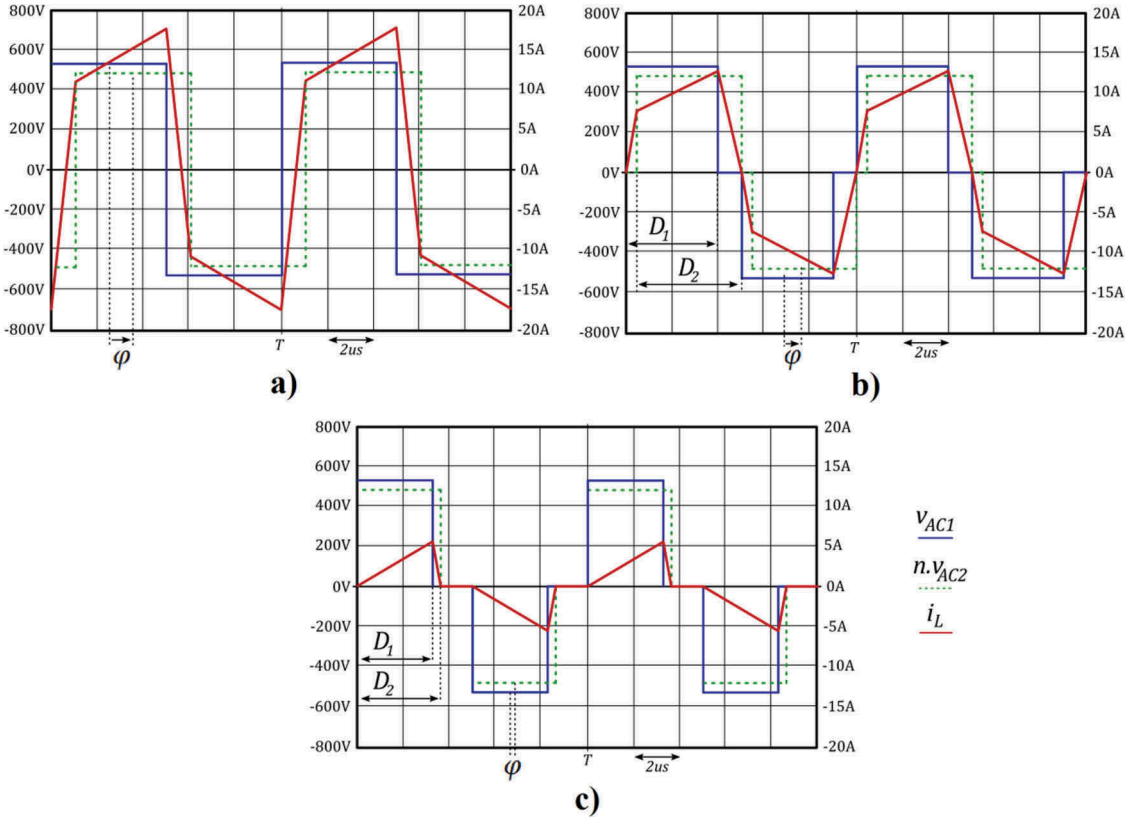


Figure 3. (a) Phase-Shift $D_1 = D_2 = 0.5$, $\varphi = 47°$. (b) Trapezium $D_1 = 0.4$, $D_2 = 0.44$, $\varphi = 28°$. (c) Triangle $D_1 = 0.31$, $D_2 = 0.38$, $\varphi = 11°$.

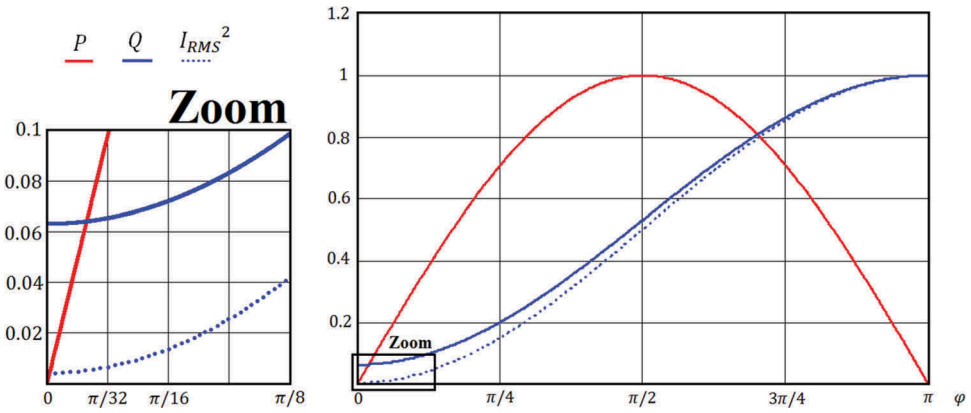


Figure 4. Active power fundamental (red), reactive power (blue) and square RMS current of L (dotted line) with respect to phase-shift. Values normalized to their maximum.

for all operating points, the evolution of RMS current of the AC current flowing on HVDC side in order to choose the modulation which minimizes this current. This will obviously reduce conduction losses and reactive power because the circulating current is lower. Figure 6 shows the different values of RMS current (fine line) and modulation area boundaries (thick line) for four different power levels. The input and output voltages are set to constant value and the RMS current is studied, with respect to D_1 and D_2 for each power level. The four modulations area named 1–4 can be completed with two others which are not shown here because they concern power transfer in opposite direction. Thanks to a MathCAD® programmed tool, the minimum RMS current is followed point by point with power increment. It is understood that an increase of power leads to a necessary increase of duty cycle because the power can only be transfer when the bridge

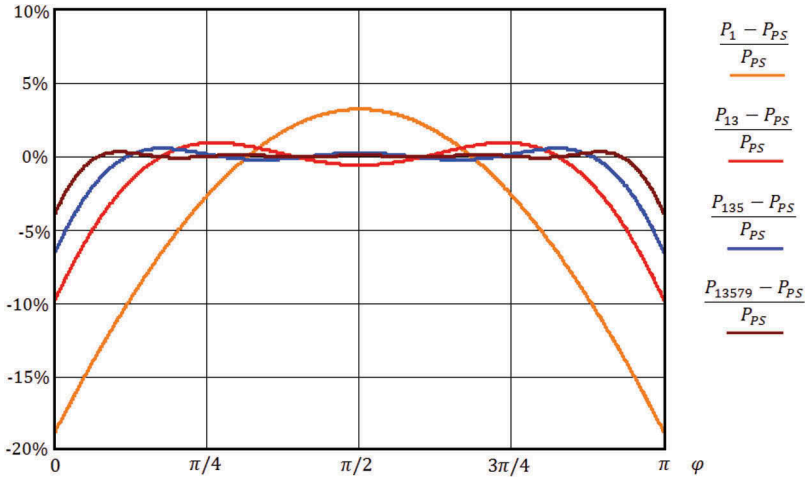


Figure 5. Error between the real signal and the harmonic method taking into account the fundamental (orange) and the consecutive harmonics up to ninth harmonic.

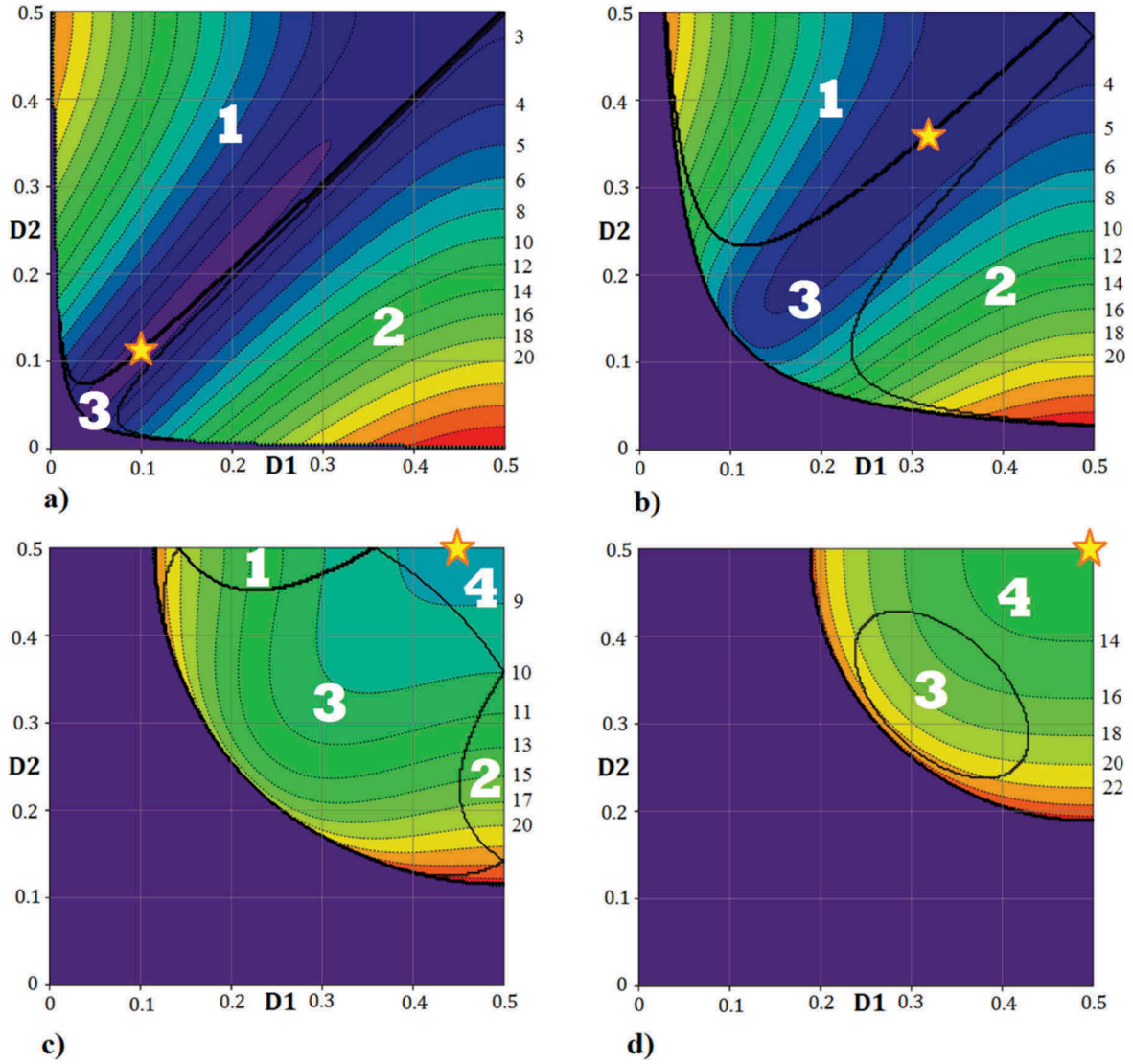


Figure 6. RMS current value (scale on right side in front of each line) and minimum current represented with a star. $V_1 = 540\text{V}$ $V_2 = 28\text{V}$ $n = 17$ $L = 35\mu H$.

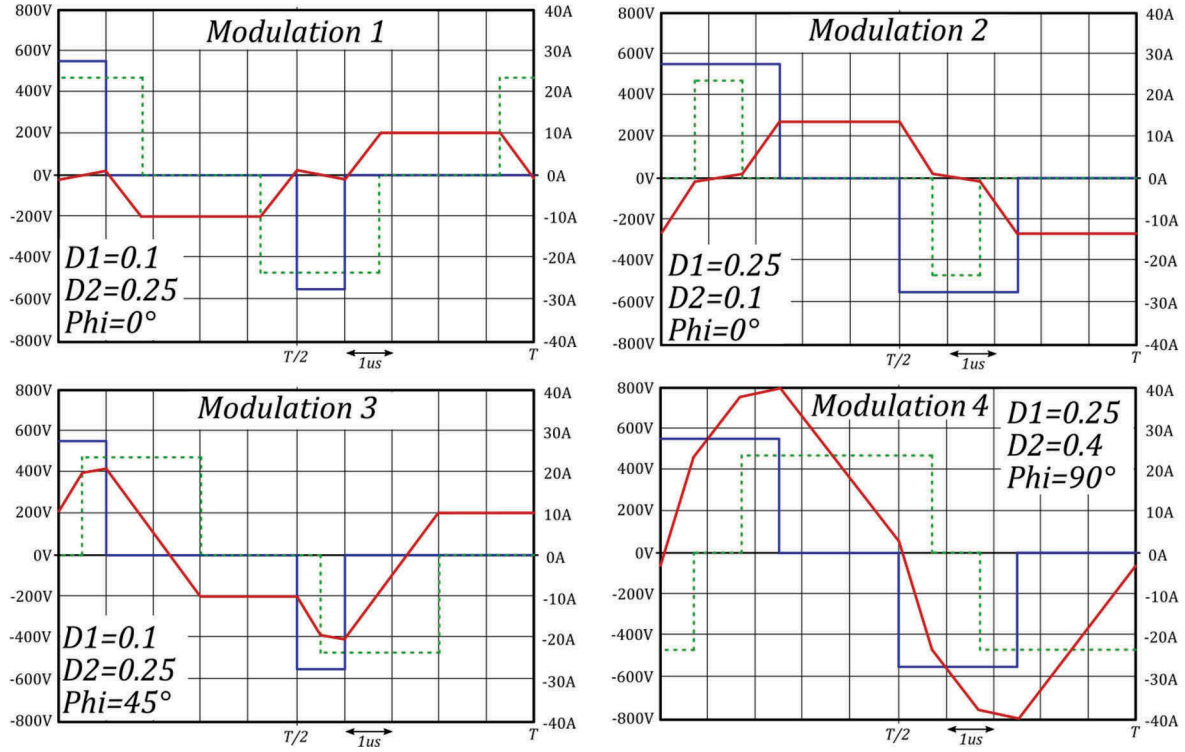


Figure 7. Example of modulations 1–4 presented in Figure 6, $v_{AC1}(t)$ in blue, $n.v_{AC2}(t)$ in green, $i_L(t)$ in red.

is connected to the grid (not during freewheeling period). The purple part is so a forbidden area. The aim is to find the best operating point in all the other available areas which is intended to meet a minimum RMS current in the AC network.

Table 1 gives the optimal parameters which minimize the RMS current and its value I_{RMS} compared to the value for phase-shift modulation I_{RMS-PS} to show the expected gain especially at low power. It looks like $D_1 = D_2 = 0.5$ seems to be a good combination to use regarding the increased of control complexity with variation of duty cycle. However, in some cases it would lead to the loss of ZVS condition for one of both bridge. It is particularly dramatic for 1200 V SiC MOSFETs. Studies can be found in thesis [12] (p. 94) which shows the effect of hard switching of 1200 V SiC compare to 100 V Si MOSFET. The conclusion of those experimental tests is an increase by a ratio of 2 for 100 V Si component when a 1200 V SiC component sees its losses increased by a factor more than 10.

It has been verified that, in low-power operation, the minimum of RMS current follows the boundary between modulations 1 and 2 (Figure 6(a,b)). This specific line is the so-called triangle modulation. At some point, one duty cycle reaches its maximum value (Figure 6(c)) and this is named M modulation (a special case one of the 4th studied modulation). In high power, both D_1 and D_2 meet 0.5. This is the phase-shift modulation, another special case of the fourth modulation. Table 2 and Figure 7 sums up the presented modulations with respect to their advantage and drawbacks. The conclusion leads to the strategy represented in Figure 8.

Table 1. Parameters for the minimum RMS current.

Figure 6.	(a)	(b)	(c)	(d)
Power in W	100	1000	3750	5625
D_1	0.101	0.318	0.454	0.491
D_2	0.114	0.361	0.5	0.5
φ in rad	0.043	0.134	0.371	0.594
I_{RMS} (I_{RMS-PS}) in A	0.51 (2.65)	2.86 (3.32)	8.44 (8.46)	13.08 (13.08)

For the point $(V_1, V_2) = (650\text{V}, 28\text{V})$, Figure 8 shows the optimal evolution of the three parameters used to control the power. This strategy, proposed in [5] and validated with MathCAD® leads to the concatenation of three modulations: triangle (low power), phase-shift (high power) and one between them which guarantees continuity of parameters. It is important to note the non-discontinuity required for system stability. The convention is as follows:

$$D_1 \in [0;0.5]\ D_2 \in [0;0.5]\ \varphi \in \left[-\frac{\pi}{2};\frac{\pi}{2}\right] \qquad (5)$$

In addition, care shall be taken when viewing this graph because the boundaries depend on V_1 and V_2 values. For all equations presented next, φ is the phase angle between voltage fundamentals. Taking this reference, the power transfer direction has the sign of φ. It is interested to notice the symmetry of DAB which means the two bridges act similarly. In Figure 8, $V_1 > n.V_2$ but if $V_1 < n.V_2$ there is a switch position between D_1 and D_2. When considering a reverse direction of power flow, the 5th and 6th studied modulation can be observed. Equations for the final strategy are derived in the next paragraphs to meet all operating points.

Table 2. Modulations comparison with respect to advantages and drawbacks.

Mod. name	Advantage	Drawbacks	Others characteristics
Phase-shift	Easy control Maximal power	Loss of ZVS High RMS current when V1 does not match n.V2	1 degree of freedom
Triangle	ZVS	Limited power when V1 is closed to n.V2	2 degrees of freedom Special case of Mod.1 and 2
Trapezium	ZVS	Reduced power compared to phase-shift	2 degrees of freedom
1	Reduced RMS current compared to phase-shift	Loss of ZVS depending on parameters values Limited power	2 degrees of freedom
2			2 degrees of freedom
3			2 degrees of freedom
4			2 degrees of freedom
M	Power close to maximum ZVS	Maximal power Complexe control	2 degrees of freedom Special case of Mod.4 when $D_2 = 0.5$

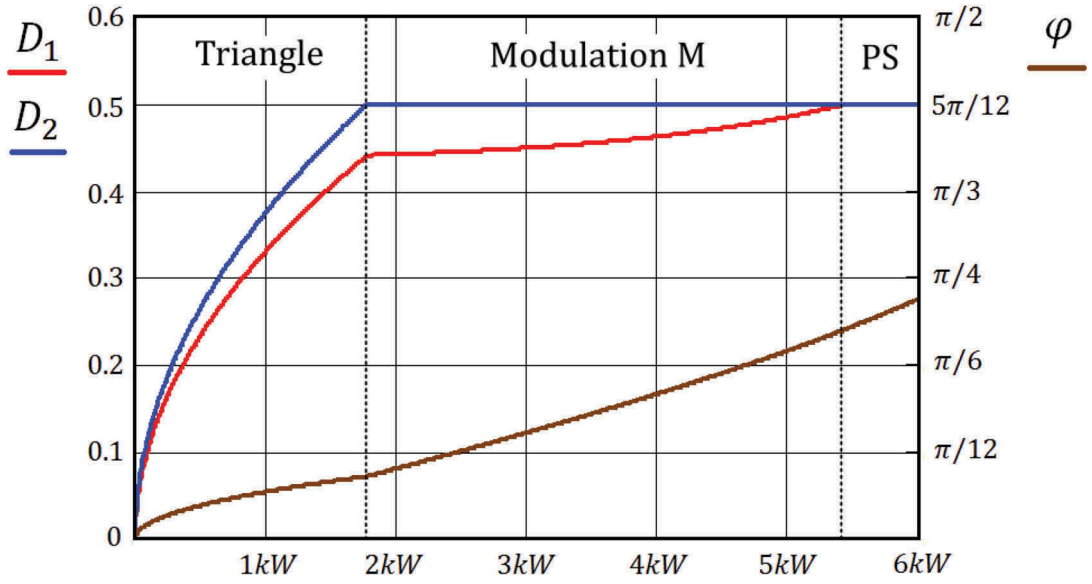


Figure 8. Proposed strategy in function of transferred power.

2.4. *Low-power, triangle modulation*

There are many reasons which can explain why, in low power, triangle modulation is the one which minimizes RMS current. First, a full bridge only transfers power when it acts in active mode. Secondly, the reduction of circulating currents is identical to always running an instantaneous positive power ($v_{AC1}(t).i_L(t)>0$ and $v_{AC2}(t).n.i_L(t)>0$). In those conditions an analytical analysis can determine a direct relationship between control parameters and circuit variables [5]

Case 1: $V_1 > n.V_2$

$$\varphi = \pi.\mathrm{sign}(P)\sqrt{fL|P|\frac{V_1 - nV_2}{V_1(nV_2)}} \tag{6}$$

$$D_1 = \frac{nV_2}{V_1 - nV_2}\frac{|\varphi|}{\pi} \tag{7}$$

$$D_2 = \frac{V_1}{V_1 - nV_2}\frac{|\varphi|}{\pi} \tag{8}$$

$$P_{\Delta 1,\max} = \frac{(V_1 - nV_2)(nV_2)^2}{4fLV_1} \tag{9}$$

$$I_{\mathrm{RMS}} = \frac{\sqrt{6}}{3Lf}\sqrt{{D_1}^3 nV_1V_2 - 2{D_1}^3{V_1}^2 + 3{D_1}^2D_2{V_1}^2 - 3D_1{D_2}^2nV_1V_2 + {D_2}^3nV_2} \tag{10}$$

Case 2: $V_1 < n.V_2$

$$\varphi = \pi.\mathrm{sign}(P)\sqrt{fL|P|\frac{nV_2 - V_1}{nV_2{V_1}^2}} \tag{11}$$

$$D_1 = \frac{nV_2}{nV_2 - V_1}\frac{|\varphi|}{\pi} \tag{12}$$

$$D_2 = \frac{V_1}{nV_2 - V_1}\frac{|\varphi|}{\pi} \tag{13}$$

$$P_{\Delta 2,\max} = \frac{(nV_2 - V_1)V_1}{4fLnV_2} \tag{14}$$

$$I_{\mathrm{RMS}} = \frac{\sqrt{6}}{3Lf}\sqrt{{D_1}^3{V_1}^2 - 3D_1{D_2}^2nV_1V_2 + {D_2}^3nV_1V_2 + {D_2}^3nV_2} \tag{15}$$

Algorithm recommends following this modulation up to its maximum value $P_{\Delta,\max}$ which is when one of the two duty cycle reaches its maximum value.

2.5. Medium power, modulation M

In a first assumption, the trapezoidal (which avoids circulating current) could be seen as a good continuity of triangle modulation. However, the strategy suggests to use something different which is called M1 when $V_1 > n.V_2$ (respectively M2 if $V_1 < n.V_2$). For both the equation of Phase-Shift is:

$$\varphi = \pi.\mathrm{sign}(P) \cdot\left(\frac{1}{2} - \sqrt{D_1(1 - D_1) + D_2(1 - D_2) - \frac{1}{4} - \frac{2f_{\mathrm{dec}}L|P|}{nV_1V_2}}\right) \tag{16}$$

To create a formula for D_1 and D_2 the next system must be solved and this is far from easy and requires mathematical software.

If

$$V_1 \geq nV_2 \;\; \frac{d\left(I_L|_{D_2=0.5}\right)}{dD_1} = 0 \leftrightarrow \begin{cases} D_1 = D_{1\mathrm{opt}} \\ D_2 = 0.5 \end{cases} \tag{17}$$

If

$$V_1 \leq nV_2 \;\; \frac{d\left(I_L|_{D_1=0.5}\right)}{dD_2} = 0 \leftrightarrow \begin{cases} D_1 = 0.5 \\ D_2 = D_{2\mathrm{opt}} \end{cases} \tag{18}$$

The detailed formulas for $D_{1\mathrm{opt}}$ and $D_{2\mathrm{opt}}$ are available in literature [2,5].

Finally, here is the expression for RMS current.

2.6. High power, phase-shift modulation

After a certain amount of power, the previous system resolution returns impossible value for duty cycle (e.g. above 0.5). In this instance D_1 and D_2 are set to the maximum (0.5) and this is actually the phase-shift modulation

$$\varphi = \frac{\pi}{2}.\mathrm{sign}(P)\left(1 - \sqrt{1 - \frac{8fL|P|}{nV_1V_2}}\right) \tag{20}$$

$$D_1 = 0.5 \tag{21}$$

$$D_2 = 0.5 \tag{22}$$

$$P_{\max} = \frac{nV_1V_2}{8Lf} \tag{23}$$

$$I_{\mathrm{RMS}} = \frac{\sqrt{3\left({V_1}^2 - 64nV_1V_2\left(\frac{|\varphi|}{2\pi}\right)^3 + 48nV_1V_2\left(\frac{\varphi}{2\pi}\right)^2 - 2nV_1V_2 + (nV_2)^2\right)}}{12Lf} \tag{24}$$

The converter is like a current source with an internal physical limitation (value of inductance). And so, it can work up to its maximum power $P_{\max}$.

2.7. Low-power prototype results

A low power prototype has been built (Figure 9) to validate the theoretical equations for control. It is a 300 W DAB converter with a variable input and output voltage up to 50 V and maximum current around 10 A. The switching frequency is set to 100 kHz with an external 10 µH inductor. The code is implemented in a DSP from Texas Instruments (TMS320F28335) to build the required PWM for both in and out inverters. A 200 ns dead band time is enough to guarantee no leg short circuit. Figure 10 presents the waveforms for all modulations and highlights a good match between theory and practical results. This low power converter is used to validate the proposed modulation strategy with good accuracy regarding open loop operation. Current studies focus on the converter electrical model with the observation of setting parameter influence and component values on global system behaviour.

The ringing associated with the switching transients must be avoided as much as possible. ZVS behaviour is then investigated to guarantee soft switching in the whole operating point. In

$$I_{\mathrm{RMS}} = \frac{1}{2Lf}\sqrt{D_1V_1\left(1 - \frac{4}{3}D_1\right) + D_2(nV_2)\left(1 - \frac{4}{3}D_2\right) + \frac{nV_1V_2}{3}\left(1 - \frac{2|\varphi|}{\pi}\right)\left(1 - \frac{|\varphi|}{\pi} + \frac{\varphi^2}{\pi^2} - 3[D_1(1 - D_1) + D_2(1 - D_2)]\right)} \tag{19}$$

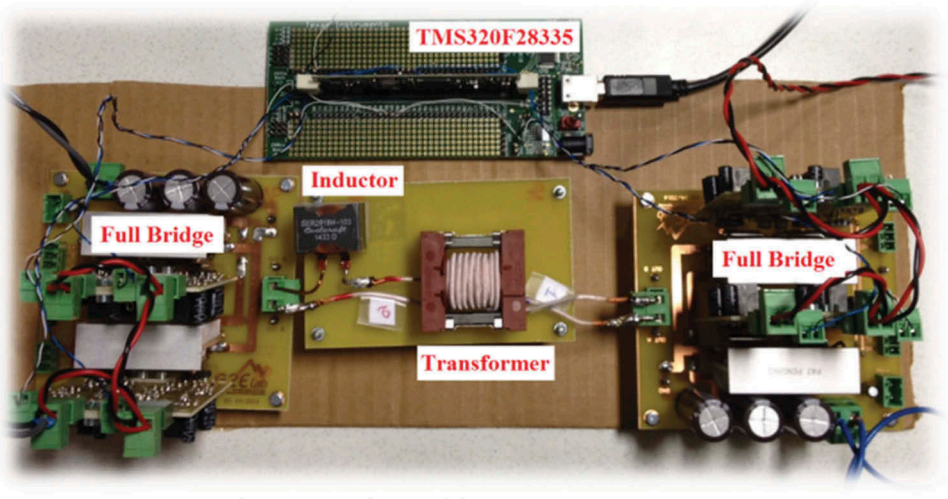


Figure 9. View of low power prototype.

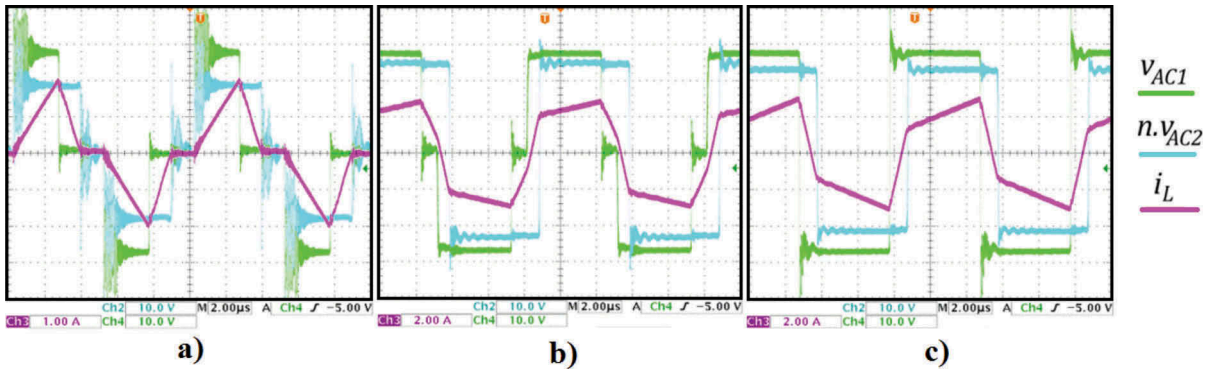


Figure 10. Practical results with low power DAB. (a) Triangle, $P = 15W$, $V_1 = 28$ V, $V_2 = 19$ V. (b) Modulation M, $P = 30W$, $V_1 = 28$ V, $V_2 = 25$ V. (c) Phase-shift, $P = 45W$, $V_1 = 28$ V, $V_2 = 24$ V.

Figure 10(a), the transient when current is zero highlight oscillations which are not catastrophic considering the low power transfer when using Triangle modulation. The related losses can be extracted with the design heatsink.

2.8. *Zero voltage switching for all operating point*

With the proposed strategy, ZVS for both full bridges is achieved for all operating points. Indeed, an analytical expression for the switched current, for every switching time t_0, t_1 and t_2, has been derived and this helps to determine their progression with the different modulation and it is possible to show a ZVS behaviour for all switches. The aim is to help the MOSFETs to switch on with a reduced voltage thanks to its body diode which conducts current in the reverse direction. MOSFETs have an intrinsic parasitic capacitor which acts like a snubber. This reduces dramatically the turn ON losses when used in HF. Knowing this condition, we can imagine adding external capacitor to increase snubber ability of MOSFETs if needed.

Table 3 gives the conditions for being in ZVS mode according to each modulation presented in Figure 11. For better understanding, p refers to primary side and s to secondary side

When solved, those equations validate the conditions for every operating point. However, the mathematical condition referred to zero is the extreme limit in theory. In experimental test, the converter has demonstrated perturbations in the inverter when the switched current is closed to zero. This could be explained by the output capacitance of MOSFETs which needs a minimum of current to charge (and discharge respectively) in an appropriate duration before the end of the dead time. This perturbation has been observed with the SiC inverter and those transistors seem to require at least 3A to switch in good conditions with a dead time of 400 ns. In Figure 12, this effect of quasi-ZVS is shown. The current cross zero before the end of the voltage switch leading to an incomplete switching behaviour. Around this time, the opposite MOSFET forces the voltage the move quickly. The very high speed of SiC component brings HF resonances in the power part of the converter which

Table 3. Equations for ZVS condition.

Figure 11(a)

$$I(t_1) = \frac{D_1(V_1 - nV_2)}{Lf} > 0 \rightarrow \text{ZVS } p.$$
$$I(t_0) = I(t_2) = 0 \rightarrow \text{ZVS } s.$$

Figure 11(b)

$$I(t_0) = I(t_2) = 0 \rightarrow \text{ZVS } p.$$
$$I(t_1) = \frac{D_2(nV_2 - V_1)}{Lf} > 0 \rightarrow \text{ZVS } s.$$

Figure 11(c)

$$I(t_0) = -\frac{nV_2(|\varphi| - \pi + \pi D_1) + \pi D_1 V_1}{2\pi Lf}$$
$$I(t_1) = \frac{V_1(2|\varphi| - \pi) + \pi n V_2}{4\pi Lf}$$
$$I(t_2) = -\frac{nV_2(|\varphi| - \pi D_1) + \pi D_1 V_1}{2\pi Lf}$$
$$\left.\begin{matrix} I(t_0) < 0 \\ I(t_2) > 0 \end{matrix}\right\} \rightarrow \text{ZVS } p.$$
$$I(t_1) > 0 \rightarrow \text{ZVS } s.$$

Figure 11(d)

$$I(t_0) = -\frac{nV_2(2|\varphi| - \pi) + \pi V_1}{4\pi Lf}$$
$$I(t_1) = \frac{V_1(|\varphi| - \pi + \pi D_2) + \pi D_2 n V_2}{2\pi Lf}$$
$$I(t_2) = \frac{V_1(|\varphi| - \pi D_2) + \pi D_2 n V_2}{2\pi Lf}$$
$$I(t_0) < 0 \rightarrow \text{ZVS } p.$$
$$\left.\begin{matrix} I(t_1) > 0 \\ I(t_2) > 0 \end{matrix}\right\} \rightarrow \text{ZVS } s.$$

Figure 11(e,f)

$$I(t_0) = -\frac{\pi V_1 + nV_2(2|\varphi| - \pi)}{4\pi Lf} < 0 \rightarrow \text{ZVS } p.$$
$$I(t_1) = \frac{V_1(2|\varphi| - \pi) + \pi n V_2}{4\pi Lf} > 0 \rightarrow \text{ZVS } s.$$

perturbed the control. Index 1 refers to master leg of high voltage inverter (made of SiC MOSFETs), index 3 refers to master leg of low voltage inverter (made of Si MOSFETs) which is lagging 85 ns.

3. High power demonstrator specifications

The converter is a DAB converter with two parallelized LVDC inverter to interface 540 V and 28 V network with large voltage dynamics.

3.1. *Semiconductor*

In high integrated converter, every part of the system must be studied with care. First of all, semiconductors have been characterized with simulation to determine their losses (conduction and switching) as a function of current. Models were validated previously thanks to the datasheet. For a HVDC bridge 1200 V SiC MOSFETs are selected. Silicon Carbide technology is assumed mature enough to consider using in an aircraft system. SiC MOSFETs are very robust and today they compete with IGBTs in the 1200 V range. For LVDC, very high current with high dynamics are expected. This could lead to damage due to parasitic inductance and so an SMD Silicon MOSFET in 100 V has been selected to be sure it will handle the overvoltage.

In semiconductors, losses are from two types: conduction and switching. For conduction losses, it is easy to calculate its value according to the resistive nature of the MOSFET channel when current flows.

$$P_{\text{conduction}} = R_{\text{on}} {I_{\text{RMS}}}^2 \tag{25}$$

Where R_{on} is the 125°C transistor ON resistance and I_{RMS} the RMS current flowing.

The switching losses are more complex to evaluate. A study of conventional method did not give us an analytical and trustable way to characterize these losses. Classically, people separate the switching transient in different step, all based on electrical equations solved with datasheet [10]. However, results (values or curves) given by the manufacturer are often far from our case because parameters are environmentally dependant and values are provided for a specific operating point. This is why simulation is selected to study the transient thanks to Spice® model available on the manufacturer's website. The software used is LTSpiceIV. To get closer to reality, parasitic elements are taken into account from the beginning to determine the switching energy. The aim is not to characterize the component but only to understand the evolution of turn OFF energy. This study assumes no losses at turn ON with ZVS and some recycle energy stored in output capacitor. On the base of double pulse test, as shown in Figure 13, each MOSFETs has been studied in switching mode in order to determine their losses.

SiC MOSFETs tested are the 25 mΩ die from CREE in TO-247 packaging [13], p. 00]. In the model, $L_s = 9$ nH, $L_g = 15$ nH, $L_d = 6$ nH are used as stray inductances. The capacitances are set to constant values from datasheet ($C_{\text{gs}} = 2825$ pF, $C_{\text{ds}} = 70$ pF) and the creation of the channel is driven by a voltage-current-temperature-dependant equation. Figure 14 presents the results for switching energy (in μJ) for a switching current (in A).

Two distinct areas can be seen, first when current is lower than 20 A. ZVS allows the transistor to store and recycle energy during switching. In this range, the current is entirely supplied from stored energy and is not dissipated in the channel. For higher current, this is a typical parabolic curve for switching energy.

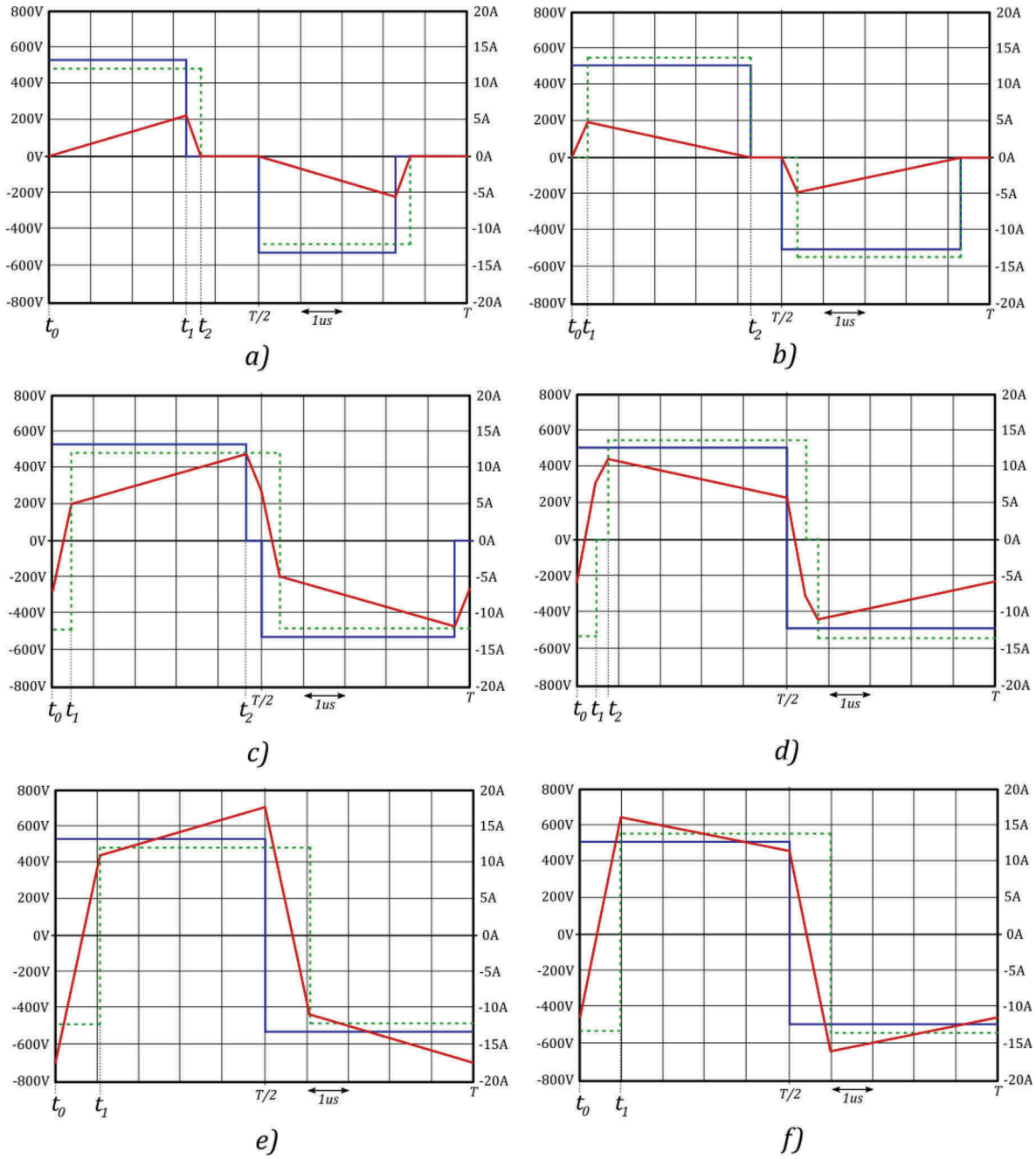


Figure 11. (a and b) Triangle modulation, (c and d) M modulation, (e and f) phase-Shift modulation.

Circuit simulations on PSIM® have highlighted that the maximum current will never exceed 20 A. That means almost no losses should be generated in the HVDC bridge.

In the LVDC bridge, very high current is expected. Figure 15 shows the switching losses results for Infineon reference IPT015N10N5 [14] with SMD packaging to reduce the parasitic inductance as much as possible.

The main advantage of simulation is the speed and the ability to change parameters if needed. In this way, several configurations (2, 3 and 4 dies in parallel) and the influence of gate resistance, output capacitance and layout inductance can be studied. A compromise leads this study to choose of 4 IPT015N10N5 dies with 8 Ω gate resistance and 10 nF external snubber with the consideration of few nH on drain and source.

Therefore, switching losses are:

$$P_{\text{switch}} = fE_{\text{off}} \tag{26}$$

And total losses are the sum $P_{\text{conduction}} + P_{\text{switch}}$

3.2. *Capacitor filter*

In the DAB, filtering is mainly capacitive and an original method is presented to determine required values without knowledge of voltage waveform but based on current flowing inside capacitors.

From Figure 2 the definition of HF inductor's instantaneous current is:

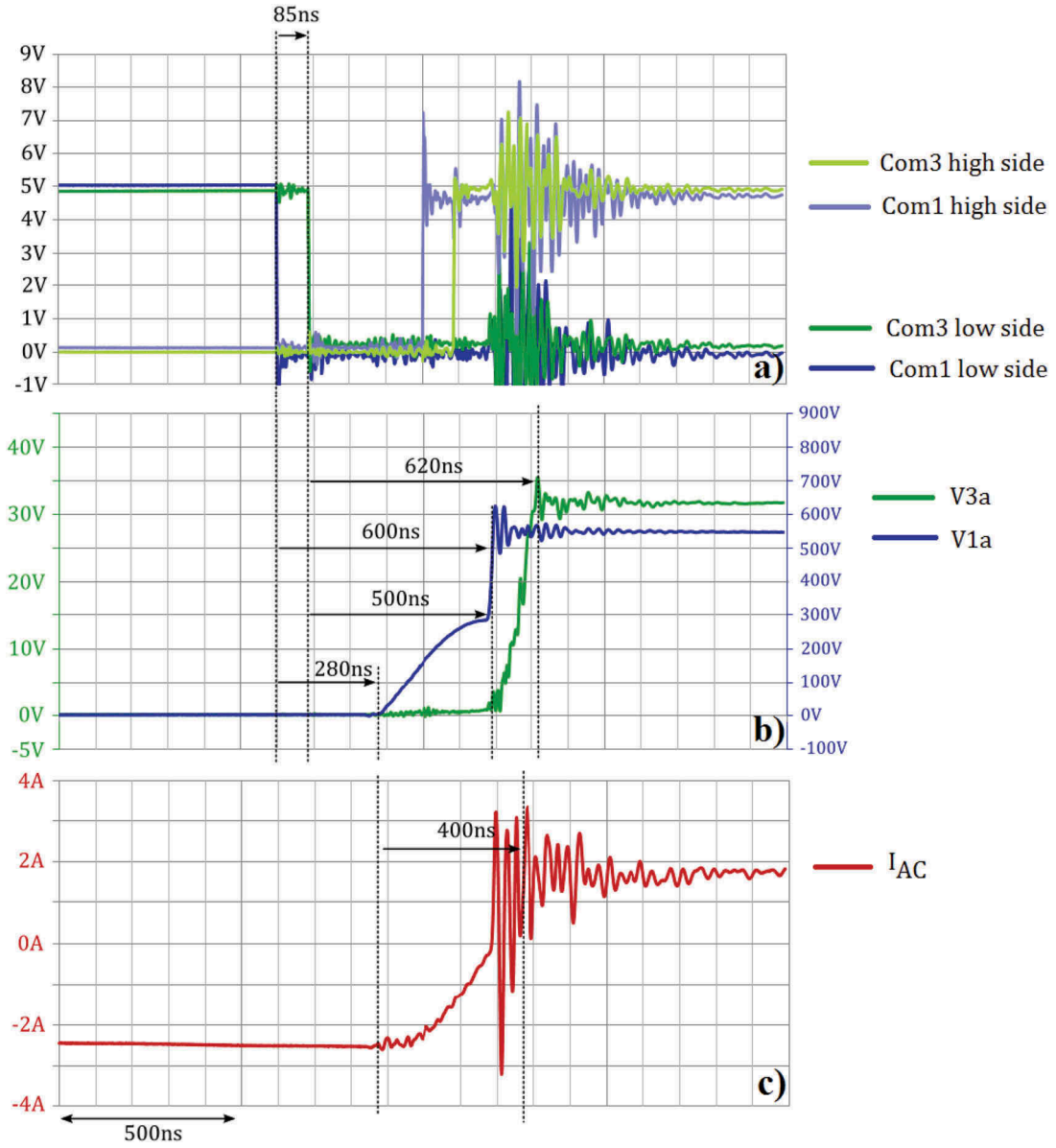


Figure 12. (a) DSP PWM, (b) inverter middle point voltage switch, (c) power current.

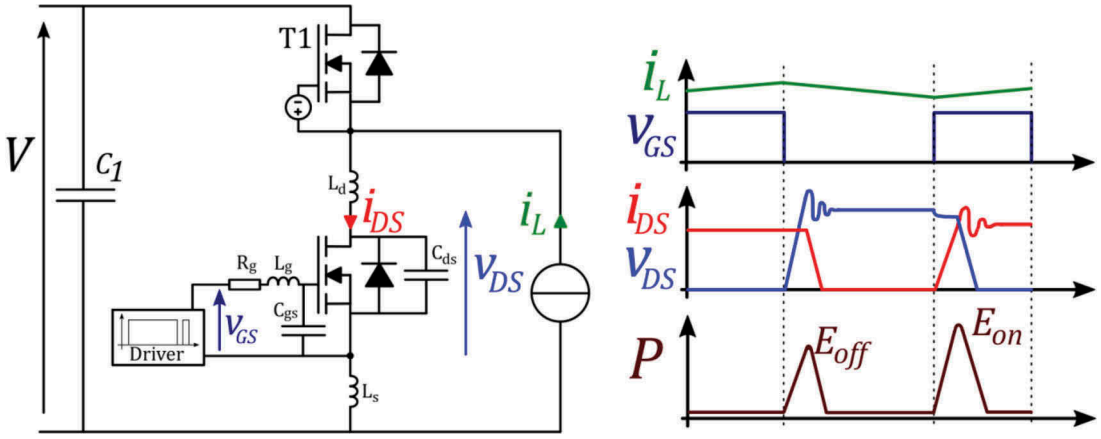


Figure 13. Double pulse test and classical waveforms for electrical.

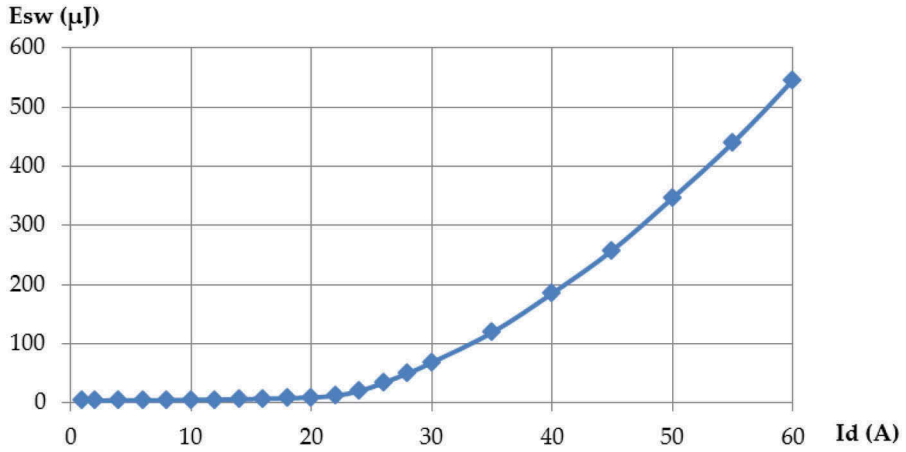


Figure 14. Switching energy simulation (µJ) for 1200 V SiC MOS C2M0025120D.

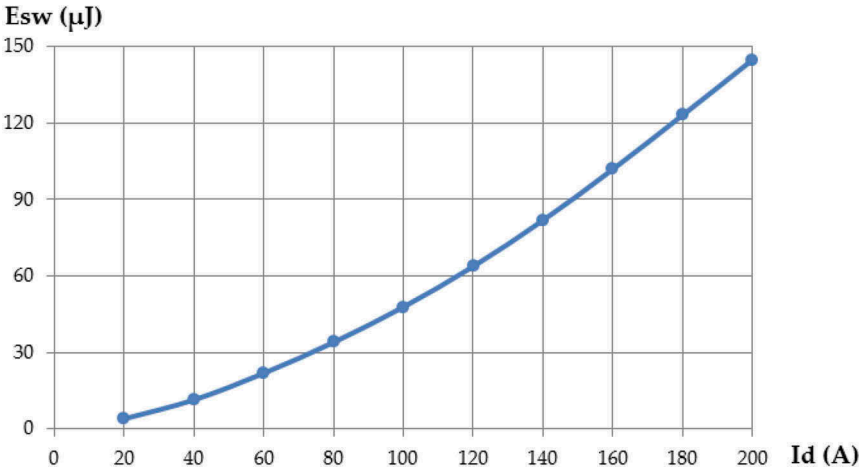


Figure 15. Switching energy simulation ((µJ) for 100 V Si MOS IPT015N10N5.

$$v_L = L\frac{di_L}{dt} = v_{AC1} - n.v_{AC2} \tag{27}$$

The critical point is considered in Phase-Shift modulation. v_{AC1} and v_{AC2} are square wave with $\pm V_i$ values. At the secondary side after the rectifier i_L is viewed as follows

In addition, the DC current is represented by the equation:

$$I_2 = \frac{nV_1}{Lf}\frac{\varphi}{2\pi}\left(1 - \frac{|\varphi|}{\pi}\right) \tag{29}$$

Therefore, capacitor current is given by:

$$i_c = i_{L-\text{red2}} - I_2 \tag{30}$$

Voltage ripple is defined by the difference between its peaks. The scheme is repeated at 2f because the rectifier doubles the frequency of the current waveform. There is a derivative relationship between voltage and current and it is known that peaks of voltage

$$\begin{aligned} i_{L-\text{red2}} \;=\; & -n\left(\frac{V_1 + nV_2}{L}t - \frac{\pi V_1 + 2nV_2\varphi - \pi nV_2}{4\pi Lf}\right) \; if \; 0 < t \le \frac{\varphi}{2\pi f} \\ & + n\left(\frac{V_1 - nV_2}{L}\left(t - \frac{\varphi}{2\pi f}\right) + \frac{2V_1\varphi - \pi V_1 + \pi nV_2}{4\pi Lf}\right) \; if \; \frac{\varphi}{2\pi f} < t \le \frac{1}{2f} \\ & + n\left(\frac{-V_1 - nV_2}{L}\left(t - \frac{1}{2f}\right) + \frac{\pi V_1 + 2nV_2\varphi - \pi nV_2}{4\pi Lf}\right) \; if \; \frac{1}{2f} < t \le \frac{1}{2f} + \frac{\varphi}{2\pi f} \\ & - n\left(\frac{-V_1 + nV_2}{L}\left(t - \frac{1}{2f} - \frac{\varphi}{2\pi f}\right) - \frac{2V_1\varphi - \pi V_1 + \pi nV_2}{4\pi Lf}\right) \; if \; \frac{1}{2f} + \frac{\varphi}{2\pi f} < t \le \frac{1}{f} \end{aligned} \tag{28}$$

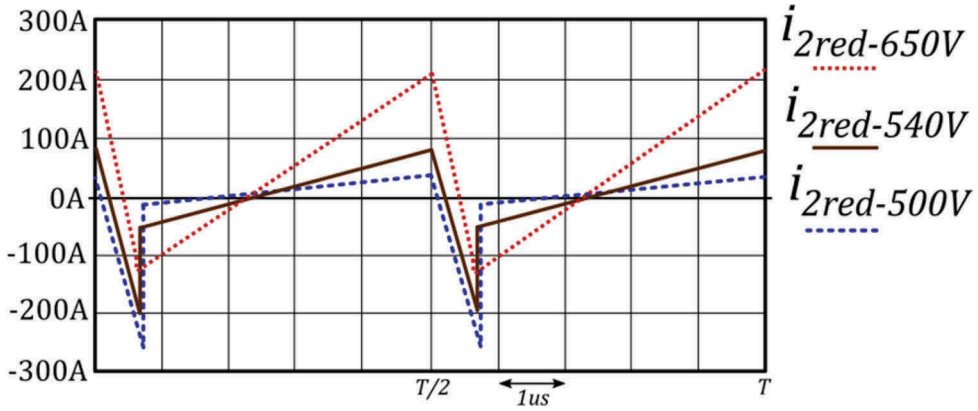


Figure 16. Capacitor current for $V_1 = 650V$ (red) 540 V (brown) 500 V (blue).

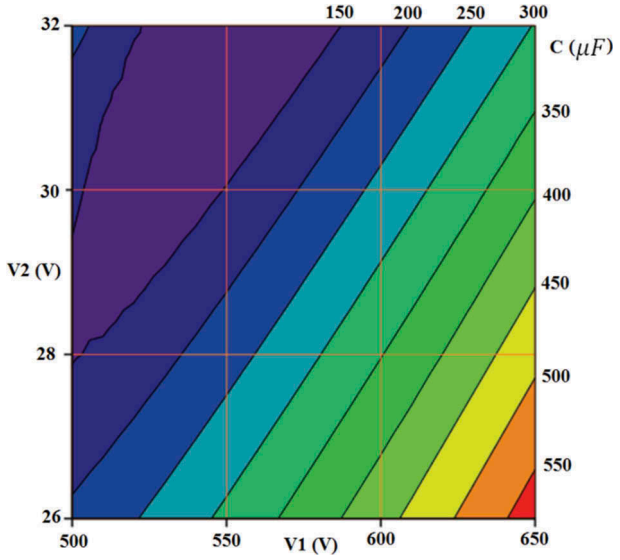


Figure 17. Required capacitance to meet the specification. Critical point is (650 V and 26 V) and $C_2 = 576\mu F$.

appear when the current crosses zero. Actually, the voltage ripple is proportional to current integral between two consecutives zero crossings. Now the problem is the low-frequency variation of voltage. Indeed, those consecutive zero crossings depend on values of the DC port. Figure 16 illustrates this phenomenon with three values of HVDC bus.

To overcome the difficulties of analytically expressing the zero crossing, the trick is to integrate the absolute value of i_c and not the instantaneous value of i_c. This will work because the mean of i_c is zero. In other word, (t_0, t_1 and t_2) are the three consecutives zero crossings. Therefor the following equation gives:

$$\int_{t0}^{t1} i_c dt = -\int_{t1}^{t2} i_c dt \tag{31}$$

In absolute value this becomes

$$\int_{t0}^{t1} |i_c| dt = \int_{t1}^{t2} |i_c| dt = \frac{1}{2}\int_{t0}^{t2} |i_c| dt = \frac{1}{4}\int_{t0}^{t0+T} |i_c| dt \tag{32}$$

But

$$\int_{t0}^{t1} i_c dt = C.\Delta V \tag{33}$$

At the end, a MathCAD® file is used to calculate this integral and the capacitance is provided based on required ripple ($\Delta V_1 < 5V$ et $\Delta V_2 < 500mV$ here).

$$C = \frac{1}{4.\Delta V}\int_0^T |i_c| dt \tag{34}$$

In the graphic (V_1, V_2) in Figure 17, it is possible to know, at nominal power, the critical value which respects the specification for all operating points. This kind of method is specifically fit for converters with large dynamics and large scale of operating point because this gives as well the critical point as the tendency and its derivative. As an industrial manufacturer, it is important to know what gain can be expected if one constraint is slightly modified.

Figure 18 presents the simulation ripple voltage, compute with PSIM®, for the validation of the required capacitance value which limit the ripple to 500 mV.

The best candidates have been highlights to be in ceramic technology for LVDC thanks to their ability to absorb extreme current. In the HVDC port, the characterization method is similar. A value of $C_1 = 4\mu F$ has been derived from the analysis. For high voltage a good compromise is the use of polypropylene film capacitor.

3.3. *Inductor and transformer*

The inductor naturally limits the transferable power. A maximum inductance is defined by the following equation when the phase angle is maximum.

$$P = \frac{nV_2V_1}{Lf}\frac{\varphi}{2\pi}\left(1 - \frac{|\varphi|}{\pi}\right) \tag{35}$$

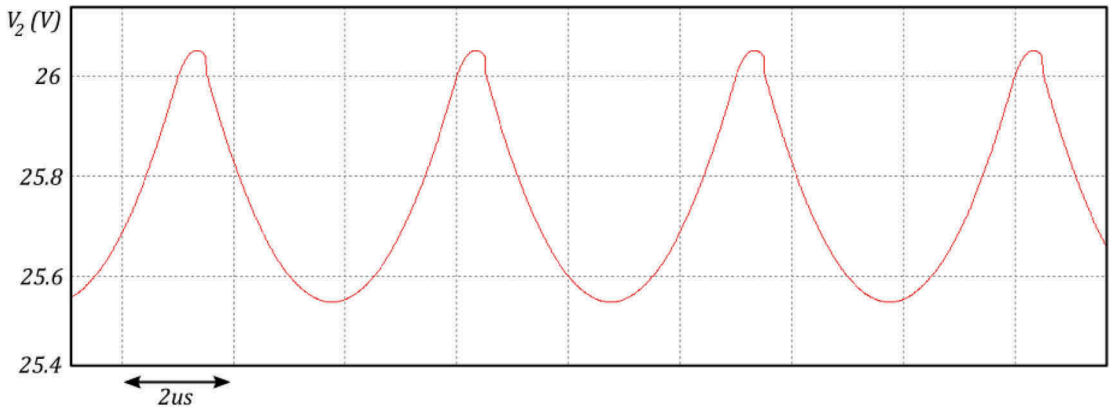


Figure 18. Voltage ripple of 26 V inverter. Capacitance value is $C_2 = 576\mu F$.

$$L_{\max} = \frac{nV_{2\min}V_{1\min}}{8fP_{\max}} \tag{36}$$

To reach the objectives of high integration, planar transformer is expected to be the best technological solution. The reason is mainly the reduction of magnetic core for the same VA rating. The difficulty which must face is the large ratio needed between the high voltage port and the low voltage port. This ratio is about 17. This goes along with the complex architecture of windings when the designer tends to reduce parasitic elements [15]. Different solutions have been studied in L2EP laboratory in France and their results highlight two main solutions. One transformer made of copper foil, composed of nine elements all insulated from each other. And another transformer made on a PCB. In a first try a PCB planar transformer has been integrated to the high-power converter but it had to be changed to a more classical transformer made of litz wire because of the very high parasitic capacitance of planar (around $500pF$) which was ringing with the leakage inductance. Unwanted oscillations have occurred leading to a bad use of the converter. The wound transformer is unfortunately bigger but thanks to its higher leakage inductance and the good use of interconnections, the total required inductance has been mastered to tune the needs of the DAB converter. This transformer is made of four U46 in 3F3 material. The primary side is composed of 17 turns (800×0.071 litz wire). The two secondary sides consist of 1 turn (2200×0.1). Its leakage inductance is 22µH and its parasitic capacitance is closed to 10pF.

3.4. *Thermal and layout consideration*

The next step, with known losses, was to imagine the converter architecture. Increased power density encourages the use of forced air cooling system associated with extrusion shapes. PCB and heat sink were studied together to find an industrial and integrated assembly. The selected solution is the use of four layers PCB with insulator film for the surface mount components. All thermal interfaces were considered to calculate the thermal resistance required for the heat sink. To help heat transfer of SMD LVDC switches, vias are implemented in the PCB. Moreover, vias handle electrical connection between all layers. The driver is in mezzanine to build a modular converter.

The metallization thickness of vias is low enough to neglect skin and proximity effect. This means only DC resistance is considered and with analogy thermo-electric the thermal resistance.

$$R_{\mathrm{DC}} = \frac{l_{\mathrm{via}}}{\sigma_{\mathrm{cu}}.S_{\mathrm{via}}} \tag{37}$$

$$R_{\mathrm{th-via}} = \frac{l_{\mathrm{via}}}{\sigma_{\mathrm{th-cu}}.S_{\mathrm{via}}} \tag{38}$$

Based on $R_{\mathrm{th-via}}$ and staggered rows placement, the surfaced thermal resistance of via is calculated with:

$$R_{\mathrm{th_s}} = R_{\mathrm{th-via}}.\left(\emptyset_p + \delta\right)^2.\cos\left(\frac{\pi}{6}\right) \tag{39}$$

$\emptyset_p$is the metalized pad diameter, δ is the length between two pads.

The converter must accept 50% of nominal power overload for 10s but regarding thermal time constant this impact is assumed only on the interface between the die and the heat sink. The junction temperature shall remain below manufacturer's recommendation (often 150°C). The thermal resistance between case and ambient is the only thing the designer can act on.

$$R_{\mathrm{th_{ha}}} = \frac{T_j - T_a - R_{\mathrm{th_{jh}}}.P_{@5625\mathrm{W}}}{P_{@3750\mathrm{W}}} \tag{40}$$

$P_{@iW}$ are losses when the power equal iW.

Rth_{jh} is the sum of several resistances in series (Rth_{jc}, grease, PCB, vias, insulator… dependant on application). Every point can be a future improvement, for instance, multilayer IMS or ceramic substrate. When all elements are calculated, the heat sink must be selected to meet the specification of component. Here is the example for the LVDC PCB.

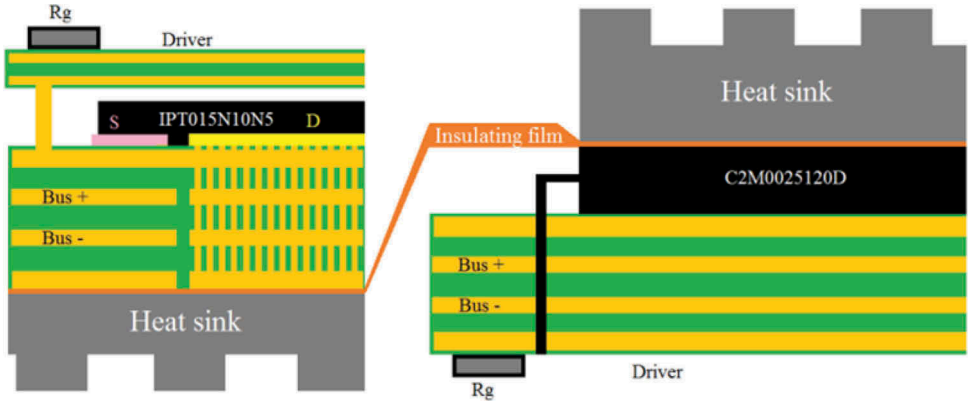


Figure 19. Layout principle of LVDC (left) and HVDC (right) semiconductor.

$$R_{\mathrm{th_{ha}}} = \frac{T_j - T_a - \left(R_{\mathrm{th_{jc}}} + R_{\mathrm{th_{vias}}} + R_{\mathrm{th_{insulator}}}\right).P_{@5625\mathrm{W}}}{P_{@3750\mathrm{W}}} \tag{41}$$

Analytical study has been performed to calculate resistance for vias, Sil-Pad K-10 insulator and epoxy FR4. It is interesting to note the gain, around 36 times, between vias and epoxy to evacuate properly the calories.

$$R_{\mathrm{th_{s-vias}}} = 1.47 \times 10^{-4}\mathrm{K.m/W} \tag{42}$$

$$R_{\mathrm{th_{s-isolant}}} = 1.17 \times 10^{-4}\mathrm{K.m/W} \tag{43}$$

$$R_{\mathrm{th_{s-FR4}}} = 53.3 \times 10^{-4}\mathrm{K.m/W} \tag{44}$$

3.5. *High power demonstrator results*

A 3.75 kW demonstrator has been built, based on previous specifications and choices. The high integration forced us to consider innovative technology because the build objectives were 200mm × 140mm × 80mm size and 2 kg. A special care is taken with magnetics in planar technology to minimize size and weight. Concerning the semiconductor switching behaviour, the layout is carefully designed to reduce as much as possible the inductive loop during the switching transient. To be efficient, the return in the control signal layout is minimum. As shown in Figure 19, the driver is placed raised above the power part to make this converter more suitable for test proceeding. Figure 20 shows the proposed layout for a LVDC full bridge leg. Each switch is composed of 4 CMS MOSFETs. In the middle can be seen the footprint of gate resistance and the 2 × 4 connector with the driver.

The demonstrator is in characterization at this moment. It weights 2.6 kg for a volume of $250 \times 180 \times 120\mathrm{mm}^3$. These results are still under the original objectives but first thermal and electrical tests have shown an oversizing concerning thermal management, which can be a future improvement towards size and weight reduction. Unused space is another way of progress. And the good mastering of planar transformer technology could help to save at least 400 g and divided per 3 the volume of the magnetics. Figure 21 shows a view of the DAB converter under tests and improvements and Figure 22 illustrates the efficiency of this converter for a Phase-Shift modulation with $V_1 = 540\mathrm{V}$ and $V_2 = 32\mathrm{V}$.

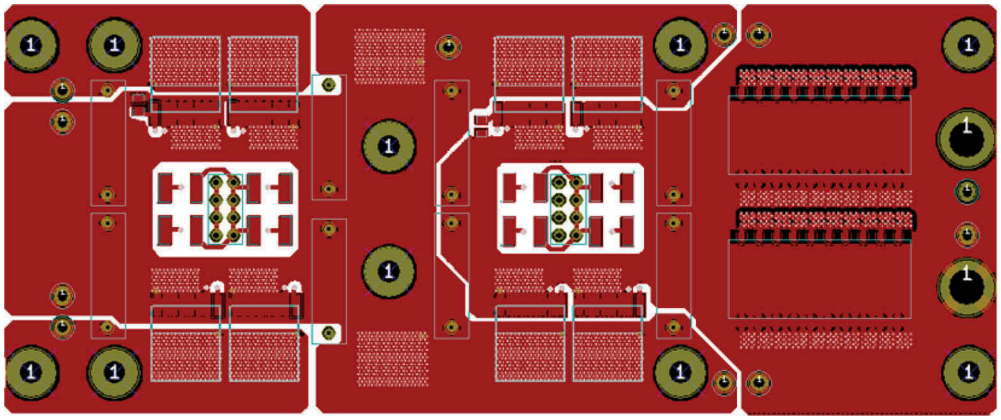


Figure 20. Layout of LVDC full bridge leg.

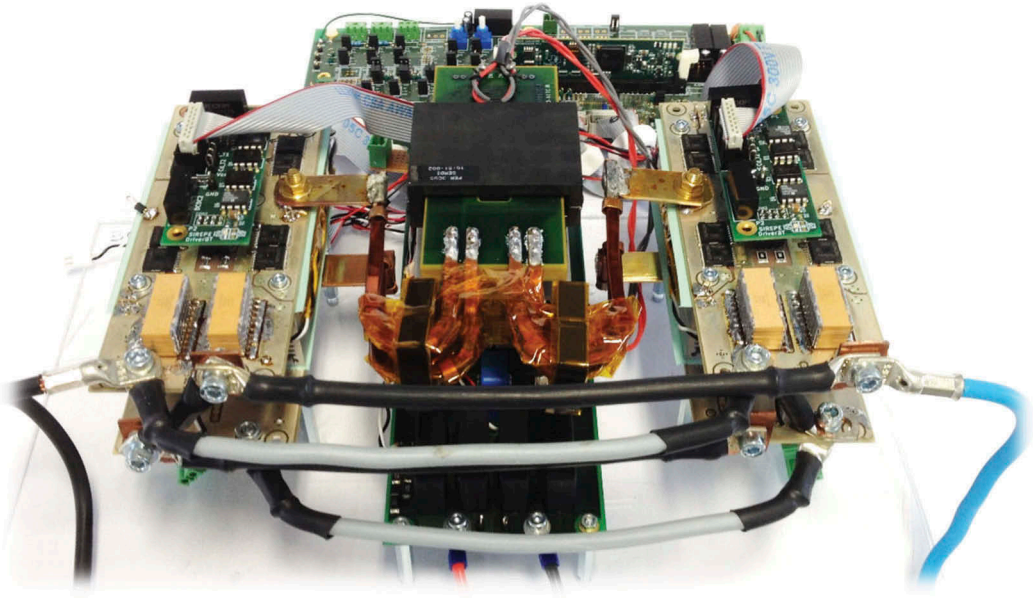


Figure 21. View of DAB.

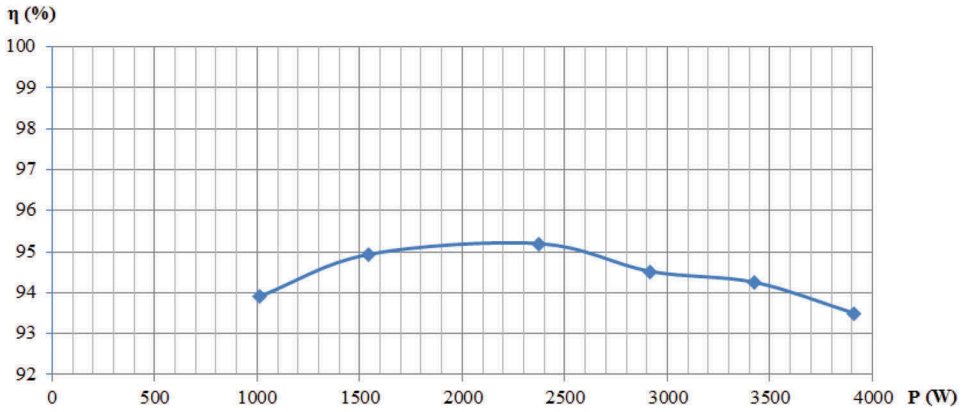


Figure 22. Efficiency of the DAB in Phase-Shift modulation for $V_1 = 540V$ and $V_2 = 32V$.

4. Conclusions

In this article the modulation strategy of a DAB DCDC reversible converter is presented. The proposed strategy minimizes RMS current and guarantees ZVS for all operating points. An original method for dimensioning capacitor filters, based on current waveforms, is demonstrated and validate with simulation. Every part of the converter has been studied with care, from the power semiconductor up to thermal management taking into account PCB layout, insulation and 3D architecture. A low-power prototype is built to validate theoretical assumptions about modulation. And a high power 3.75 kWconverter is characterised to prove active conversion system suits aircraft specifications.

Current research aims to carefully understand the behaviour of the high-power DAB in order to find possible improvements.

Nomenclature

D1	Duty cycle used for the HVDC full bridge
D2	Duty cycle used for the LVDC full bridge
DAB	Dual active bridge
f	Switching frequency
φ	Phase angle between v_{AC1} and v_{AC2}
HF	High frequency
HDVC	High-voltage direct current
I_L	RMS value of the current through L
L	HF DAB converter inductance
LVDC	Low-voltage direct Current
n	Transformer turns ratio
P	DAB power (assuming a lossless DAB)
T	Switching period
V_1	HVDC port voltage
V_2	LVDC port voltage
v_{AC1}	AC voltage generated by the HVDC full bridge
v_{AC2}	AC voltage generated by the LVDC full bridge
ZVS	Zero voltage switching

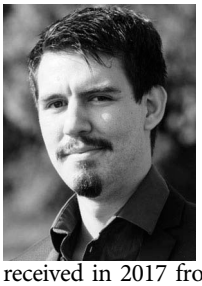
Acknowledgements

This Ph.D. work is in partnership between THALES AES Corporation and the Grenoble Electrical Engineering Laboratory G2Elab. Other work carried out in collaboration with L2EP laboratory specializes in magnetics to gain weight and size reduction of magnetic parts.

Disclosure statement

No potential conflict of interest was reported by the authors.

Notes on contributors



Maximin Blanc was born in Albertville, France, in 1991. He studied electrical engineering at Grenoble Institute of Technology majoring in power electronics and received the M.Sc. degree in 2014. He worked at THALES AES in partnership with Grenoble Electrical Engineering Laboratory in the Power Electronic team for the PhD degree, received in 2017 from Université Grenoble Alpes. He is currently working in SIREPE, a French company specialized in power electronic converter design. His current research interests include the analysis, the design, and the optimization of high frequency power converter suitable for high integrated application.

Yves Lembeye was born in 1966. He received the Ph.D. degree in 1997 in electrical engineering from the *Grenoble-INP* and the HDR in 2008 from the *Univ. Grenoble Alpes* – France.

He is professor at the *Institut Universitaire* de *Technologie 1 of Grenoble (Univ. Grenoble Alpes)*. His research activities take place in the Grenoble Electrical Engineering Laboratory (G2Elab) within the Power Electronics research group.

His centre of interest is low power DC/DC and AC/DC converters high current low voltage converters and passive components integration. He has published over 80 technical papers in these areas.

(G2Elab, Bâtiment GreEn-ER, 21 avenue des martyrs, CS 90624, 38031 GRENOBLE Cedex, France. Phone: +33-4-76-82-63-02, E-mail: Jean-Paul.Ferrieux@g2elab.grenoble-inp.fr)

Jean-Paul Ferrieux was born in 1959. He received the Ph.D. degree and the HDR both in electrical engineering in Grenoble – France, in 1984 and 1989, respectively.

He is Professor at the Grenoble-Alpes University – IUT1 – Grenoble. His research activities take place in the Grenoble Electrical Engineering Laboratory (G2Elab) within the Power Electronics research group.

His major field of interest is power electronics (static converters and resonant converters, passive components). He has published over 100 technical papers in these areas and he's co-author of a power electronics book entitled 'Switch-mode power supplies, resonant converters'.

(G2Elab, Bâtiment GreEn-ER, 21 avenue des martyrs, CS 90624, 38031 GRENOBLE Cedex, France. Phone: +33-4-76-82-63-02, E-mail: Jean-Paul.Ferrieux@g2elab.grenoble-inp.fr)

Corentin Rizet received the Engineering degree from the Grenoble Institute of Technology, France, in 2007 and a Ph. D. degree with the Laboratory of Electrical Engineering of Lille (L2EP), the Grenoble Electrical Engineering Laboratory (G2ELAB) and APC by Schneider Electric. He has founded SIREPE in 2012, a private research laboratory where he works as research engineer and chairman.

His main research interests include optimal design and architecture of converter, especially the multi-level and interleaved coupled topologies.

Arnaud Mahe was born in Saint-Nazaire, France, in 1976. He received the Master's Degree in Engineering from CUST, Clermont-Ferrand, France, in 2000. He is working in different units of the THALES Group in the field of Power Electronics as a Research/Design Engineer.

Taoufik Bensalah, taoufik.bensalah@fr.thalesgroup.com

ORCID

Arnaud Mahe http://orcid.org/0000-0001-6843-7514

References

[1] Krismer F, Biela J, Kolar JW. A comparative evaluation of isolated bi-directional DC/DC converters with wide input and output voltage range. In: *Industry applications conference, 2005. Fourtieth IAS annual meeting. Conference record of the 2005*. Vol. 1. 2005. p. 599–606.

[2] Krismer F. Modeling and optimization of bidirectional dual active bridge DC-DC converter topologies [Diss.]. Eidgenössische Technische Hochschule ETH Zürich, Nr. 19177; 2010.

[3] De Doncker RW, Divan DM, Kheraluwala MH. A three-phase soft-switched high-power-density DC/DC converter for high-power applications. IEEE Trans Ind Appl. 1991;27(n° 1):63–73.

[4] Schibli N. Symmetrical multilevel converters with two quadrant DC-DC feeding [Thèse]. Ecole Polytechnique Fédérale de Lausanne, 2000.

[5] Krismer F, Kolar JW. Closed form solution for minimum conduction loss modulation of DAB converters. IEEE Trans Power Electron. 2012 janv;27 (1):174–188.

[6] Wang Y, de Haan SWH, Ferreira JA. Optimal operating ranges of three modulation methods in dual active bridge converters. In: IPEMC '09. IEEE 6th International Power Electronics and Motion Control Conference, 2009. Wuhan: IEEE; 2009. p. 1397–1401.

[7] Mi C, Bai H, Wang C, et al. Operation, design and control of dual H-bridge-based isolated bidirectional DC-DC converter. IET Power Electron. 2008 déc;1 (4):507–517.

[8] Oggier G, Ledhold R, Garcia GO, et al. Extending the ZVS operating range of dual active bridge high-power DC-DC converters. In: PESC'06. 37th IEEE

Power Electronics Specialists Conference, 2006. Jeju South Korea: IEEE; 2006. p. 1–7.
[9] Oggier GG, Garcia GO, Oliva AR. Switching control strategy to minimize dual active bridge converter losses. IEEE Trans Power Electron. 2009 juill;24 (7):1826–1838.
[10] Zhao B, Song Q, Liu W. Power characterization of isolated bidirectional dual-active-bridge DCDC converter with dual-phase-shift control. IEEE Trans Power Electron. 2012 sept;27(9):4172–4176.
[11] Zhao B, Song Q, Liu W, et al. Overview of dual-active-bridge isolated bidirectional DCDC converter for high-frequency-link power-conversion system. IEEE Trans Power Electron. 2014 août;29(8):4091–4106.
[12] Brandelero JC. Conception et réalisation d'un convertisseur multicellulaire DC/DC isolé pour application aéronautique. France: Université de Toulouse; 2015.
[13] CREE. MOSFET C2M0025120D. USA:CREE.
[14] Infineon. MOSFET IPT015N10N5. Germany: Infineon.
[15] Lu W, Chunying G. Detailed design of high-frequency planar power transformer. In: 2011 6th IEEE Conference on Industrial Electronics and Applications (ICIEA). Beijing: IEEE; 2011. p. 1610–1614.