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Lyubomir Kerachev, Yves Lembeye, Jean-Christophe Crebier. Study of Techniques for Flip-Chip Bonding to Organic Substrates for Low-Power Applications. *IEEE Transactions on Components, Packaging and Manufacturing Technology*, 2015, 5 (10), pp.1533–1540. 10.1109/TCPMT.2015.2470550 . hal-02277687

HAL Id: hal-02277687

<https://hal.science/hal-02277687>

Submitted on 26 May 2021

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Study of Techniques for Flip-Chip Bonding to Organic Substrates for Low-Power Applications

Lyubomir Kerachev, Yves Lembeye, and Jean-Christophe Crebier

Abstract—This paper deals with the study of technologies for flip-chip assembly of CMOS integrated power converters on standard FR4 organic substrates. Tests for the characterization of commercially available technologies for microassemblies, such as anisotropic adhesive bonding, thermocompression bonding, thermosonic/ultrasonic bonding, and solder bonding, are carried out. The aim of this paper is to determine the most suitable flip-chip bonding technology for power CMOS circuits with more than 50 pads. First, the coupled design of the CMOS chip and the corresponding substrate dedicated to low-power microconversion (10 W) is presented. It is shown that the parasitic resistances and inductances of the interconnections increase the conduction and switching losses of the device. This leads to a temperature rise, which can limit the operating ratings of the circuit. The experimental results are provided to evaluate each technology for flip-chip assembly.

Index Terms—CMOS integrated circuits, electronics packaging, flip-chip devices.

I. INTRODUCTION

THE increase in the power density is one of the leading criteria in designing power converters. Therefore, many works focus on the development of highly integrated microconverters [1]–[4]. Concepts based on standard CMOS fabrication processes are exploited in order to optimize the performance while downsizing the cost, the complexity, and the number of active devices to be implemented [5]–[7]. However, the electrothermomechanical interconnections can limit the efficiency of the converters and increase their size. For instance, the standard IC packages with an increased number of I/O pads suffer from larger volume, increased cost, increased wire-bonding resistances, and parasitic inductances [8]–[11] while offering normalized assembly requirements. In some cases, the thermal pad increases significantly the heat removal capability of the chip [25], [26].

Flip chip and associated assembly technologies allow the connections between the chip's pads and the tracks of the substrate via adhesive paste, stud bumps, copper pillars, or solder bumps instead of bonding wires [12]. This results in significant downsizing of chip package, reducing the assembly cost, and decreasing the parasitic phenomena, such

as pad resistances and inductances [13], [14]. In addition, it reduces the number of thermal interfaces between the chip and the substrate, which operates as the principal heat removal path. The most popular flip-chip technologies are adhesive flip-chip bonding [15], [16], thermocompression bonding [17], thermosonic/ultrasonic bonding [18], and solder bump bonding [19]. Flip-chip bonding can also optimize the thermal management of the power device if a large number of bonds are realized in association with an appropriate design of the copper tracks on the substrate. Thus, the heat can be evacuated to the ambient temperature through the bumps, their number being almost inversely proportional to the equivalent thermal resistance of the interconnection layer.

In the next sections, a CMOS H bridge designed for low-power highly integrated microconverters will serve as a basis for comparison of the characteristics of the flip-chip technologies cited above. It is designed for 2-A maximal current, 5 V maximal voltage, and up to 1-MHz switching frequency. This involves the increased number of pads of the device in order to share the electrical and thermal constraints. The standard design rules of the printed circuit boards (PCBs) are also considered in the design of the chip so that the die could be mounted directly on the substrate using the conventional PCBs and the standard commercial flip-chip technologies. In such a way, the chip and the substrate are codesigned to optimize number and location of the pads over the die surface. The assemblies are compared in terms of reliability, electric resistances of the joints, and thermal management capabilities. The custom flip-chip bonding technique inspired by the solder bumping technology is also proposed and experimentally characterized.

II. DESIGN OF THE POWER CMOS DIE

A. Concept

The structure of the power CMOS die has been created so that it is more generic and could be implemented in various converter topologies, such as buck, boost, buck-boost, and interleaved converters. For this purpose, ten independent CMOS power inverter legs have been integrated in the same die with their associated gate driver circuits (Fig. 1). The command signals can be provided from any external source, such as microcontrollers, or any other logic circuits (FPGA, CPLD etc), but at a cost of increased number of I/O pads. The design of each inverter leg is based on the standard 0.35- μm 5 V CMOS fabrication process offered by austriamicrosystems. It is designed for the applications up to 2 A depending on the thermal capabilities of the package and the assembly (200-mA mean current per inverter leg). Since a standard

This work was supported in part by ANR Miconet 2 and in part by ANR ProCD Emergence.

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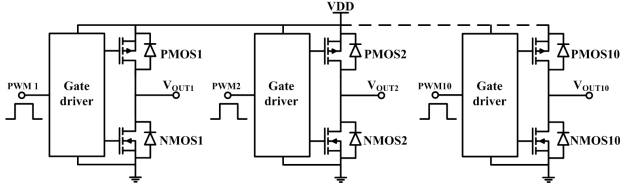


Fig. 1. Structure of the CMOS power die.

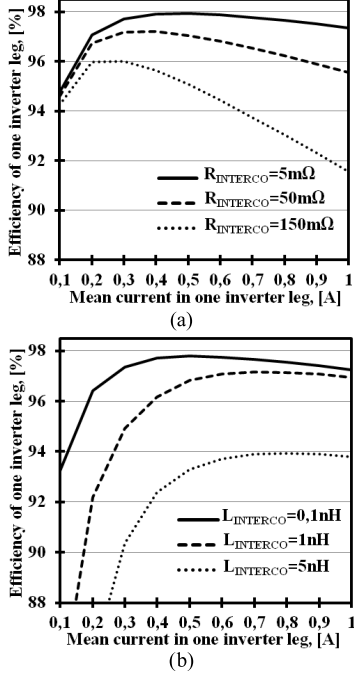


Fig. 2. CMOS inverter leg efficiency as a function of the mean load current ($V_{DD} = 5\text{ V}$, $f_{sw} = 1\text{ MHz}$, and $\alpha = 0.5$). (a) $L_{INTERCO} = 0.1\text{ nH}$. (b) $R_{INTERCO} = 5\text{ m}\Omega$.

CMOS technology process is used, only several characteristics of the MOSFETs, such as internal resistances and gate–drain–source capacitances, can be defined as a function of the gate width W of the MOSFETs [7]. A very special attention must be paid to minimize the length of the power tracks at the surface of the chip. The gate driver circuit used in association with each inverter leg is also optimized with respect to the switching losses of the power MOSFETs and its consumption [5]–[7].

Fig. 2(a) and (b) shows a Cadence simulation result of the efficiency of one CMOS inverter leg for different rates of the mean load current, different values of the interconnect resistances ($R_{INTERCO}$), and the parasitic inductances ($L_{INTERCO}$) for each I/O pad of the inverter leg when switching at 1 MHz with a duty cycle $\alpha = 0.5$. The values of the resistances of the MOSFETs at 25 °C obtained in the simulation are $R_{DSN} = 45\text{ m}\Omega$ and $R_{DSP} = 56\text{ m}\Omega$.

The simulation results show that 97% efficiency can be achieved over a wide current range even for higher power levels, the main limitation in this case being the heat removal capability of the extra losses. It clearly appears that it is mandatory to ensure a good thermal management of the assembly in order to keep the die operating under its maximal operating temperature which is 125 °C [20] while offering

TABLE I

LOSSES IN ONE CMOS INVERTER LEG FOR 200-mA AVERAGE CURRENT, 5 V DC, $\alpha = 0.5$, $R_{INTERCO} = 5\text{ m}\Omega$, AND $L_{INTERCO} = 0.1\text{ nH}$

Conduction losses	Switching losses	Driver losses	Losses in interconnect resistances
8.1mW	5.2mW	5.2mW	4mW

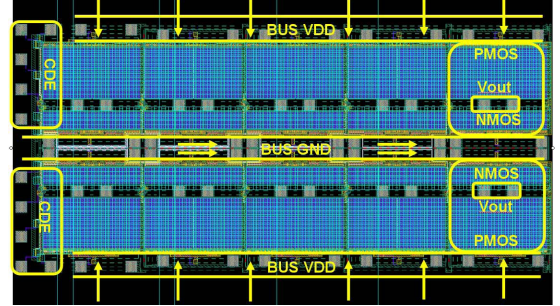


Fig. 3. Top layout of the power CMOS die.

a maximum power density level. The power losses are summarized in Table I at nominal current 200 mA under 5 V dc 1-MHz switching frequency.

Fig. 2(a) shows that the efficiency of one inverter leg is highly dependent on the value of the interconnect resistances. As it can be seen in Table I, the losses in the bumps are at the same level as the conduction losses, the switching losses, and the driver losses for only 5-m Ω bump resistance and 0.1-nH parasitic inductance.

Furthermore, the parasitic wiring inductances ($L_{INTERCO}$) create on one hand voltage overshoots during the switching period which could damage the device and on the other hand, increase the switching time of the MOSFETs which causes higher switching losses [Fig. 2(b)]. Reducing their values helps to suppress unwanted ringing and also to minimize the switching losses by reducing the switching time of the MOSFETs [27], [28]. This highlights the need of an efficient assembly and the impact of the parasitic resistances and inductances on the efficiency of the die (and consequently that of the converter where it is implemented) which is not always that critical at higher voltage applications, for example.

Fig. 3 shows the layout of the power die designed with respect to the standard PCB design rules for flip-chip assembly. The designs of both the PCB and the CMOS chip are driven by the need to keep the current uniformly spread among all the ten CMOS power inverter legs. The +dc supply terminal is connected to two tracks, one on each side of the device. The ground terminal (GND) is in the middle of the chip, between the two rows of the CMOS power inverter legs. This configuration allows maximum reduction of the resistances of the power tracks in the die, since the power nMOSFET and pMOSFET are vertically flattened. Besides, it allows uniform spreading of the pads over most of the surface of the die. The number of pads is determined with respect to their maximal current density given in Digital Rights Management of the technology [20] and based on the criteria that the equivalent bump resistances of each power terminal of the inverter legs are significantly reduced in comparison with the characteristics of the device. Thus, the surface of the die is

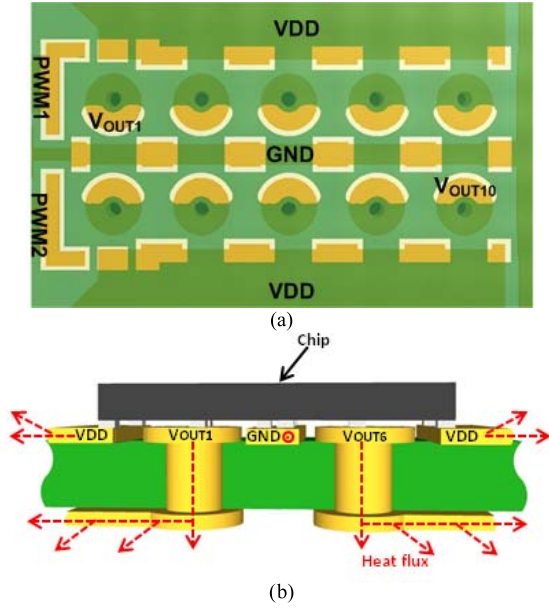


Fig. 4. Layout of the PCB. (a) Top view. (b) Cross section.

9.9 mm² (4.5-mm length and 2.2-mm width) and it contains 70 pads. The ten pads are dedicated to the command, 20 pads in parallel are dedicated to the GND (two pads in parallel per inverter leg), 20 pads in parallel are dedicated to the V_{DD} (two pads per inverter leg), and 20 pads are dedicated to the middle points (two per inverter leg). Hence, each inverter leg is closely connected to six pads for maximum heat removal while giving the opportunity to reduce the equivalent series resistance of each power terminal as well as the current density on each pad. In addition, the MOS devices being quite large, the use of two pads for each contact minimizes the current circulation in the conductive layers of the die. The position of each pad is optimized to reduce this current circulation at die level. As it will be introduced later, having two pads per contact also offers the great opportunity to perform four points measurement across each interesting part.

The design of the PCB has been carried out with a standard two-layer technology and material FR4 with the objective to ensure optimal thermal management of the assembly (Fig. 4). The output pads of each inverter leg are placed on vias in order to get a direct access to the outputs on the backside of the PCB. In that way, the heat can also be drained through the bumps to the copper tracks on the bottom layer. In order to achieve such PCB design, the shape of each power transistor has been optimized to enable the placement of the vias. The V_{DD} and GND tracks on the top layer of the PCB serve as the heat spreader as well.

B. Interest of the Flip-Chip Assembly of the Power Die

At first, the die has been packaged in ceramic quad flat package CQFP-44 using bonding wires to connect the chip pads to the package lead frames (Fig. 5).

Fig. 6 shows the circuit of one CMOS inverter leg with the parasitic interconnect resistances $R_{INTERCO}$ and $L_{INTERCO}$. Since it is integrated in the same die with its gate driver circuit, $R_{INTERCO}$ and $L_{INTERCO}$ between the drains of the transistors pMOS and nMOS and between the gate driver and the gates

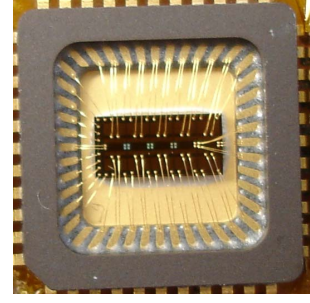


Fig. 5. Photo of the packaged die in package CQFP-44.

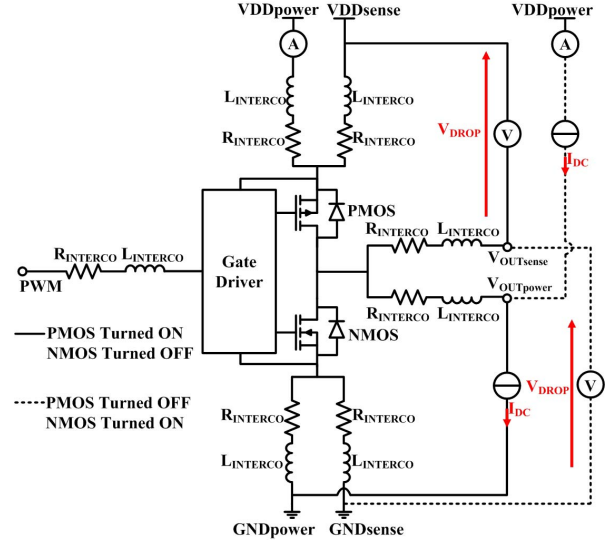


Fig. 6. Four-terminal measurement of the ON-state resistances of the power MOSFETs of one CMOS inverter leg integrated in a die.

of the transistors are neglected. The resistances between all the terminals of one inverter leg have been derived from the experiments. The approach described here has been used for the characterization of all interconnection techniques. First, each transistor is turned ON separately in order to make a dc current pass through and to measure its voltage drop V_{DROP} . The measured values of the dc current I_{DC} and of the voltage drop V_{DROP} allow calculating of the ON-state resistances of the power MOSFETs (1). The measures have been performed with an Agilent 34405A 5(1/2) digit multimeter. The values of the ON-state resistances of the power MOSFETs are measured with four-terminal sensing method in order to eliminate the impedances of the interconnections and of the tracks by separating the current carrying and voltage sensing electrodes. A driving pulse large enough to stabilize the electric waveforms but short enough to neglect the temperature rise has been implemented. Thus, their values at 25 °C including the resistances of the metal layers inside the chip are $R_{DSN} = 38$ m Ω and $R_{DSP} = 53$ m Ω , very close to the theoretical values obtained in the simulation ($R_{DSN} = 45$ m Ω and $R_{DSP} = 56$ m Ω).

Since there are two pads in parallel on the same potential, the four-terminal sensing method has also been performed to measure their resistances in the steady state

$$R_{DS} = \frac{V_{DROP}}{I_{dc}}. \quad (1)$$

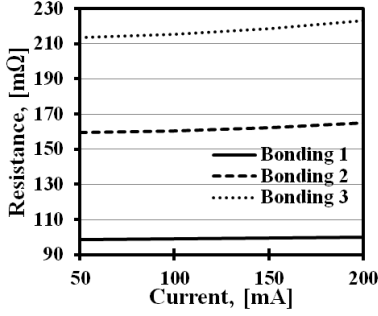


Fig. 7. Resistance of the bonding wires in package CQFP-44. Bonding 1: shortest wire. Bonding 2: medium wire. Bonding 3: longest wire.

The resistance of the bonding wires depends on their length and size. Bigger dies need bigger package, and as a consequence, the bonding wires are longer. Moreover, if the shape of the die is not square but rectangular, the bonding wires may have different lengths. Fig. 7 shows the experimental results of the measured resistance for different dc current rates. The longest bonding wire has 220-m Ω resistance and the shortest one has 100-m Ω resistance. As it can be observed, the resistance of the longest bonding wire increases with the current because of the heat due to the more generated losses.

We will consider the interconnect resistances R_{INTERCO} as a part of the die characteristics in order to evaluate their impact on its efficiency. Therefore, the total conduction losses P_{COND} of one inverter leg are given by (2), where I is the value of the current through one power inverter leg, $R_{\text{INTERCO(E)}}$ is the equivalent interconnect resistance, $P_{\text{COND(MOSFET)}}$ is the losses only in the transistors, and $P_{\text{COND(INTERCO)}}$ is the losses in the interconnect resistances

$$P_{\text{COND}} = \frac{1}{2} \cdot (R_{\text{DSP}} + R_{\text{DSN}} + R_{\text{INTERCO(E)}}) \cdot I^2$$

$$P_{\text{COND}} = P_{\text{COND(MOSFET)}} + P_{\text{COND(INTERCO)}} \quad (2)$$

Thus, in the nominal operating state of the die (5 V/10 \times 200 mA/1 MHz), the losses in the bonding wires in one inverter leg are estimated $P_{\text{COND(INTERCO)}} = 26$ mW and they are more than four times higher than the conduction losses of the power MOSFETs [$P_{\text{COND(MOSFET)}} = 8$ mW]. This gives in total conduction losses up to 340 mW which corresponds to 3.4% of the efficiency of the chip without considering the switching and driver losses. Moreover, this package is not able to evacuate the heat due to the losses. In this case, there is high risk to destroy the bonding wires and to make the assembly dysfunctional. To overcome this problem, the die has also been packaged in a more compact plastic package QFN-44 to reduce the length of the bonding wires and to take advantage of its thermal pad. However, the high density of fine pitch pads can cause short circuits between the bonding wires and make the circuits dysfunctional since the space in the package is limited. Fig. 8 shows an X-ray analysis of the packaged die in the package QFN-44. As it can be observed, the short circuits occur between some of the bonding wires. As a result, the 120 samples that have been packaged are dysfunctional.

Therefore, the flip-chip bonding is a solution to reduce the contact resistance between the chip pads and the PCB

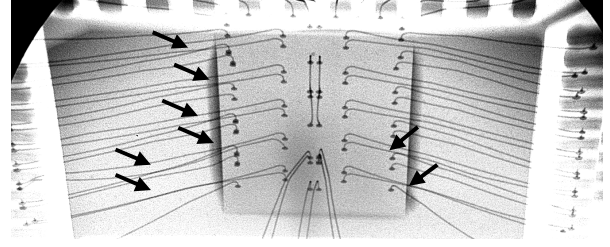


Fig. 8. X-rays image (45°) of the packaged die in package QFN-44. Arrows: short circuits between the bonding wires.

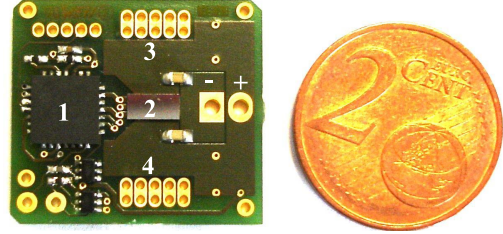


Fig. 9. Photo of the flip-chip assembly of the chip. 1: microcontroller. 2: chip. 3: outputs from 1 to 5. 4: outputs from 6 to 10.

substrate, to evacuate the power losses, to optimize the interconnections, and also to reduce the assembly cost.

III. OVERVIEW OF THE STUDIED FLIP-CHIP BONDING TECHNOLOGIES

At first, the studied flip-chip bonding techniques are presented and the experimental results are provided in Section IV. Fig. 9 shows a photo of the new test board on which the die is bonded to the PCB using different flip-chip bonding techniques. The microcontroller is placed on the board as well in order to decrease the parasites in the command signal.

This design allows more optimal routing of all the pads of the die and reducing of the total volume of the board, while maximizing the total surface of the copper planes in order to improve the heat removal capabilities of the assembly. The vias of the PCB under the die are used as a bridge between the two layers. A 110-K/W thermal resistance die-to-ambient in natural convection has been derived from an analytical model based on equivalent thermal circuit of the assembly. The total surface of the copper plane used for heat removal is 230 mm² as 140 mm² is on the top layer and 90 mm² is on the bottom layer of the PCB with 35- μ m copper thickness. The total surface of the substrate is 400 mm² (20 mm \times 20 mm), including the microcontroller, its periphery components, and the connectors.

A. Anisotropic Conductive Adhesive

The anisotropic conductive adhesive (ACA) is not electrically conducting itself, but it is filled with conducting particles that create the contact between the chip pads and the tracks on the substrate. The adhesive can be a film material or a paste [21]. In this paper, an adhesive film has been used and the golden stud bumps with 70- μ m diameter have been placed on the pads of the chip in order to create the joints.

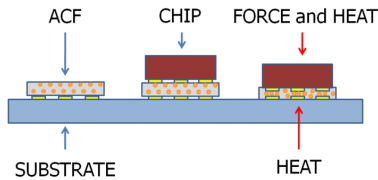


Fig. 10. Flip-chip bonding with an adhesive film [21].

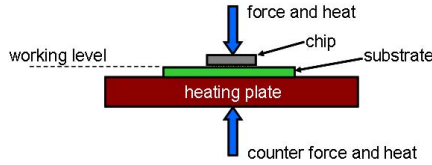


Fig. 11. Thermocompression flip-chip bonding [21].

As shown in Fig. 10, at first, the adhesive film is placed on the substrate where the chip has to be mounted. Then, the chip is aligned and glued. In order to create the contacts, a force is introduced and a temperature is applied to cure the material. This process is simple, low cost, and the low cure temperature does not damage the physical properties of the PCB substrate [15].

B. Thermocompression Flip-Chip Bonding

To create a flip-chip assembly with thermocompression, the golden stud bumps with 70- μm diameter have been planted on the chip pads to create the joints. The assembly has been placed on a heating plate in order to preheat the substrate up to 200 °C. Then, a thermal cycle has been defined so that the temperature of the chip reaches up to 350 °C and an external force is applied to weld the joints, both the parameters depending on the chip size and the number of pads (Fig. 11). Typically, the force is 0.1–0.7 N/bump [21].

One drawback of this technology is the high peak temperature of the thermal cycle. The standard PCB substrate built with FR4 material can be deformed at temperatures more than 200 °C [22]. Another weakness can be considered that the placement of components on the bottom layer of the substrate is not allowed before the bonding process in order to ensure good flatness and uniform heating from the heating plate. This could be a problem for more complex circuits where the number of components is increased and the surface of the board has to be minimized. Nevertheless, the components on the bottom layer could be mounted after the flip-chip bonding, but in this case, the assembly will be exposed to another thermal cycle.

C. Ultrasonic/Thermosonic Flip-Chip Bonding

The ultrasonic/thermosonic flip-chip bonding is similar to the thermocompression flip-chip bonding (Fig. 11) but the assembly and the substrate do not suffer from high peak temperature. First, the substrate has been preheated at 120 °C temperature. Then, a force (0.06 N/bump) has been introduced to the die and an ultrasonic burst (1400 mW) was triggered while reaching the peak temperature (150 °C) of the thermal cycle. Therefore, the contacts between the chip bumps and the

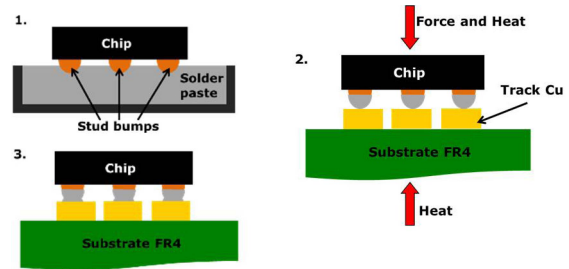


Fig. 12. Custom solder bonding.

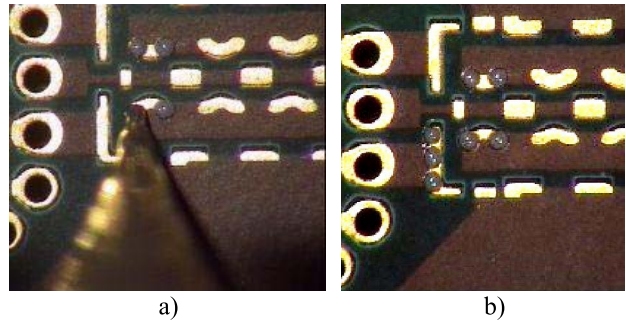


Fig. 13. Photograph of the dispense process on the PCB side. (a) Injection of a solder paste into the solder mask openings. (b) Result after the injection of a solder paste.

PCB tracks are created by friction welding. A special care has to be taken in what refers to the parameters of the bonding process. On one hand, the high force and ultrasonic power can break the joints when the ultrasonic burst is triggered. On the other hand, the low force and ultrasonic power may not weld the joints.

A FINEPLACER flip-chip bonder is used for the realization of the assembly. Its high alignment precision makes it more appropriate for the dies with increased number of pads. A pyramid tool that allows the energy transfer from the two sides of the chip has been used since the flat ultrasonic tool, where the chip is fixed by vacuum only limits the power transfer into the chip during the process.

D. Custom Stud Bump Solder Flip-Chip Bonding

The custom flip-chip bonding technique has been tested in order to mount the dies on the PCB with the same FINEPLACER flip-chip bonder. At first, the gold stud bumping process has been performed in order to make the chip pads wettable and to give them some height. Then, the bumps are tip into a solder paste material SnPb63/37 and the chip is aligned to the PCB substrate. Afterward, a thermal cycle was defined so that the paste welds and creates the joints between the stud bumps and the PCB tracks (Fig. 12).

First, the experimental results showed that the mechanical strength of the prototypes was not good. The chip was removed very easily because of the small quantity of the solder paste since it is glued naturally on the stud bumps. As shown in Fig. 13, a dispense process has been done directly on the PCB to get more solder under the stud bumps in order to enhance the mechanical strength of the assembly.

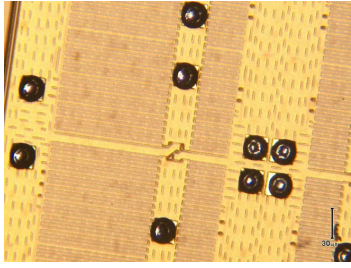


Fig. 14. Solder bumps on the pads of the CMOS circuit.

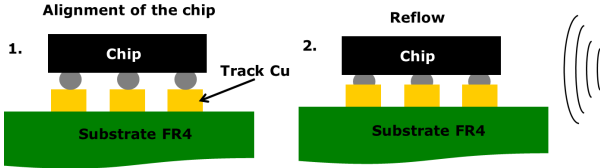


Fig. 15. Solder bonding flip-chip assembly.

E. Solder Flip-Chip Bonding

The solder flip-chip bonding technology deals with the soldering of bumps composed of different alloys, such as SnPb, SnAgCu, SnAg, and SnCu, directly on the chip pads [23], [24]. Fig. 14 shows an image of solder bumps of SnAgCu alloy with 90- μm diameter soldered on the chip pads. The chip is then aligned to the PCB substrate and the joints are built by welding the bumps after the reflow process (Fig. 15). This technology allows mounting of components on the top and bottom layers of the substrate before the flip-chip bonding process and no mechanical stress is required.

IV. EXPERIMENTAL RESULTS AND DISCUSSION

The experimental results with an ACA and the thermocompression bonding did not correspond to what we expected. During the tests, only the consumption of the microcontroller has been measured and no output signals have been detected. The reason is that the joints on the command pads have not been created because the consumptions of the driver circuits of the inverter legs have not been measured. Moreover, the voltage drop of the body diodes of the power MOSFETs has not been measured (Fig. 6). Therefore, we can conclude that the joints between the pads V_{DD} , GND, and the output of the die and the tracks on the PCB are not realized. Seven samples with no result of each bonding technique were sufficient to conclude that these two flip-chip technologies are not adapted to the design specifications of this die.

The ultrasonic/thermosonic bonding allowed us to partially characterize the assembly since the joints of only one inverter leg have been created with success after ten attempts with different configurations of the bonding process. The measured interconnect resistances $R_{INTERCO}$ have been highly reduced to the values between 25 and 27 $\text{m}\Omega$ and they do not vary with at different dc current rates up to 200 mA. If all the joints have been created, the losses in the bumps per inverter leg would be roughly reduced eight times [$P_{COND(INTERCO)} = 3.2 \text{ mW}$ for 5 V/200 mA] compared with the assembly with bonding wires. This result is close to what we expect in terms of interconnect resistance, but in terms of reliability, it is not satisfactory. While a force was applied on the side of

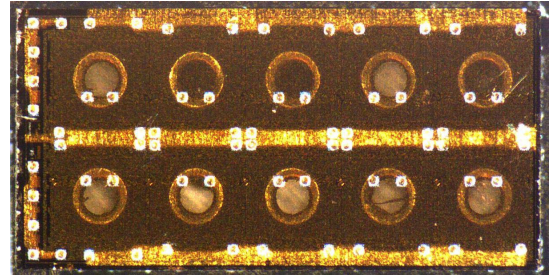


Fig. 16. Photograph of the chip with stud bumps aligned to the PCB.

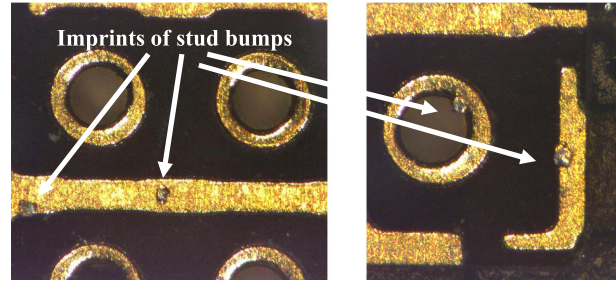


Fig. 17. Photographs after shearing.

the chip where the command pads are placed (Fig. 16, pads on the left side of the chip), the output signals of three more inverter legs were detected. Therefore, we can conclude that not all the joints of the pads are uniformly created or some of them are missing.

A shear test has been carried out in order to check the mechanical strength of the assembly. Fig. 16 represents top view of the chip aligned to the board before shearing and Fig. 17 shows some imprints of the stud bumps on the tracks of the PCB after shearing. It is important to note that no underfill has been used for this assembly. As it can be observed, many joints are not at all created because not all imprints of the stud bumps are left on the PCB tracks.

Therefore, we can conclude that the ultrasonic flip-chip bonding could be a good solution for the flip-chip assembly of dies with smaller number of pads and simpler substrate patterning. In the case of the proposed power die, much more energy is needed to uniformly create the joints between all the stud bumps and the tracks on the PCB.

Twelve assemblies have been realized with the custom stud bump solder bonding. In the best case, all the joints between their stud bumps and the PCB tracks of maximum seven inverter legs were created and they were operational. The values of the interconnect resistances were homogenous and they are reduced to between 10 and 13 $\text{m}\Omega$ but further characterization of the assembly would be not representative since not all joints are created. However, this technique is more efficient, shows stable results regarding the interconnect resistances and offers better contact between the chip and the PCB compared with the technologies presented above. The losses in the interconnections per inverter leg are estimated $P_{COND(INTERCO)} = 1.6 \text{ mW}$ for 5 V/200 mA which could increase the total efficiency of the chip with roughly 4% in comparison with the assembly with bonding wires.

The solder flip-chip bonding allowed us to solder all 70 pads. The interconnect resistances for each inverter leg

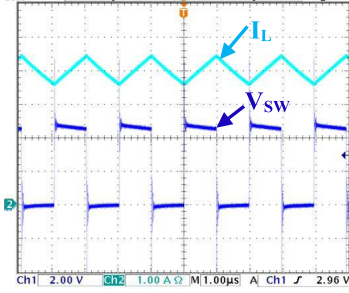


Fig. 18. Current in the inductor and voltage at the switching node of the inverter legs.

TABLE II
LOSSES OF THE POWER CMOS DIE AT $V_{IN} = 5$ V,
 $f_{sw} = 500$ kHz, $\alpha = 0.5$, AND $I_{OUT} = 4$ A

Conduction losses, [mW]	Switching losses, [mW]	Gate driver losses, [mW]	Total losses, [mW]
120	20	80	220

of 15 realized trials are homogenous and their values vary between 1.8 and 3.1 m Ω . Therefore, their losses have been reduced roughly 70 times (0.37 mW for 5 V/200 mA) compared with the wire bonding technology and as a consequence they can be neglected. Afterward, the die has been implemented in a standard buck converter in order to characterize the thermal and the electric constraints of the assembly. The outputs of all inverter legs have been connected in parallel and the converter has been tested under the following conditions: 1) supply voltage $V_{IN} = 5$ V; 2) switching frequency $f_{sw} = 500$ kHz; 3) duty cycle $\alpha = 0.5$; 4) resistive load $R = 0.625$ Ω ; and 5) output load current $I_{OUT} = 4$ A. Fig. 18 shows the current in the inductor I_L and the voltage waveform at the switching node of the inverter legs V_{SW} . The measured signals correspond to what we expected, the functionality of the structure has been validated and no distortion has been observed.

The measured total losses of the CMOS die are 220 mW and Table II summarizes the loss breakdown. Fig. 19 shows a thermal image of the assembly under the same operation conditions in natural convection. As it can be observed, the ambient temperature is ~ 22 $^{\circ}\text{C}$ and the maximal temperature is ~ 45 $^{\circ}\text{C}$. The temperature rise at steady state is ~ 23 $^{\circ}\text{C}$. Therefore, the extracted thermal resistance die-to-ambient is 104 K/W. This result corresponds to what we expect in the analytical estimation. Since the conducting losses are at the same level as the losses due to the switching frequency (switching losses and gate driver losses from Table II), it is possible to increase the output current or the switching frequency up to 1 MHz without reaching its maximal operating temperature 125 $^{\circ}\text{C}$ [20]. Moreover, the heat is well evacuated from the copper surfaces on the PCB. This means that the losses in the assembly are not prominent, the quality of the joints is good, and they are able to drain the heat through the bumps.

Table III summarizes the results obtained with the studied flip-chip bonding techniques. The data are given per inverter

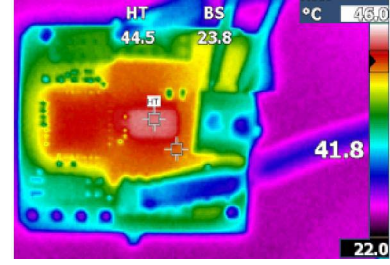


Fig. 19. Thermal picture in natural convection of the assembly.

TABLE III
COMPARISON OF THE INTERCONNECT RESISTANCES OBTAINED WITH
THE STUDIED FLIP-CHIP BONDING TECHNIQUES

Bonding technique	Created joints	$R_{INTERCO(MIN)}$ [m Ω]	$R_{INTERCO(MAX)}$ [m Ω]	$P_{COND(INTERCO)}$ [mW]	Nb of samples
Wire-bonding CQFP-44	58	100	220	26	5
ACA	0	-	-	-	7
Thermo-compression	0	-	-	-	7
Ultrasonic/thermosonic	10	25	27	3.2	10
Custom stud bump solder	50	10	13	1.6	12
Solder flip chip	70	1.8	3.1	0.37	15

leg at 5 V/200 mA (1 W) which is its nominal operating condition.

The solder bonding technique gives best results regarding the values of the interconnect resistances which are directly related to the conduction losses of the CMOS circuits. The homogenous results obtained with 15 samples are representative for the reliability of this technology, which is cost effective for solder bumping on wafer level.

V. CONCLUSION

In this paper, a study of commercial techniques for flip-chip bonding is presented. A CMOS circuit for low-power microconverters is designed and used as a basis for comparison. The chip contains ten power inverter legs and is built for 10-W maximal switching power (5 V/2 A/1 MHz). It is shown that the flip-chip bonding offers high reduction of the contact resistances and good thermal management of the chip. The 70 pads are needed for the command and for the decreasing of the bump resistances and the electrical constraints of the inverter legs. Thus, the flip-chip of the die is more difficult.

The anisotropic adhesive bonding and the thermocompression bonding are not appropriate for the presented application considering FR4 substrates. Poor quality joints between the chip pads and the tracks on the PCB have been created. The ultrasonic/thermosonic bonding gave a partial result, allowing the characterization of the interconnect resistances of only one inverter leg. More energy is needed in order to create the joints between all 70 pads of the chip and the PCB tracks. Therefore, an alternative approach based on the soldering of the stud bumps by dispense of solder paste on the PCB copper tracks is proposed. The result is the uniform bump resistance of all operational inverter legs. The results obtained with the solder flip-chip bonding technology correspond to what we expect in

terms of electrical, thermal, and mechanical constraints. This technique is cost attractive on wafer level and seems to be most appropriate for mass fabrication of highly integrated CMOS-based power converters.

ACKNOWLEDGMENT

The authors would like to thank G. Kuerbis and C. Daedlow from Finetech GmbH & Co. KG for their cooperation.

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