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Design of a 77 GHz *LC*-VCO with a Slow-wave Coplanar Stripline-Based Inductor

E. Sharma, A. A. Saadi, M. Margalef-Rovira, E. Pistono, M. J. Barragan, A. A. Lisboa De Souza, P. Ferrari, S. Bourdel

Abstract—The objective of this paper is to demonstrate that the use of a distributed approach for the design of the inductance of an *LC*-tank mm-wave VCO can lead to higher performance. Performance is improved in both frequency tuning range and power consumption, thanks to a reduction of the cross-coupled pair size. The direct comparison of VCOs designed in different technologies is not easy, and not fair either, since the performance of the varactors and the inductance widely differ for different fabrication technologies. Hence, two VCOs were designed and integrated in the same CMOS 55-nm technology by using the same varactors. Thus, a “classical” VCO using an inductor available in the technology and serving as reference, and a distributed-inductance based VCO using a slow-wave transmission line were considered. A detailed and efficient approach is adopted for the synthesis of slow-wave transmission line based inductance without using time consuming EM simulations. The slow-wave VCO permits to limit the overall size linked to a distributed approach, while improving the electrical performance. Experimental results on proof-of-concept demonstrators at a working frequency of 77 GHz allow validating our proposal.

Index Terms— CMOS, *LC*-VCO, S-CPS, Slow-Wave, millimeter-wave.

I. INTRODUCTION

THE development of consumer applications such as 5G or automotive radars requires the use of silicon technologies since they are less expensive and facilitate integration. In these technologies, the realization of high performance circuits at millimeter-wave (mm-wave) frequencies is a major challenge. In the case of Voltage-Controlled-Oscillators (VCOs), the

high losses of the passive devices available in silicon technologies reduce performance in terms of phase noise due to resonator's reduced quality factor as well as power consumption and Frequency Tuning Range (FTR) since larger MOS transistors are generally required for obtaining a higher transconductance to compensate losses. Varactors required in most VCO topologies to vary the oscillation frequency have a very low quality factor in particular for high frequencies and hence, constitute the most critical device limiting the VCO performance [1].

At mm-wave frequencies, VCOs are generally based either on a *LC*-resonator tank (*LC*-VCO) or on a Standing-Wave-Oscillator (SWO) topology. In the former, the resonator is made by lumped elements while in the latter, it is achieved by a quarter-wave length transmission line (TLine) loaded with varactors. A Cross Coupled Pair (CCP) is used to cancel resonator losses and thus ensures the sustained oscillations. Whatever the considered topology, high losses in the resonator generally imply a large CCP. Hence, in addition to high power consumption, a large CCP generates high parasitic capacitances, leading to a reduced FTR. Thus, the main issue of VCO optimization concerns the resonator losses and hence, improving its *Q*-factor is one of the main challenges.

At frequencies close to 80 GHz, the *LC*-VCO is a quite common topology [2]. This structure is popular due to a simple design that does not require intensive EM simulations, since the lumped inductors provided in the design kits associated to a given technology are accurate and generally modeled based on measurements. Unfortunately, the passive components available in the standard design kits offer a limited performance at mm-wave frequencies.

To improve the quality factor of the resonator, SWOs have been proposed by substituting the inductance by a quarter-wave length TLine [3]. To go further and reduce the effect of the CCP parasitic capacitances, these CCP can also be distributed all along the TLine [4],[5].

In [6],[7], the *LC*-VCO topology was considered by synthesizing the inductance with a TLine. Several types of TLines can be investigated and optimized according to the Back End Of Line (BEOL) and the operating frequency [8]. These topologies are quite similar to SWO since the resonator is formed by a TLine loaded by a varactor. However, the sizing method can differ. Indeed, in a SWO, the TLine is sized to have an electrical length of $\lambda/4$ when it is loaded by the varactor whereas, in the custom inductance based *LC*-VCO,

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the TLine is sized to achieve a given inductance when it is shorted at one end.

In a general manner, the main drawback related to VCOs based on standing waves or synthesized inductances is the need for intensive EM simulations to design the resonator. In addition, the optimization process is quite long due to the interactions between the characteristics of the TLine obtained by EM simulations, and the CCP parasitic capacitances extracted from electrical simulations.

In this paper, the design of an LC -VCO is presented. To improve the Q -factor of the LC tank, the inductance is synthesized with a Slow-wave (SW) Coplanar Stripline (S-CPS) [9]. The sizing of the S-CPS-based inductance is achieved with the electrical model proposed in [10]. Based on this model, the optimum layers of the BEOL and the optimum dimensions of the S-CPS are obtained without the need of computationally intensive EM simulations. Moreover, theoretical background for the calculus of the equivalent inductance is presented, allowing a better understanding of the interest of the slow-wave concept and the trade-off between size and performance. Indeed, the presented theoretical study enabled to figure out the advantage of slow-wave concept and explain well the relationship between the lumped inductance and the distributed one, in the particular application of LC-VCO design. In addition, the presented approach of S-CPS based inductance synthesis reveals excellent accuracy and fast design. To validate the method and the performance of the S-CPS-based inductance, the proposed VCO is compared with a classical LC -VCO designed with a lumped inductance from the design kit of used technology. To this end, the same varactors and inductor value are used in both designs in order to observe the benefit of the S-CPS based inductor on the VCO performances. Furthermore, we adopted in each case the CCP size which ensures the same extra gain margin for oscillation start up, as will be explained.

This paper is organized as follows. Section II presents the operation principle of the proposed VCO and details a method for sizing the resonator and the CCP. In section III, the theoretical background to derive the equivalent inductance and Q -factor of a short-circuited SW transmission line is detailed. This derivation (i) gives the basic equations for the calculus of the equivalent inductance, and (ii) shows how the slow-wave concept allows increasing this inductance for a given physical length. Next, the inductance design is described and a special focus is done on the choice of the BEOL layers. In section IV, the implementation of both VCOs is presented as well as the measurement results. Finally, the conclusions and prospects are drawn in the last section.

II. VCO PRINCIPLE

The design principle of the proposed VCO is given in Fig. 1[11]. The LC resonator is formed by two varactors and an inductor synthesized by a S-CPS shorted at one end. Transistors M_1 - M_2 form the CCP and M_3 - M_4 with TLine stubs constitute the output buffers providing a $50\text{-}\Omega$ output for measurement purposes, respectively.

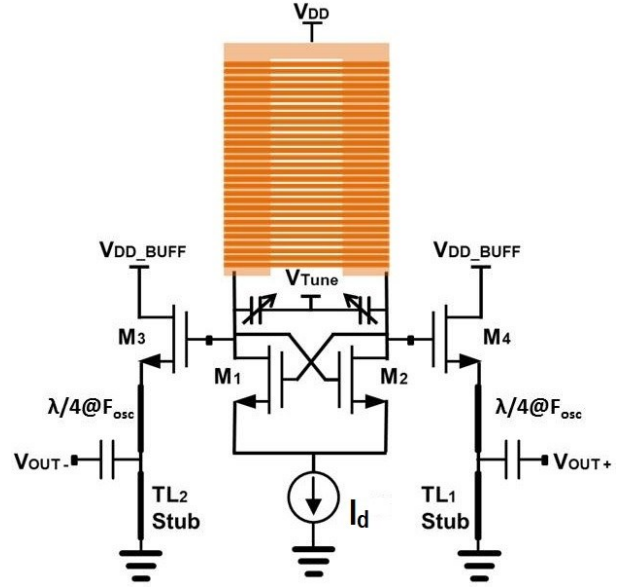


Fig. 1. VCO Principle.

A. CCP and Buffer Sizing

The CCP compensates the resistive losses of the resonator as well as the interconnection losses by presenting a negative resistance (R_{neg}) to the resonator's terminals. The well-known following criterion must be satisfied for sustained oscillations,

$$|R_{neg}| = R_p/K \leq 2/g_m \quad (1)$$

, where R_p is the equivalent parallel resistance seen at the resonator's terminals at the operating frequency, K is the loss compensation (excess) factor theoretically equal to 1, it is also defined as the necessary safe margin to ensure oscillation start up; and g_m is the transconductance of M_1 and M_2 , respectively. g_m depends on the MOS size (W/L) and the bias current (I_d) as follows:

$$g_m = \sqrt{2 K_n \frac{W}{L} I_d} \quad (2)$$

where K_n is a constant that depends on the electron mobility and the oxide capacitance. As presented in Fig. 2, small absolute values of the negative resistance needed to compensate for high loss can be obtained with large MOS transistors and/or a large bias current. Large MOS transistors cause large parasitic capacitances whereas a large bias current increases the power consumption. Thus, the sizing of the CCP is a trade-off between the power consumption requirements and the added parasitic capacitances. The smallest CCP might be chosen (for a given power consumption) to maximize the FTR. A parametric simulation of the CCP, as the one given in Fig. 2, was carried out to investigate the range of negative resistances and their associated parasitic capacitances. For the PDK used in this work, it is possible to synthesize negative resistance from $-600\ \Omega$ to $-150\ \Omega$ for W and I_d varying from $10\ \mu\text{m}$ to $20\ \mu\text{m}$, and $1\ \text{mA}$ to $12\ \text{mA}$, respectively, as shown in Fig. 2(a). Resulting parasitic capacitances range from $14\ \text{fF}$ to $28\ \text{fF}$ (Fig. 2(b)).

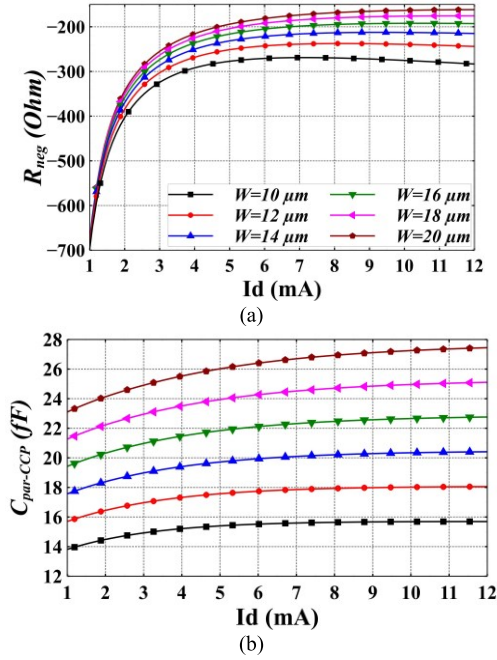


Fig. 2. (a) Negative resistance (R_{neg}), (b) Parasitic capacitance ($C_{par-CCP}$) for different CCP sizes.

Based on M_3 and M_4 , the output buffers are based on source follower amplifiers having a real part of the output impedance equal to 50Ω :

$$R(Z_{out}) = \frac{1}{g_m} = 50 \Omega \quad (3)$$

The stubs (TL_1 and TL_2) are tuned to cancel the imaginary part of the output impedance. The output impedance of the VCO slightly varies with the CCP size and a 7-fF parasitic capacitance (associated to the buffer) can be estimated by electrical stimulation based on the PDK.

B. Resonator Sizing

The resonator is sized to achieve the required oscillation frequency F_{osc} as follows:

$$F_{osc} = 1/(2\pi\sqrt{L_{ind} \cdot C_p}), \quad (4)$$

with L_{ind} the inductance value of the tank and C_p the total capacitance seen from the inductance. C_p is equal to the capacitance of the varactor C_{var} in parallel with the parasitic capacitance $C_{par-tot}$ given by the CPP and the buffers, ($C_{par-CCP}$ and $C_{par-buffer}$):

$$C_p = C_{var} + C_{par-tot}. \quad (5)$$

As presented in Section II-A, the parasitic capacitance $C_{par-tot}$ can be estimated based on parametric electrical stimulation.

If a continuous FTR is required, a varactor must be considered at the expense of a larger tuning range that could be obtained with switched capacitors for instance. The choice of the varactor is a trade-off between the FTR and the Q -factor. Large varactors lead to high FTR but low Q -factors involving larger CCP transistors and higher power consumption. In this work, the power consumption minimization was studied. Hence the considered varactor exhibits the highest Q -factor in the technology. It was chosen on the basis of electrical

simulations with the PDK. As presented in Fig. 3, the capacitance range is [4.4 fF – 9 fF] and the Q -factor varies from 10 to 15 at 80 GHz.

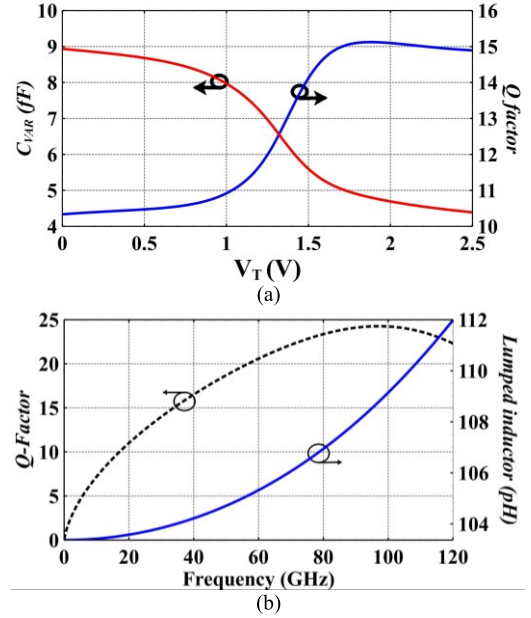


Fig. 3. (a) Simulation of the varactor from the PDK, at 80 GHz. (b) Simulation of lumped inductor from the PDK.

Knowing the value of $C_{var} = [4.4 - 9]fF$ and the values of $C_{par-tot}$ and L are obtained with PDK based electrical simulations of the LC-VCO which is our reference design. The obtained values of L , $C_{par-CCP}$ and $C_{par-tot}$ are 107 pH, 24fF and 31fF respectively which give a theoretical tuning range calculated with (4) from 77 GHz to 82 GHz. Fig. 3(b) illustrates the simulated performance of the used inductor from the PDK associated to the technology involved in the VCO design.

III. S-CPS SYNTHESIZED DIFFERENTIAL INDUCTOR

A. Theoretical background

The equivalence between a shorted TLine, which is a distributed device, and an inductance is quite straightforward, even if this was not clearly explained in a dedicated paper, to the best of authors knowledge. The concept was already used in some papers such as [12]. The main drawback of this approach is linked to the overall size of the TLine, which can be prohibitive, given the price of mm^2 in advanced CMOS and BiCMOS technologies. A solution to reduce the TLine size consists in using SW TLines, namely S-CPS (for SW Coplanar Stripline) [13]. A second advantage of using S-CPS is the Q -factor that is much higher as compared to the use of classical Tlines such as microstrip lines, as will be shown in this section.

First, the basic theory is presented, considering a TLine defined by its characteristic impedance Z_c , and its attenuation constant (α) and phase constant (β), respectively. Next, the comparison between S-CPS and classical Tlines is carried out to definitely show the interest in using S-CPS.

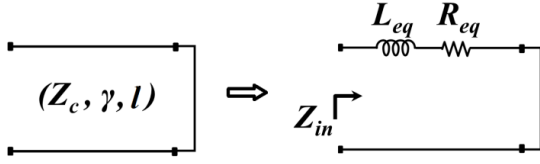


Fig. 4. Equivalent lumped inductance synthesized with short-circuited TLine.

Fig. 4 gives the schematic of the shorted TLine and its equivalent lumped model with an inductance L_{eq} in series with a resistance R_{eq} , Z_{in} being the input impedance.

From the $ABCD$ matrix of the short-circuited TLine, Z_{in} can be expressed as:

$$Z_{in} = \frac{B}{D} = Z_c \cdot \tanh(\gamma l), \quad (6)$$

with $\gamma = \alpha + j\beta$, and l the transmission line physical length.

Let first consider the lossless case, i.e. $\gamma = j\beta$, in order to show how the slow-wave concept allows increasing the equivalent inductance L_{eq} . In that case, Z_{in} can be written as:

$$Z_{in} = jZ_c \cdot \tan(\beta l). \quad (7)$$

The equivalent inductance can be derived as:

$$Z_{in} = jL_{eq}\omega = jZ_c \cdot \tan(\beta l), \quad (8)$$

thus, leading to the well-known equivalence:

$$L_{eq} = \frac{Z_c \tan(\beta l)}{\omega}. \quad (9)$$

Note that the shorted Tline can be only equivalent to an inductance when βl is lower than $\pi/2$ (modulo π).

By restricting βl to a value much lower than unity (i.e. a physical length much lower than the guided wavelength λ_g), a first order Taylor series development leads to the quasi-static (QS) expression of L_{eq} :

$$L_{eq-QS} = \frac{Z_c \beta \cdot l}{\omega} = \frac{Z_c \sqrt{\epsilon_{reff}}}{c_0} l, \quad (10)$$

with c_0 the light velocity in vacuum, and ϵ_{reff} is the relative permittivity of the media. If the transmission line LC distributed electrical model is considered, it can be written as:

$$L_{eq-QS} = \frac{Z_c \beta \cdot l}{\omega} = \sqrt{\frac{L}{C}} \cdot \frac{\omega \sqrt{L \cdot C} \cdot l}{\omega} = L \cdot l. \quad (11)$$

Equation (11) means that the equivalent inductance is equal to the linear inductance multiplied by the physical length when the latter is much lower than λ_g .

Based on (9) and (11), the equivalent inductances (L_{eq}) and its quasi-static value (L_{eq-QS}) can be plotted versus βl (or similarly versus f). Fig. 5 shows an example of a typical case with two TLines, a classical one and a SW one. For a fair comparison, these two TLines have the same characteristic impedance $Z_c = 50 \Omega$ and physical length $l = 100 \mu\text{m}$. They differ in terms of effective dielectric constant ϵ_{reff} . The effective dielectric constant of the classical TLine was chosen equal to $\epsilon_{reff-classical} = 4$, whereas it was chosen equal to $\epsilon_{reff-SW} = 9$ for the SW TLine, respectively. These two values of effective dielectric constant correspond to typical cases. For instance, a microstrip line will be considered later in section III.B for the practical comparison with S-CPS.

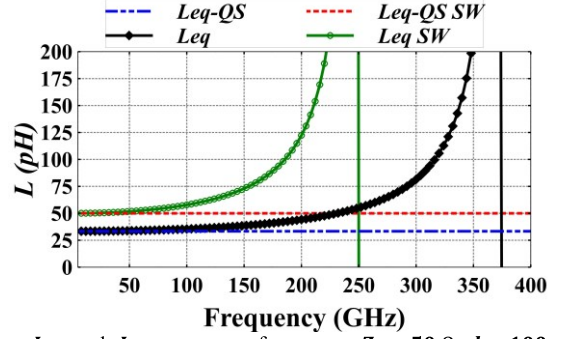


Fig. 5. L_{eq} and L_{eq-QS} versus frequency. $Z_c = 50 \Omega$, $l = 100 \mu\text{m}$, $\epsilon_{reff} = 4$ and $\epsilon_{reff-SW} = 9$.

When βl is much lower than unity, i.e. for low frequency, L_{eq} is equal to L_{eq-QS} . When βl increases (i.e. either the frequency or the physical length increases), L_{eq} increases and differs from the quasi-static case, as shown in Fig. 5. When $\beta l = \frac{\pi}{2}$, an infinite value of L_{eq} is obtained due to the tangent function behaviour. This corresponds to a frequency of 362 GHz for the classical TLine, and 250 GHz for its SW counterpart, respectively.

L_{eq-QS} is interesting to be considered for comparison purposes. For the classical TLine and its SW counterpart, $L_{eq-QS} = 33.3 \text{ pH}$ and $L_{eq-QS}^{SW} = 50 \text{ pH}$, respectively. The ratio $\eta_{QS} = \frac{50}{33.3} = 1.5$ corresponds to the slow-wave factor SWF:

$$SWF = \sqrt{\frac{\epsilon_{reff-SW}}{\epsilon_{reff-classical}}}. \quad (12)$$

Hence, SW transmission lines allow the physical length reduction to achieve the same equivalent inductance as compared to its classical TLine counterpart. This phenomenon is magnified by the increase of L_{eq} with the frequency. Indeed, as shown in Fig. 5, for a working frequency equal to 80 GHz, $L_{eq} = 34.6 \text{ pH}$ for the classical TLine, and $L_{eq-SW} = 54.7 \text{ pH}$ for its SW counterpart, respectively. This leads to a ratio $\eta = 1.58 > \eta_{QS}$.

Let's now consider a lossy TLine in order to derive the quality factor of the equivalent inductance L_{eq} . As already stated, in that case, the shorted TLine is modelled as a lumped model composed of L_{eq} in series with R_{eq} . The equivalent quality factor Q_{eq} is given by:

$$Q_{eq} = \frac{L_{eq} \omega}{R_{eq}}, \quad (13)$$

and $\tanh(\gamma l)$ can be expressed as:

$$\tanh(\gamma l) = \frac{\tanh(\alpha l) [1 + (\tanh(\beta l))^2]}{1 + [\tanh(\alpha l) \tanh(\beta l)]^2} + j \frac{\tanh(\beta l) [1 - (\tanh(\alpha l))^2]}{1 + [\tanh(\alpha l) \tanh(\beta l)]^2} \quad (14)$$

Hence, Q_{eq} can finally be written as:

$$Q_{eq} = \frac{\tan(\beta l) \cdot [1 - (\tanh(\alpha l))^2]}{\tanh(\alpha l) \cdot [1 + (\tan(\beta l))^2]} = \frac{\tan(\beta l)}{\tanh(\alpha l)} \cdot \frac{1 - (\tanh(\alpha l))^2}{1 + (\tan(\beta l))^2}. \quad (15)$$

Same cases for Z_c , physical length l and dielectric constants $\epsilon_{reff-classical}$ and $\epsilon_{reff-SW}$ as for the calculus of L_{eq} in the lossless case were considered. The attenuation constant was modelled by:

$$\alpha = \alpha_{DC} + \alpha_f \sqrt{f/f_0}, \quad (16)$$

with typical values $\alpha_{DC} = 0.2$ dB/mm, $\alpha_f = 0.4$ dB/mm, and $f_0 = 60$ GHz. This model corresponds to an attenuation constant equal to 0.6 dB/mm at 60 GHz, which is close to state-of-the-art TLines in CMOS BEOLs. Q_{eq} is plotted in Fig. 6 for both cases, i.e. classical TLine and SW TLine.

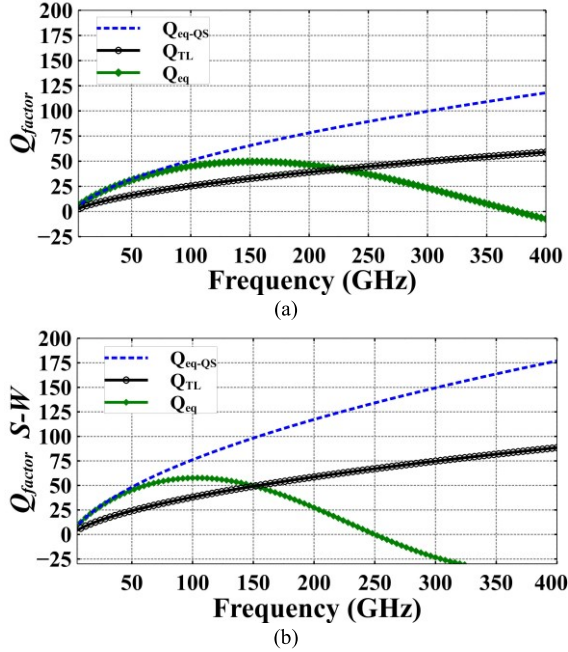


Fig. 6. Q -factor versus frequency for $Z_c = 50 \Omega$, $l = 100 \mu\text{m}$, (a) $\epsilon_{reff-classical} = 4$ and (b) $\epsilon_{reff-SW} = 9$.

When considering low-loss TLines, the quasi-static Q -factor (at low frequency) of the equivalent inductance can be derived from (15). It gives the limit of the maximum Q -factor that can be achieved. From (15) and for $\alpha l \ll 1$ and $\ll 1$, $Q_{eq-QS} = \frac{\beta}{\alpha}$ is easily derived. It was also plotted in Fig. 6 for comparison. Note that it is twice the well-known Q -factor of a TLine $Q_{TL} = \frac{1}{2} \frac{\beta}{\alpha}$.

Q_{eq} follows Q_{eq-QS} up to a frequency that is roughly equal to 20% of the resonance frequency of the shorted TLine (e.g. when its electrical length is equal to 90°). The maximum Q_{eq} is obtained at a lower frequency for the SW TLine, i.e. 104 GHz as compared to 152 GHz for its classical TLine counterpart, respectively. Moreover, the maximum Q_{eq} is greater for the SW TLine, i.e. 57.7 as compared to 49.6, respectively.

In conclusion, SW TLines lead to, (i) shorter short-circuited stubs for the realization of equivalent inductances, and (ii) higher quality factors, as compared to classical TLines.

In section III.B, practical TLines are considered for the design of the inductance in a standard BEOL, namely, microstrip lines, CPS and S-CPS. Finally, in section III.C, the design of the S-CPS that was used in the VCO considered in this paper is described.

B. Comparison of S-CPS, CPS and microstrip lines for synthesized inductances

In order to show the usefulness of the S-CPS topology to achieve efficient equivalent inductances, both in terms of performance and area consumption, equivalent inductances were also derived from CPS and microstrip lines topologies by performing EM simulations. The electrical performance achieved by each topology is plotted in Fig. 7. The physical dimensions of S-CPS and CPS strips and gap width are exactly the same ($W_s = 10 \mu\text{m}$, $G = 30 \mu\text{m}$ and the shield in the S-CPS is located at $2 \mu\text{m}$ height from the strip). They lead to a characteristic impedance equal to $Z_{c-S-CPS} = 76 \Omega$ and $Z_{c-CPS} = 129 \Omega$, respectively. A characteristic impedance equal to that of the S-CPS, i.e. $Z_{c-microstrip} = 76 \Omega$, was retained for the microstrip line, leading to a strip width equal to $1.7 \mu\text{m}$. Same physical length of $100 \mu\text{m}$ was considered for the three structures.

A similar behaviour is found between the results obtained theoretically in Section III.A and the results obtained from EM simulations. The equivalent inductances are shown in Fig. 7 (a) for the three kinds of studied TLines (S-CPS, CPS and microstrip). The shape of the equivalent inductance is similar to those shown in Fig. 5, L_{eq} increasing with frequency, in particular for the S-CPS. Concerning the microstrip line, the increase of L_{eq} with frequency is lower since its relative dielectric constant is much lower. It can also be seen that L_{eq} increases at very low frequencies. This behaviour is due to the losses and was not observed in Fig. 5 since the losses were neglected for the theoretical analysis.

The Q -factor of the TLine (Q_{TL}) and that associated to its equivalent lumped inductance (Q_{eq}), are given in Fig. 6 Fig. 7(b) and (c), respectively. As expected, Q_{eq} is higher than Q_{TL} up to a frequency depending on the effective dielectric constant ϵ_{reff} . The Q -factor reached by the S-CPS is the highest among the three TLines, with a value of 60 from 70 GHz to 80 GHz. Furthermore, the advantage of the S-CPS based equivalent inductance against its microstrip counterpart is well highlighted. Since, higher L_{eq} is achieved for the same length ($100 \mu\text{m}$), thus the length can be reduced for the same targeted inductance. For instance, at $f = 30$ GHz $L_{eq-S-CPS} = 94$ pH, $L_{eq-microstrip} = 51$ pH, and the ratio $\eta_{MS} = 94/51 = 1.84$ is obtained, which is in agreement with the slow-wave factor defined in (12). These results confirm the results obtained in the theoretical background presented in the previous section.

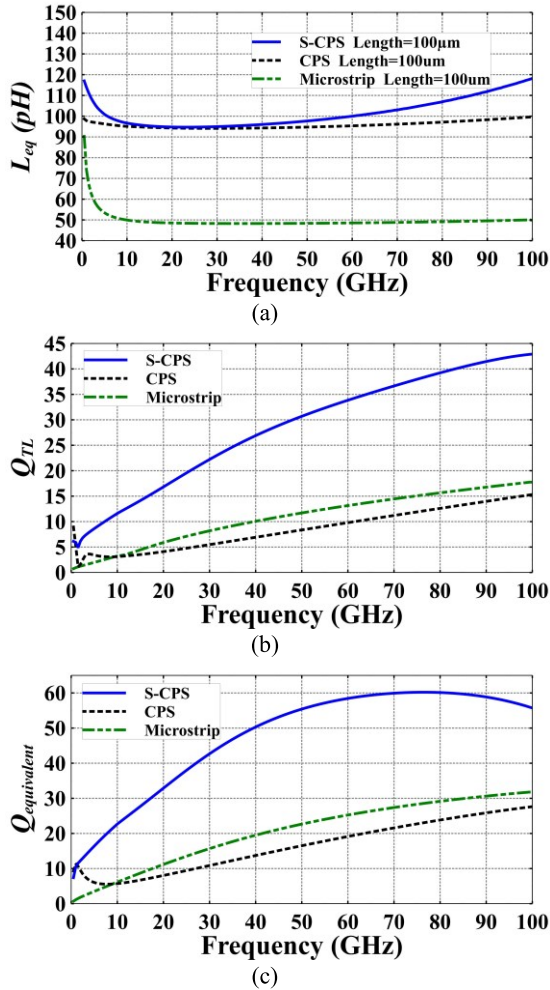


Fig. 7. EM performance of the three TLines S-CPS, CPS and microstrip considered to synthesize an inductance. (a) Equivalent inductances, (b) Q -factors of the TLines. (c) Q -factor of the equivalent inductances.

C. S-CPS synthesis in CMOS 55 nm technology

Once the interest of S-CPS equivalent inductance demonstrated, design method must be developed to give simple tools for circuit designers. Many design parameters have to be considered, with two competing objectives, (i) maximizing the electrical performance, and (ii) minimizing the size. It is clear that these two objectives cannot be reached at the same time, since the increase of the Q -factor of SW TLines requires wider TLines, thus increasing their overall size or footprint, as explained in [14]. Hence, in this paper, a trade-off between the electrical performance and the size was considered, and the method described hereinafter shows how to select the optimum dimensions of the S-CPS to reach the targeted trade-off. The S-CPS equivalent inductance was optimized for a working frequency of 80 GHz, with a targeted value of 107 pH, as stated in Section II.B. The structure of the considered S-CPS is given in Fig. 8. In S-CPS structures, there are two groups of geometrical parameters impacting the inductance design. The first ones are the planar dimensions of S-CPS (W_s and G). The second ones are the strip thickness (t_s) and the height between the strips and the shield (t), respectively, as described in Fig. 8(a). Besides the mentioned design parameters, the dimensions SS and SL associated to the

shield were set to 0.6 μm , following the studies carried out in [14], [15].

The $RLCR$ model proposed in [14] and coded in [10], which differs from the classical $RLCG$ telegraphist model, is used to synthesize the desired inductance without using time consuming EM simulations. From inputs that are the physical dimensions of the S-CPS (width W_s , gap G , shield dimensions SS and SL) and the properties of the BEOL (such as thickness of layers, metal conductivity and dielectric permittivity), the model gives the electrical parameters of the S-CPS (Fig. 8 (b)). In this manner, from the $RLCR$ electrical model of the S-CPS, the desired inductance is easily synthesized.

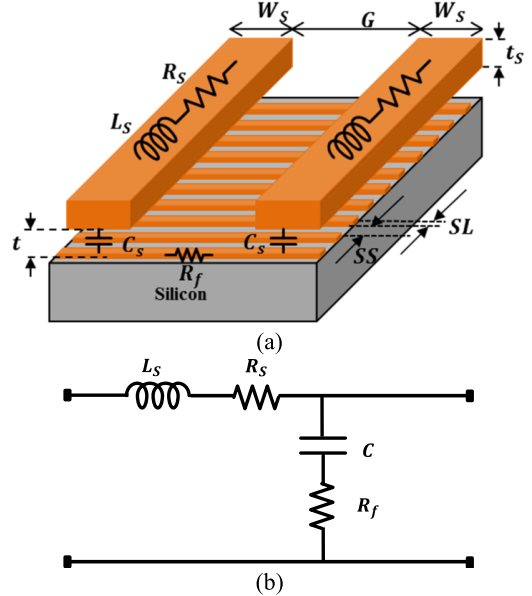


Fig. 8. S-CPS: (a) 3-D topology and (b) $RLRC$ Model.

Since the electrical model is based on physical parameters, it allows a fast exploration of the design space, which helps the designer to find the optimum values for the planar dimensions as well as the layers used in the BEOL. In this paper, the total width of the S-CPS was set to 50 μm , i.e. $2W_s + G = 50 \mu\text{m}$. The value of 50 μm results from the trade-off mentioned above: a wider line would lead to a higher quality factor, but at the expense of a larger size. At the same time, it increases the complexity of the interconnection between the S-CPS, varactors and the CCP. Indeed, since the CCP and varactors are lumped and quite small, tapers are necessary to connect with the S-CPS. Hence, the wider the S-CPS, the higher the parasitic effects of the tapers.

Fig. 9 gives two charts showing L_{eq} and Q_{eq} of the equivalent inductance versus its length, for the VCO working frequency of 80 GHz. These charts help in determining the required inductance. Fig. 9(a) depicts L_{eq} and Q_{eq} for various W_s and G for a given choice of the layers used in the BEOL (i.e. fixed t_s and t). Fig. 9(b) illustrates the same variation of L_{eq} and Q_{eq} , but for various t , for fixed W_s , G and t_s . It is worth to mention that the current study was carried out by considering a generic BEOL.

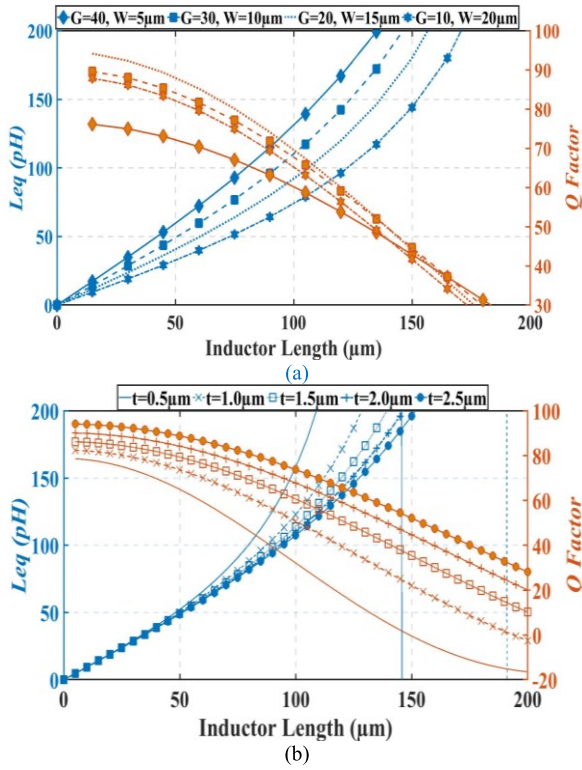


Fig. 9. (a) BEOL constant ($t = 2 \mu\text{m}$, $t_s = 5.4 \mu\text{m}$), W and G vary. (b) BEOL varies, W and G constant ($G = 30 \mu\text{m}$, $W = 10 \mu\text{m}$, $t_s = 5.4 \mu\text{m}$).

From Fig. 9(a), it can be observed that the maximum L_{eq} is obtained for the maximum $G = 40 \mu\text{m}$. This was expected since a wider gap leads to a larger linear inductance, and consequently a larger equivalent inductance of the shorted TLine. It was also explained in [14], [16] that a wider G leads to both higher characteristic impedance and relative effective dielectric constant for SW TLines. However, an optimum combination of G and W_s exists to reach the maximum Q -factor, as explained in [14]. This occurs for $G = 20 \mu\text{m}$ in the present study. Therefore, to make a trade-off between performance and size, the combination $G = 30 \mu\text{m}$ and $W_s = 10 \mu\text{m}$ was selected.

In Fig. 9(b), it is observed that the highest Q -factor is obtained for the highest t , while the equivalent inductance remains almost constant. Increasing t reduces the effect of the shield, thus reduces the SW behavior of the S-CPS, but also leads to a lower attenuation constant and hence, a higher quality factor, as explained in [14]. On the other hand, by lowering t the SW effect is emphasized since $\epsilon_{\text{reff-S-CPS}}$ increases as it can be observed on the variation of L_{eq} , which achieves lower resonance frequency for smaller t , leading consequently to a more interesting shrink property. Here again, the choice of t results from a trade-off between size and quality factor.

Finally, based on the above analysis as well as the provided charts and to fulfill the BEOL associated to the used technology, the retained parameters for the inductance are as follow, $l = 98.4 \mu\text{m}$, $G = 30 \mu\text{m}$, $W = 10 \mu\text{m}$, $t_s = 5.4 \mu\text{m}$

and $t = 2.01 \mu\text{m}$, $SS = SL = 0.6 \mu\text{m}$, leading to $Q_{eq} = 60$ for the targeted $L_{eq} = 107 \text{ pH}$.

These results obtained from the model developed in [10] were coded in MATLAB and validated by EM simulations. The variation of L_{eq} and Q_{eq} versus frequency, from DC up to 120 GHz, are plotted in Fig. 10. A good agreement between EM simulations and the electrical model based simulations was obtained. L_{eq} increases with frequency and tends to infinity at a resonant frequency for which the electrical length of the TLine is equal to 90° (around 200 GHz in the studied case, not plotted herein). In addition Q_{eq} passes through a maximum equal to 60 around 75 GHz, and then decreases as the frequency increases. It can be observed that the Q -factor of the lumped equivalent inductance is always greater than the TLine one, from DC to 100 GHz. They cross around 120 GHz. Note that these results match with the theoretical study presented in section II.A, which validates again the adopted approach in synthesizing the S-CPS inductor only using the mentioned algorithm coded in MATLAB.

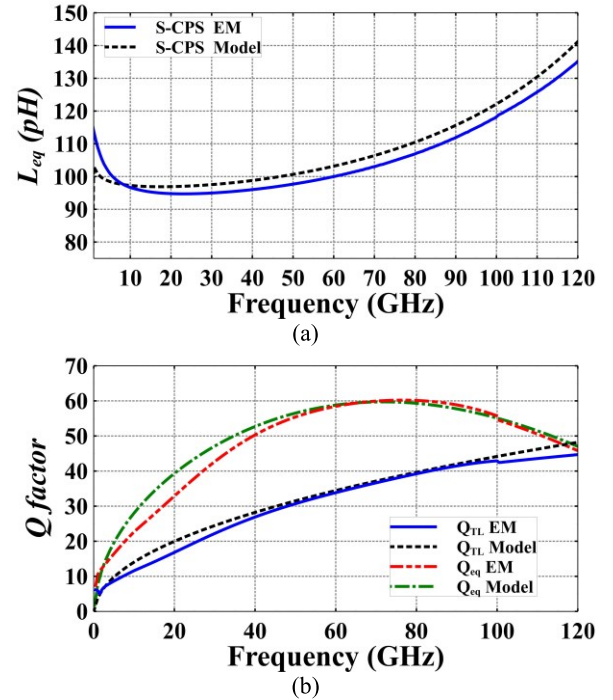


Fig. 10. Performance computed for practical S-CPS (a) Equivalent lumped inductance L_{eq} (b) Q_{eq} and Q_{TL} .

IV. IMPLEMENTATION AND RESULTS

In order to validate the concept, two VCOs were designed in CMOS 55 nm technology. First, a classical LC -tank VCO was designed, which serves as reference, and the second is the proposed VCO designed with S-CPS synthesized inductance. As already stated, to achieve a fair comparison, both designs consider the same varactors and the same inductance value of 107 pH. The reference VCO was designed with a lumped inductance of 107 pH from the PDK and same inductance value was synthesized with S-CPS for the proposed VCO. The used lumped inductor is a one turn spiral shape owning coil width of $5.5 \mu\text{m}$ and inner diameter of $55 \mu\text{m}$. The CCP was sized to compensate the losses of the tanks with the same

compensation factor ($K = 3$). Since the losses of the synthesized equivalent inductance are lower ($R_p = 966 \Omega$) than its lumped counterpart ($R_p = 610 \Omega$), the CCP was designed with smaller MOS transistors than the ones of the reference VCO, which leads to lower parasitic capacitances. In addition, it consumes less DC current as presented in TABLE I.

TABLE I
DESIGN PARAMETERS OF THE VCOs

Parameters	LC-tank VCO	S-CPS Inductance SWO
Inductance	107 pH	107 pH
Inductance Q_{TL}/Q_{eq}	NA/23	38/60
Varactor (max/min)	8.9 fF/4.4 fF	8.9 fF/4.4 fF
Varactor Q -factor	13.5	13.5
Tank Q -factor	8.5	11.1
Negative Resistance ($R_p/3$)	210 Ω	322 Ω
Cross-Coupled Pair (W/L)	17 $\mu\text{m}/0.06 \mu\text{m}$	11 $\mu\text{m}/0.06 \mu\text{m}$
Parasitic Capacitance ($C_{par-CCP}$)	23.5 fF	16.5 fF
Bias Current (I_d)	7.57 mA	4.74 mA
V_{DD}	1.2 V	1.2 V

Fig. 11 shows the chip micrograph of both VCOs. Total chip area for each VCO is 0.4 mm^2 (including RF and DC pads). The area of the synthesized equivalent inductance is comparable to the size of the inductance of the PDK, hence higher electrical performance was achieved without sacrificing the size.

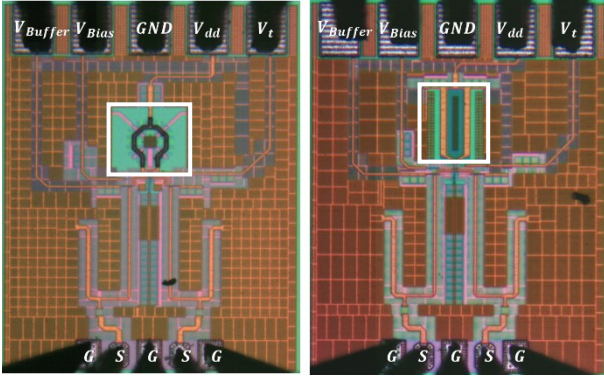


Fig. 11. Chip micrograph of VCO with LC-tank (left) and S-CPS synthesized inductance (right).

To characterize the performance of the proposed VCOs, on-wafer probing was performed. The losses of the microprobe and cable used were de-embedded a posteriori (about 10 dB at 80 GHz). The single-ended output spectrum and phase noise of VCOs were measured with a Keysight spectrum analyzer N9040B and E-band harmonic mixer. Fig.12 depicts the measurement setup used in the characterization.

Fig. 13 shows the measured output spectrum of the S-CPS inductance based. Thanks to a lower parasitic capacitance in the S-CPS inductance based VCO, its FTR is higher than the reference VCO. Fig. 14 shows the variation of the measured oscillation frequency versus the voltage control. Indeed, for the reference VCO, the measured F_{osc} varies from 73.78 GHz to 77.12 GHz leading to a 3.34 GHz tuning range, whereas for the S-CPS inductance based VCO, the measured F_{osc} varies from 75.36 GHz to 79.05 GHz, leading to a slightly higher 3.69 GHz tuning range.

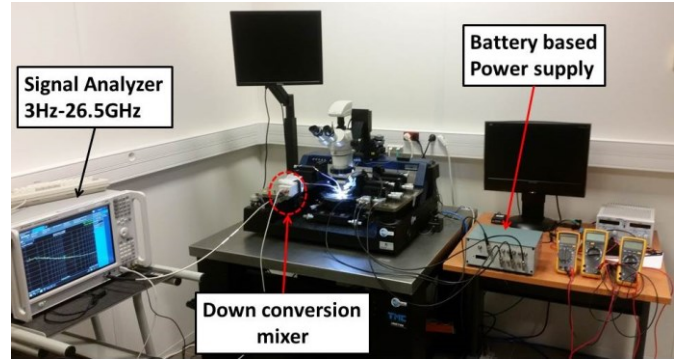


Fig. 12. Setup used to characterize the VCOs.

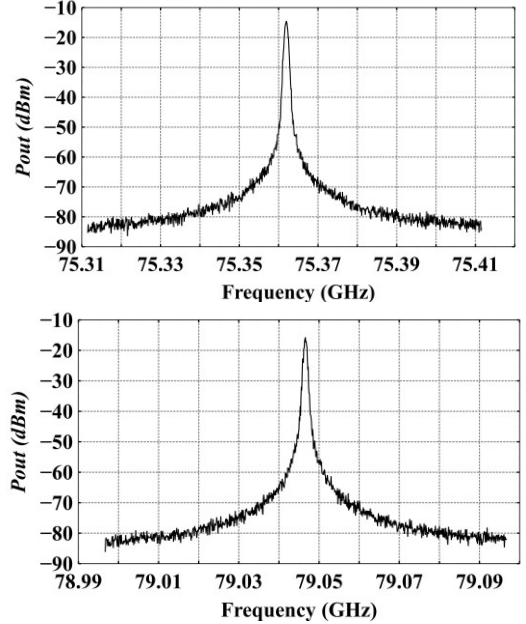


Fig. 13. Measured spectrum of the VCO with S-CPS inductance for the extreme values of tuning voltage (0 and 2.5 V) at a SPAN of 100 MHz.

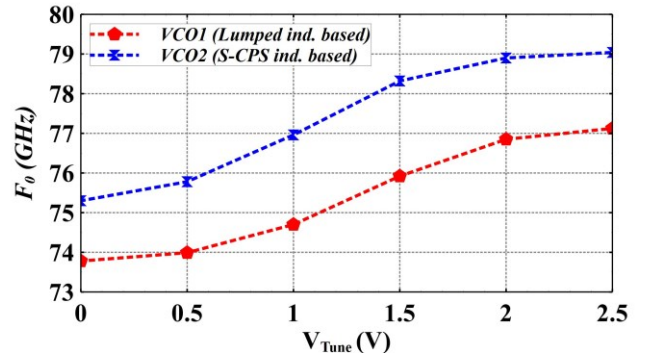


Fig. 14. Measured oscillation frequency versus V_{tune} .

Fig. shows the measured phase noise for both VCOs within the frequency offset band of 1 MHz and 10 MHz. Measured phase noise at 10 MHz offset is -115 dBc/Hz for S-CPS inductance based VCO whereas a -112 dBc/Hz is obtained for the reference VCO. Moreover, Fig. 16 plots the phase noise of both VCOs at various oscillation frequencies.

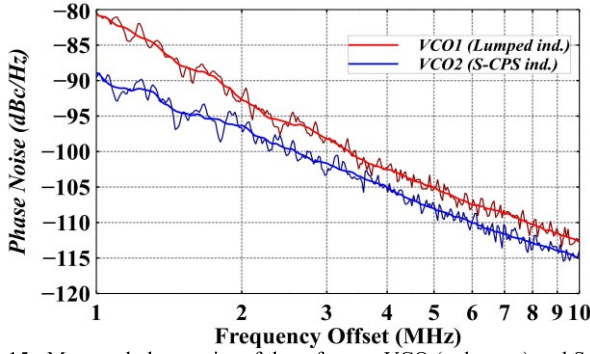


Fig. 15. Measured phase noise of the reference VCO (red curve) and S-CPS inductance based VCO (blue curve).

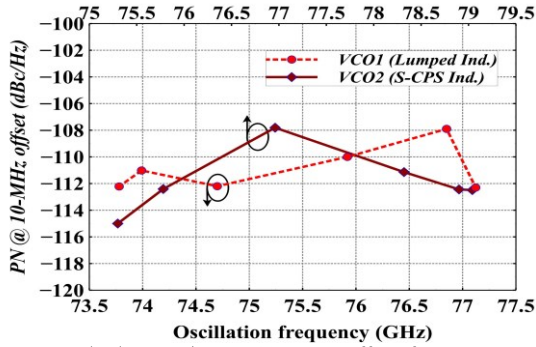


Fig.16. Measured phase noise at 10 MHz offset frequency at various oscillation frequencies.

Another important performance parameter is the power consumption. With a V_{DD} of 1.2 V, the power consumptions of the reference VCO and S-CPS inductance based VCO cores are 9.0 mW and 5.7 mW, respectively, while the output buffer consumption is 9.2 mW. After correcting the probe and cable losses, measured output powers of reference VCO and S-CPS inductance based VCO are -4.4 dBm and -4.5 dBm, respectively, leading to power efficiencies of 4.03 % and 6.22 %, respectively.

Measurement results are summarized in Table II and compared to the state-of-the-art results at mm-waves. For comparison purposes, we use the widely accepted figure of merit (FOM) and FOM with tuning range (FOM_T) defined as [17],

$$FOM = L(\Delta f) - 20 \times \log\left(\frac{F_{osc}}{\Delta f}\right) + 10 \times \log\left(\frac{P_{diss}}{1mW}\right), \quad (17)$$

$$FOM_T = FOM - 20 \times \log\left(\frac{FTR}{10}\right), \quad (18)$$

where $L(\Delta f)$ is the phase noise at the offset frequency Δf from oscillation frequency F_{osc} in dBc/Hz. P_{diss} is the DC power consumption in mW. Even though the realized performance by the S-CPS inductance based VCO are competitive, it should be noted that the main objective of the comparison is to highlight the advantage of the S-CPS inductor based VCO as compared to its counterpart designed with lumped LC tank.

TABLE II
MEASURED PERFORMANCES OF THE VCOS

Ref.	Tech.	F_{osc} (GHz)	FTR (%)	P_{dc} (mW)	PN @ 10 MHz (dBc/Hz)	FOM (dBc/Hz)	FOM _T (dBc/Hz)
[4]	65-nm CMOS	81.5	14	33	-105	-179.7	-182.6
[6]	65-nm CMOS	76.5	15.8	14.3	-108.4	-174.5	-178.5
[17]	90-nm CMOS	56.7	16	8.7	-118.7	-184.3	-187.4
[18]	65-nm CMOS	73.8	9 ⁺	8.4	-112.2	-180.0	-192.2
[19]	130-nm CMOS	89.8	0.6	22	-107.7*	NA	NA
[20]	55-nm BiCMOS	80	15**	18	-100.5*	-186.0	-189.5
[21]	65-nm CMOS	70.2	23 ^o	7.7	-118	-180.4	-187.4
[22]-1	65-nm CMOS	75.9	7.3	12	-109.4	-176.2	-173.6
[22]-2	65-nm CMOS	89.4	5.1	11	-108.3	-176.9	-171.1
[23]	180-nm BiCMOS	60	17 ^x	19	-87.5*	176.0	180
[24]	65-nm CMOS	64	7	5	-113	-182.2	NA
[25]	40-nm CMOS	86	5.8	28.4	-108.5/- 118.8	-172.5/- 183.2	NA
[26]	130-nm BiCMOS	74	4.86	65	-99.3*	-172.3	NA
[27]	130-nm BiCMOS	57	16.8	7.6	-124.75	-186.3	190.85
VCO1 [#]	55-nm CMOS	75.45	4.42	9.08	-112	-180.5	-173.4
VCO2 ^{##}	55-nm CMOS	77.1	4.80	5.69	-115	-185.0	-178.6

*PN at 1MHz offset; **FTR achieved with capacity bank; ⁺ One mode selected for FTR; ^oFTR achieved with switched transformer; ^xSwitchable coupled VCO #Reference VCO, ## S-CPS inductor based VCO.

V. CONCLUSION

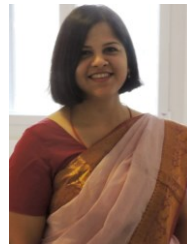
This paper demonstrates the advantages of synthesizing the inductor of a LC-VCO with S-CPS for mm-wave circuits in silicon technology. Based on an electrical model, the design of the inductor is quite straightforward with a good precision and does not require intensive EM simulations. A sizing method for the inductor and for the VCO was proposed. The approach was validated through a fair comparison with a reference lumped tank based LC-VCO designed with the same varactors and on the same technology. From the measurement results, merits of the proposed approach can be remarked. Thanks to the use of slow-wave transmission lines, the synthesized inductor has a higher Q -factor, which results in higher VCO performance in terms of FTR and power consumption.

REFERENCES

- [1] C. Changhua, K. O. Kenneth, "Millimeter-wave voltage-controlled oscillators in 0.13- μ m CMOS technology", *IEEE J. Solid-State Circuits*, vol.41, no.6, pp.1297–1304, 2006.
- [2] H. Hsieh, Y. Chen, L. Lu, "A Millimeter-Wave CMOS LC-Tank VCO With an Admittance-Transforming Technique", *IEEE Trans. Microw. Theory Tech.*, vol.55, no.9, pp.1854–1861, 2007.
- [3] W. F. Andress, D. Ham, "Standing wave oscillators utilizing wave-adaptive tapered transmission lines", *IEEE J. Solid-State Circuits*, vol.40, no.3, pp.638–651, 2005.
- [4] H. Koo, C. Kim, S. Hong, "A G-Band Standing-Wave Push-Push VCO Using a Transmission-Line Resonator", *IEEE Trans. Microw. Theory*

- Tech.*, vol.63, no.3, pp.1036–1045, 2015.
- [5] J. Chien, L. Lu, "Design of Wide-Tuning-Range Millimeter-Wave CMOS VCO With a Standing-Wave Architecture", *IEEE J. Solid-State Circuits*, vol.42, no.9, pp.1942–1952, 2007.
- [6] G. Liu, R. Berenguer, Y. Xu, "A MM-Wave Configurable VCO Using MCPW-Based Tunable Inductor in 65-nm CMOS", *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol.58, no.12, pp.842–846, 2011.
- [7] G. Huang, S. Kim, Z. Gao, S. Kim, V. Fusco, B. Kim, "A 45-GHz CMOS VCO Adopting Digitally Switchable Metal-Oxide-Metal Capacitors", *IEEE Microw. Wireless Compon. Lett.*, vol.21, no.5, pp.270–272, 2011.
- [8] W. Hant, T. W. Ku, R. Wong, M.-. F. Chang, "A 60GHz CMOS VCO Using On-Chip Resonator with Embedded Artificial Dielectric for Size, Loss and Noise Reduction", *Proc. IEEE Int. Solid-State Circuits Conf. - Digest of Technical Papers*, pp.1218–1227, 2006.
- [9] M. Abdel-Aziz, al., "Slow-wave high-Q coplanar striplines in CMOS technology and their RLCG model", *Microw. Optical Tech. Lett.*, vol.54, no.4, pp.650–654, 2012.
- [10] A. Bautista, A. Franc, P. Ferrari, "Accurate Parametric Electrical Model for Slow-Wave CPW and Application to Circuits Design", *IEEE Trans. Microw. Theory Tech.*, vol.63, no.12, pp.4225–4235, 2015.
- [11] E. Sharma, E. Pistono, P. Ferrari, S. Bourdel "80 GHz VCO with Slow-wave Coplanar Stripline Synthesized Differential Inductor," *IEEE International Conference on Electronics, Circuits and Systems, ICECS 2018*, 9-12 Dec. 2018, Bordeaux, France.
- [12] W. Wu, J. R. Long, R. B. Staszewski, "High-Resolution Millimeter-Wave Digitally Controlled Oscillators With Reconfigurable Passive Resonators," *IEEE J. Solid-State Circuits*, vol. 48, no. 11, pp. 2785–2794, Nov. 2013.
- [13] M. Abdel Aziz et al., "Slow-wave high-Q coplanar striplines in CMOS technology and their RLCG model", *Microw. Optical Tech. Lett.*, vol. 54, no 3, pp. 650–654, March 2012
- [14] A.-L. Franc, E. Pistono, G. Meunier, D. Gloria, and P. Ferrari, "A Lossy Circuit Model Based on Physical Interpretation for Integrated Shielded Slow-wave CMOS Coplanar Waveguide Structures," *IEEE Trans. on Microw. Theory Tech.*, vol. 61, no. 2, pp. 754–763, Feb. 2013
- [15] A. Bautista, A. Franc and P. Ferrari, "An accurate parametric electrical model for slow-wave CPW," *IEEE International Microwave Symposium, MTT-S 2015*, Phoenix, AZ, 2015, pp. 1–4.
- [16] A. Bautista, M. Abdel-Aziz, F. Podevin, and P. Ferrari "A Predictive Model for Slow-wave Coplanar Striplines in integrated technologies", *Proc. IEEE Int. Microw. Theory Tech. Symposium, MTT-S 2016*, May 17-22, 2016, San Francisco, USA.
- [17] T. Y. Lu et al., "Wide Tuning Range 60 GHz VCO and 40 GHz DCO Using Single Variable Inductor," in *IEEE Trans. on Circuits Syst. I: Regular Papers*, vol. 60, no. 2, pp. 257–267, Feb. 2013.
- [18] J. Yin and H. C. Luong, "A 57.5–90.1-GHz Magnetically Tuned Multimode CMOS VCO," *IEEE J. Solid-State Circuits*, vol. 48, no. 8, Aug. 2013.
- [19] A. Tarkeshdouz, A. Mostajeran, S. Mirabbasi, and E. Afshari, "A 91-GHz Fundamental VCO With 6.1% DC-to-RF Efficiency and 4.5 dBm Output Power in 0.13- μm CMOS," *IEEE Solid-State Circuits Letters*, vol. 1, no. 4, April 2018
- [20] L. Iotti, A. Mazzanti, and F. Svelto, "Insights Into Phase-Noise Scaling in Switch-Coupled Multi-Core LC VCOs for E-Band Adaptive Modulation Links," *IEEE J. Solid-State Circuits*, vol. 52, no. 7, July 2017.
- [21] Y. Chao and H. C. Luong, "Analysis and Design of Wide-Band Millimeter-Wave Transformer-Based VCO and ILFDs," *IEEE Trans. on Circuits Syst. I, Reg. Papers*, vol. 63, no. 9, Sep. 2016.
- [22] T. Xi, S. Guo, Ping Gui, Daquan Huang, Yanli Fan, and Mark Morgan, "Low-Phase-Noise 54-GHz Transformer-Coupled Quadrature VCO and 76-/90-GHz VCOs in 65-nm CMOS," *IEEE Trans. on Microwave Theory and Techniques*, vol. 64, no. 7, July 2016.
- [23] Q. Zou, K. Ma, and K. S. Yeo, "A low phase noise and wide tuning range millimeter-wave VCO using switchable coupled VCO-cores," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 62, no. 2, pp. 554–563, Feb. 2015.
- [24] T. N. Nguyen, P. P. Pande, D. Heo, "A 64 GHz 5 mW low phase noise Gm-boosted colpitts CMOS VCO with self-switched biasing technique," *IEEE International Microwave Symposium, MTT-S 2015*, 17-22 May 2015, Phoenix, USA.
- [25] M. Vigilante, P. Reynaert, "An E-Band low-noise Transformer-Coupled

- Quadrature VCO in 40 nm CMOS," *40th European Solid State Circuits Conference, ESSCIRC 2014*, 22-26 Sept. 2014, Venice Lido, Italy.
- [26] G. Sapone, E. Ragonese, A. Italia, and G. Palmisano, "A 0.13- μm SiGe BiCMOS Colpitts-Based VCO for W-Band Radar Transmitters," *IEEE Trans. on Microwave Theory and Techniques*, vol. 61, no. 1, Jan. 2013
- [27] A. H. M. Shirazi, A. Nikpaik, R. Molavi, S. Lightbody, H. Djahanshahi, M. Taghivand, S. Mirabbasi and S. Shekhar, "On the Design of mm-Wave Self-Mixing-VCO Architecture for High Tuning-Range and Low Phase Noise," *IEEE J. Solid-State Circuits*, vol. 51, no. 5, pp. 1210–1222, May 2016

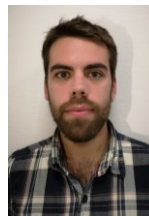


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