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Yoann Pascal, Mickael Petit, Denis Labrousse, François Costa. Thermal simulations of SiC MOSFETs under short-circuit conditions: influence of various simulation parameters. 2019 IEEE International Workshop on Integrated Power Packaging (IWIPP), Apr 2019, Toulouse, France. 10.1109/iwipp.2019.8799085 . hal-02187486

**HAL Id: hal-02187486**

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Submitted on 17 Jul 2019

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# Thermal simulations of SiC MOSFETs under short-circuit conditions: influence of various simulation parameters

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**Abstract**—The temperature distribution in a Silicon Carbide (SiC) MOSFET during a destructive short-circuit is simulated using a custom 1D-finite difference model implemented using Matlab. Some of the main assumptions usually put forward in the literature dealing with this kind of simulations are tested in this paper. We show that some of those simplifications (model of the heat source, die top-side boundary conditions, etc.), sometime in-spite of common sense, have a great impact on the simulated temperature.

**Keywords**—modelling, short-circuit, SiC, thermal simulation

## I. INTRODUCTION

Short-circuits are highly stressful conditions, in particular for power transistors: the high voltage applied across the component, together with the resulting overcurrent (usually 3 to 10 times as high as the nominal value), results in extremely high power dissipation, which can reach several hundreds of kW in TO-247-packaged devices. This induces temperature gradients and, as a result, tremendous thermomechanical stress – and even destructive over heating if the short-circuit lasts too long. And yet, these highly stressful constrains are quite commonly met by power circuits due, for instance, to errors from the controller or hard shorts on the loads.

Having at ones disposal a tool accurately simulating junction temperature during such test would be of great interest. As a matter of fact, it could be used to predict the robustness of a circuit and to help understand failure mechanisms such as critical temperatures and heating rates, current crowding, etc. [1], [2]. It could also be used for die- and packaging- design so as to optimise robustness, e.g. by studying the influence of the base-plate thickness or that of the moulding composition. Furthermore, such tool could be used to estimate the maximum acceptable response time of a protective circuit [3], [4].

Many research papers have attempted to tackle the aforementioned issues. Published estimators can be based on linear or non-linear models implemented in a circuit simulator (e.g. SPICE) [5]–[7] or using a dedicated Finite Element (FE) software (e.g. Ansys) [2], [4], [8]–[10]. Although the first approach is a priori much faster, it is usually limited to a few thousands nodes (and often far less), leading to moderate accuracy. On the other hand, complete 3D FE simulations can be much more costly and accurate [3], [11]. If some papers perform electro-thermal simulations

so as to couple thermal and electrical models [3], [5]–[7], [12], [13], others use experimental electrical measurements to define the heat source [9], [14]–[16].

This paper discusses some of the main and most common assumptions made in those thermal models. Its focus is on Silicon Carbide (SiC) MOSFET under short-circuit tests – although the method and results could be extrapolated to other devices and test conditions.

The study was conducted in the frame of power-die Printed Circuit Board (PCB) embedding. It was, in particular, developed in order to study the robustness of a new die top-side connection technic [17]. Its mains point was to estimate, through simulation, the robustness of a PCB embedded power die having its top-side connected to the circuit using a pressed piece of nickel foam [18].

A brief review of some models and their main features is given in section II, our own model is exposed in section III. Some simulation results are detailed in section IV, and various simulation parameters are tested in section V. A discussion is proposed in section VI; last, section VII concludes the paper.

## II. LITERATURE REVIEW

Many research paper dealing with die temperature estimation during short-circuit tests have been published. The main assumptions and methods found in some of them, mostly focused on SiC MOSFETs, are listed below.

Most models assume that the diffusivity of the material (epoxy resin for a discrete component or silicone gel in a power module) is low enough so that the heat flux through it can be neglected. It is also often assumed that the assembly (die alone or die, solder and base-plate) bottom side is at constant temperature. This is justified by the small heat diffusion length vs. the assembly thickness, which accounts for the heat not reaching the device bottom-side. Let us call Top side- and Bottom side- Standard Boundary Conditions (T-SBC & B-SBC) these common boundary conditions.

In [14], 1D and 3D models of a SiC JFET are built but only the temperature dependence of the thermal properties ( $\lambda$ ,  $c_p$ ) of SiC are taken into account; in particular the latent heat of aluminium is neglected. The die-attach and a base plate are included in the simulations. T- & B-SBC are used.

In [8], a 3D model of a SiC JFET, its solder, and base plate is proposed but no other 3D element (e.g. inhomogeneous current distribution) is modelled – except for

This work was supported by a grant overseen by the French National Research Agency (ANR-15-CE05-0010) – project HIT-TEMS.

the die edges which are adiabatic. The temperature dependence of the properties of SiC is taken into account. T- and B- SBC are used.

In [9], a 3D model, including the die, its solder and a baseplate, is used. The temperature dependence of the thermal properties ( $\lambda, c_p$ ) of the materials are neglected. The heat source is assumed to be distributed in a 3  $\mu\text{m}$ -thick layer of semi-conductor, supposedly modelling the channel. T- & B-SBC are used.

In [7], the die under study is discretized in a rather small number of virtual cells, thermally modelled by linear RC circuit in a Spice software. This approach results in 3D-simulations in which the emphasis is put in the main current-flow direction, with limited resolution (and therefore limited cost) in the orthogonal one.

In [4], a 2D Finite Element simulation of half a cell of SiC MOSFET is offered. The boundary conditions are implemented according to the datasheet. It is shown that the warmest point is located 2  $\mu\text{m}$  below the gate oxide. T- and S- SBC are used on the die surfaces.

In [10], a 2D model is proposed, with T- and S- SBC. The simulated p-well is 1  $\mu\text{m}$ -deep while the drift layer has doping concentration  $1.1 \cdot 10^{16} \text{cm}^{-3}$  and thickness 13  $\mu\text{m}$ . In [2], the same team studied the influence of cell-to-cell mismatch (channel doping, length, etc.) on the robustness.

In [13], a 1D-model is proposed, assuming a trapezoid E-filed in the depletion layer, with thickness 10  $\mu\text{m}$ . T-SBC are used whereas the package and heatsink are modelled by other means.

In [12], two 1D electro-thermal models are proposed. The first one is linear and implemented in PLECS whereas the other, implemented in Comsol, takes into account the temperature dependence of the thermal properties of the materials. A triangular power source is assumed; the drift layer has doping concentration  $1.1 \cdot 10^{16} \text{cm}^{-3}$ , it is buried 1  $\mu\text{m}$  deep in the bulk. T- and S- SBC are used on the die surfaces.

In [19], a 1D-model of a die, its solder, and a leadframe is proposed. The drift region has thickness 20  $\mu\text{m}$  and doping

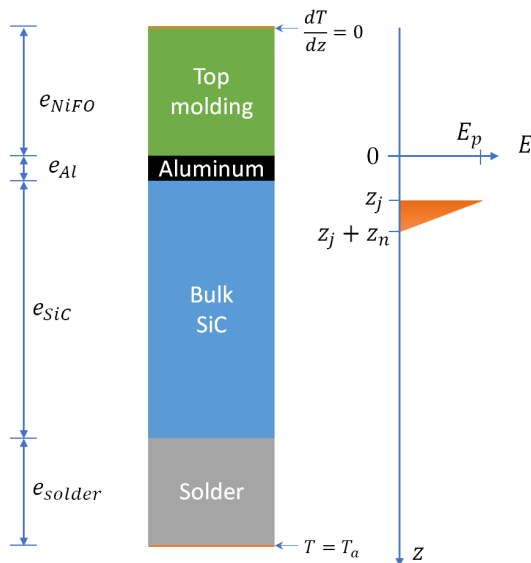


Fig. 1. Simulated model : structure and electric field

density  $2 \cdot 10^{15} \text{cm}^{-3}$ . T- & B- SBC are used.

In [15], three 1D models are compared. The most extensive one assumes a triangular electrical field and models the die as a chain of linear thermal R-C circuits. T-SBC is used whereas a linear R-C circuit is used to model solder and heatsink.

In [20], a 1D model of a SiC MOSFET and its solder are simulated. The simulated drift layer has doping concentration  $1 \times 10^{16} \text{cm}^{-3}$  and the power source is located 600 nm below the surface of the SiC crystal. T- & S- SBC are used.

In the 1D model proposed in [16], the heat source is on the front side of the chip. The temperature dependence of the properties of SiC is taken into account. T-SBC is used whereas the solder and the baseplate are modelled by a lumped resistance.

### III. MODEL

#### A. Structural model

Given the high aspect ratio of a SiC power MOSFET (the ratio thickness vs. width is in the order of 1 vs. 15 to 30) and the limited diffusion of heat in the die (cf. section III.C), it was assumed that the heat-flow within the die under study was uniaxial, in the  $z$ -direction, orthogonal to the die top-side. The 1D-model shown in Fig. 1 was therefore developed. It comprises the die itself, modelled as a SiC substrate and a top-side aluminium layer, a die-attach layer, and a layer of material (hereafter referred to as “NiFO”) modelling the moulding of the device.

The thicknesses of the various layers are given in TABLE I. In particular, those of the SiC and aluminium layers are those of the transistor under study, a CPM2-1200-0025B [21]. The modelled moulding layer is thinner than in a real package but simulations show that, due to the low diffusivity of heat in it, increasing  $e_{NiFO}$  would not improve the simulation accuracy while increasing the computational cost.

TABLE I. GEOMETRICAL PARAMETERS OF THE MODEL,  $z_j$  HAVING BEEN CALCULATED FOR A BIAS VOLTAGE  $V_{ds} = 600 \text{V}$

Parameter	Unit	Value
$e_{NiFO}$	$\mu\text{m}$	100
$e_{Die} = e_{Al} + e_{SiC}$	$\mu\text{m}$	180
$e_{Al}$	$\mu\text{m}$	4
$e_{SiC}$	$\mu\text{m}$	176
$e_{solder}$	$\mu\text{m}$	20
$z_j = e_{Al} + e_{pWell}$	$\mu\text{m}$	4,6
$z_n$	$\mu\text{m}$	8

T- & B- SBC (i.e. Neumann conditions on top and Dirichlet boundary on the bottom of the assembly) were used. However, simulations will show that this has limited impact on the results since the heat does not reach the model boundaries within the simulation time.

As for the heat source, a distributed power source was simulated, with volume power:

$$\dot{q}_v(z, t) = E(z, t) \cdot J(t) \quad (1)$$

Where  $E$  and  $J$  are the Electric field (E-field) and the current density.  $J$  was obtained from current measurements (detailed in [18]) normalized by the die active area. As for the E-field, it is assumed that the transistor drift layer is homogeneously doped and thick enough so that the E-field in the crystal is triangular. It is further assumed that it only

extends in the N-doped region. Under these assumptions and given the critical field of 4H-SiC ( $E_c \approx 200 \text{ V} \cdot \mu\text{m}^{-1}$  [22]) and the breakdown voltage of the transistor (specified as  $V_{BR}^* = 1200 \text{ V}$ , measured to be  $V_{BR} = 1310 \text{ V}$ ), one can estimate the drift layer doping concentration [23]:

$$N_d = \frac{\epsilon_0 \epsilon_{r,SiC} E_c^2}{2qV_{BR}} \approx 1 \cdot 10^{16} \text{ cm}^{-3}, \quad (2)$$

$$\epsilon_0 = 8.854 \cdot 10^{-12} \text{ Fm}^{-1}$$

Where  $q$  and  $\epsilon_{r,SiC}$  are the electron charge ( $q \approx 1.6 \cdot 10^{-19} \text{ C}$ ) and 4H-SiC relative permittivity ( $\epsilon_{r,SiC} \approx 9.66$ ). The depletion layer width can then be estimated from Gauss law, given the applied voltage  $V_{ds} = 600 \text{ V}$  [23]:

$$z_n = \sqrt{\frac{2\epsilon_{SiC}V_{ds}}{qN_d}} \approx 8 \mu\text{m} \quad (3)$$

The depth of the depletion layer  $e_{pwell} = 1 \mu\text{m}$  was chosen from values commonly found in the literature [10], [12].

### B. Heat equation

The complete, local, heat equation reads:

$$\rho c_p \frac{\partial T}{\partial t} - \nabla(\lambda \nabla T) = \dot{q}_v \quad (4)$$

Where  $\lambda$ ,  $c_p$  and  $\rho$  are the thermal conductivity, specific heat capacity and the mass density of the medium and  $\dot{q}_v$  is the volume heat production rate.  $\lambda$ ,  $c_p$  and  $\rho$  are a priori temperature dependant but changes in  $\rho$  are neglected.

Assuming that the heat flux is directed along the direction  $\vec{z}$ , (4) can be simplified as:

$$\rho c_p \frac{\partial T}{\partial t} - \frac{\partial}{\partial z} \left( \lambda \frac{\partial T}{\partial z} \right) = \dot{q}_v \quad (5)$$

$$\Leftrightarrow \rho c_p \frac{\partial T}{\partial t} - \frac{\partial \lambda}{\partial z} \frac{\partial T}{\partial z} - \lambda \frac{\partial^2 T}{\partial z^2} = \dot{q}_v$$

Due to the high temperature gradients expected to take place in the device, the space-derivative of  $\lambda$  cannot be neglected a priori.

Using the forward finite difference for time derivatives and centred finite differences for space derivatives yields:

$$T_{j+1}^i = T_j^i + \frac{\Delta t}{\rho_j^i \cdot c_{pj}^i} \dot{q}_{vj+1}^i \quad (6)$$

$$+ \frac{\Delta t}{\Delta z^2 \cdot \rho_j^i \cdot c_{pj}^i} [\lambda_j^{i+1}(T_j^{i+1} - T_j^i) - \lambda_j^i(T_j^i - T_j^{i-1})]$$

Where  $\Delta t$  and  $\Delta z$  are the time- and space- step sizes and  $(i, j) \in \mathbb{Z} \times \mathbb{N}$  are such that  $X_i^j$  is the value of quantity  $X$  at time  $t = j \cdot \Delta t$  and location  $z = i \cdot \Delta z$ . Our simulations use constant values:  $\Delta t = 10 \text{ ps}$ ,  $\Delta z = 150 \text{ nm}$ . Using steps twice larger results in temperature differences smaller than 10 K, proving that the selected values are small enough.

The temperature field at time  $t + \Delta t$  is therefore estimated using the temperature field and the related material properties ( $\lambda, c_p$ ) at time  $t$ .

### C. Physical properties of the materials

This study is, in particular, developed in order to study the robustness of a die top-side connection made of high pore density nickel foam. It therefore aims at assessing the impact of adding a proportion of nickel in a discrete component moulding on its robustness. The moulding ‘‘NiFO’’ is therefore modelled as homogenous material with properties linearized vs. the nickel proportion [24]:

$$X_{NiFO} = \alpha_{Ni} \cdot X_{Ni} + (1 - \alpha_M) \cdot X_{epoxy} \quad (7)$$

Where  $X_Y$  is the quantity  $X$  (e.g.  $\lambda$  or  $c_p$ ) for material  $Y$  (standard epoxy resin or nickel) and  $\alpha_{Ni}$  is the proportion of nickel in NiFO. Unless otherwise specified,  $\alpha_{Ni} = 0.3$ .

The temperature dependence of the physical properties of nickel, aluminium and SiC used in the model are taken into account. Those of epoxy are neglected, due to the lack of proper model combined with the large variety of available resins. Those of solder are also neglected: simulations show that the solder temperature remains very close to the ambient. Thermal conductivities and capacities at 298 K are given in TABLE II. Their normalised variations vs. temperature are given in Fig. 2.

TABLE II. PROPERTIES OF THE MATERIALS UNDER STUDY AT 298 K

@298 K	$\lambda$ (W/mK)	$c_p$ (J/K·kg)	$\rho$ (kg/m <sup>3</sup> )
Aluminium [25], [26]	239	910	2699
Nickel [26]	91	443	8902
Epoxy [27]	0.3	900	1250
NiFO (7)	27.6	763	3546
SiC [28]	353	1031	3211
Solder [29]	60	160	7400

The peak in aluminium thermal capacity accounts for the material enthalpy of fusion; its width was set to a non-zero value so as to help simulation convergence while fitting experimental values from [30] – simulations nonetheless show that this parameter has negligible impact on the estimated temperature field.

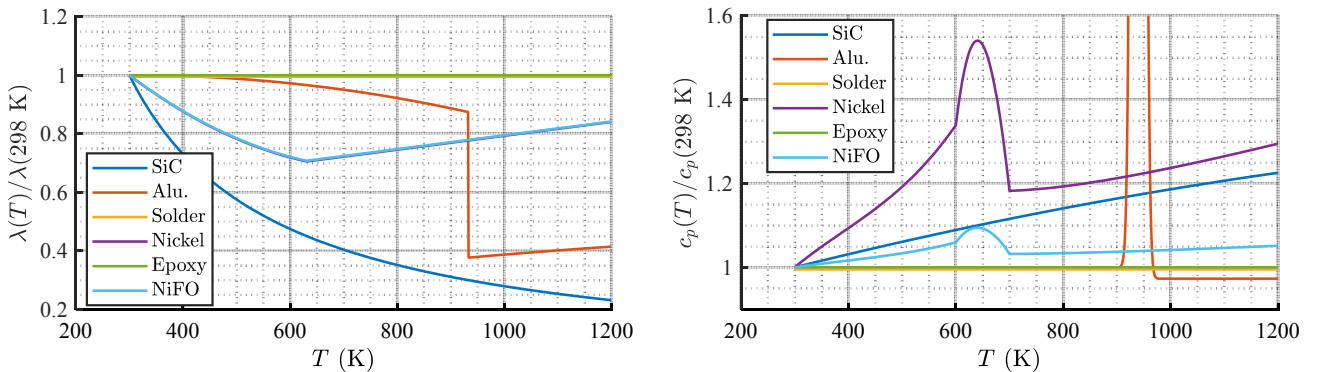


Fig. 2. Normalised ( $\lambda, c_p$ ) vs. temperature  $T$ .

For a given frequency  $f$ , thermal skin depth can be defined, analogously to electrical skin depth, as:

$$\delta_{th} = \sqrt{\frac{\lambda}{\rho c_p \pi f}} \quad (8)$$

$\delta_{th}$  is given at 1 MHz in Fig. 3. The short-circuit measured current density is given in Fig. 4, showing that the power source can be quite accurately modeled as a step with rise-time  $2 \mu\text{m}$ , i.e. bandwidth 160 kHz. Thermal skin-depths at this frequency are 2.5 times greater than those at 1 MHz. This suggests that the heat will not diffuse further than a few tens of  $\mu\text{m}$  in the SiC bulk or the NiFO.

#### IV. SIMULATION RESULTS

##### A. Reference design

The model defined in the previous section is solved using Matlab. The values of the parameters used in this simulation will be hereafter referred to as “reference ones”.

Fig. 4 shows the aluminium layer temperature vs. time. The plateau between  $6.5 \mu\text{s}$  and  $8.5 \mu\text{s}$  corresponds to the melting of aluminium. The temperature distribution at the end of the short-circuit, after  $11 \mu\text{s}$  of test, is given in Fig. 4. The temperature distribution is observed right before catastrophic failure, long after the control over the transistor had been lost – i.e. microseconds after the transistor could safely be turned off [1]. The hottest spot, located few micrometres under the top-side of the die (as already described in [4], [10], [31]), reaches over 1100 K. The temperature field is also shown in the  $(t, z)$ -plane.

##### B. Influence of the proportion of nickel in the moulding

Several simulations are performed for various values of  $\alpha_{Ni}$  ranging from 0 (the moulding is then pure epoxy resin) to 1 (the moulding is then pure nickel). The temperature distribution in the device at the end of the test ( $t = 11 \mu\text{s}$ ) is shown in Fig. 5. These simulations show that increasing the

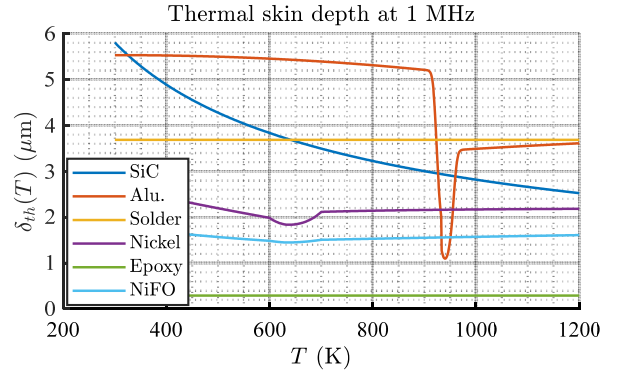


Fig. 3. Thermal skin depth  $\delta_{th}$  of the materials under study at 1 MHz.

proportion of nickel in the moulding greatly slows down the die heating, resulting in an increase in robustness. Though, there is no point in adding nickel in more than a few tens of micrometres above the die, due to limited heat diffusion length.

#### V. INFLUENCE OF SOME SIMULATION PARAMETERS

##### A. Boundaries conditions

As expected, Fig. 4 shows that the heat does not diffuse much in SiC (violet shaded area) nor in NiFO (green shaded area). This renders our choice of boundary conditions non-critical.

Setting a Neumann condition on the top-side of the die – and thus neglecting the impact of the moulding – would however result in an overestimation of the temperature. As a matter of fact, in the reference design, 18 % of the overall heat is stored in the moulding, against 10 % in the aluminium layer (including 5 % accounted for by the enthalpy of fusion) and 71 % in the SiC bulk. Furthermore, in the case of longer and less powerful short-circuits, modelling the leadframe/base plate might prove necessary since heat might reach it [4], [8].

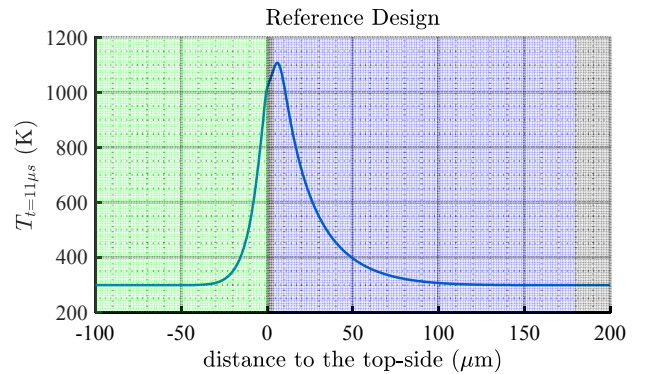
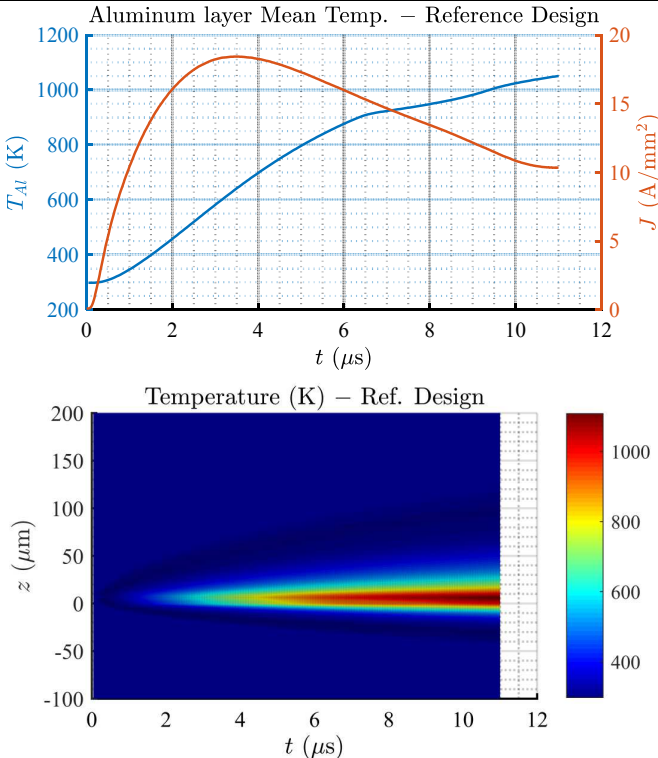


Fig. 4. Simulation results. (top left): aluminum layer mean temperature (blue) and current density (red) vs. time; (right) die temperature profil at the end of the short circuit (shaded areas: green: NiFO, dark grey: aluminum, violet: SiC, light grey: solder); (bottom left): temperature field in the time  $\times$  space domain.



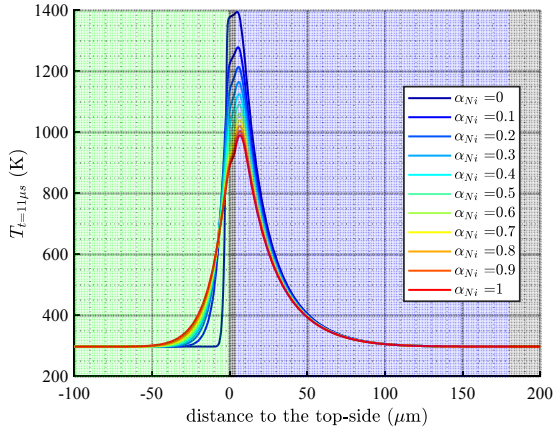


Fig. 5. Temperature profile in the device at the end of the short circuit for various values of  $\alpha_{Ni}$

### B. Influence of the temperature dependence of $(\lambda, c_p)$

Taking into account the temperature dependence of  $(\lambda, c_p)$  has already been proven paramount, for instance in [32], for an Si IGBT. Similar conclusions can be drawn from our model since the temperature reached at the end of the short-circuit is 175 K lower when neglecting this dependence (Fig. 6). This is due to the fast decrease in conductivity, slightly compensated by an increase in heat capacity, which results in a very local heating of the die.

### C. Power source

In [33], the authors estimate the thickness of the drift layer assuming a triangular E-fied distribution with peak value the critical field of 4H-SiC (i.e.  $\approx 200$  V/ $\mu\text{m}$ ) at the breakdown voltage (i.e. 1200 V). They then find that the drift layer should be 10.9  $\mu\text{m}$ -thick, with a doping concentration of  $N_d = 1.07 \cdot 10^{16} \text{cm}^{-3}$ . This value was then modified so that the simulated results agree with the datasheet:  $N_d = 5.7 \cdot 10^{17} \text{cm}^{-3}$ . In [22], a drift layer with doping concentration  $2.5 \cdot 10^{15} \text{cm}^{-3}$  is modelled. On the other hand, various values can be found for the depth of the junction ( $e_{pwell}$ ): from 0 in [13], [16], 0.6  $\mu\text{m}$  in [20], 0.7  $\mu\text{m}$  in [9], 1  $\mu\text{m}$  in [10], [12], about 1.1  $\mu\text{m}$  in [4], [33]. Last, if most papers consider that the E-field is triangular, some (e.g. [13]) consider a trapezoidal one.

This denotes a great uncertainty on the die structure and, ergo, on the power source characteristics.

Simulations have been performed so as to assess the

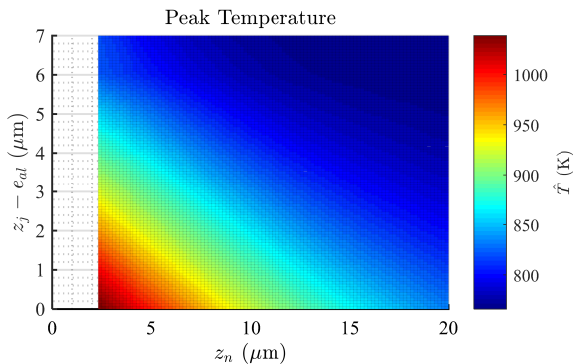


Fig. 7. Peak die temperature vs depletion layer thickness ( $z_n$ ) and depth under the aluminum layer ( $z_j - e_{Al}$ ).

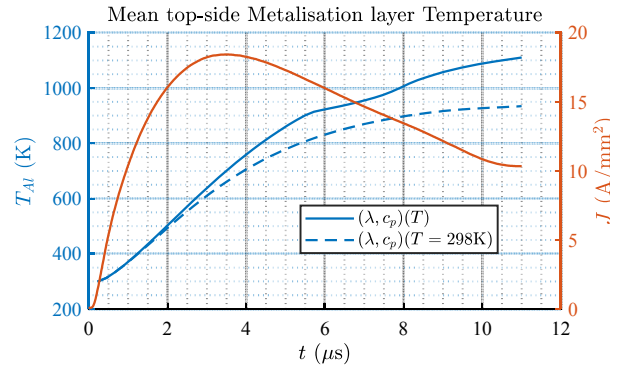


Fig. 6. Comparison of the aluminum layer temperatures neglecting (dotted blue line) or taking into account (solid blue line) the temperature dependence of  $(\lambda, c_p)$ ; current density (red line).

impact of the power source model on the temperature field. Results are given in Fig. 7, where the die peak temperature is shown vs. the depletion layer width  $z_n$  and the junction depth  $z_j$ .  $z_n$  was varied between 2.3  $\mu\text{m}$  and 20  $\mu\text{m}$ , corresponding to doping concentrations [23] ranging from  $5 \cdot 10^{15} \text{cm}^{-3}$  to  $5 \cdot 10^{16} \text{cm}^{-3}$ , whereas  $z_j \in [0, 7] \mu\text{m}$ . Fig. 7 shows that the peak temperature is highly sensitive to the power source modelling. As a matter of fact, in spite of the limited domain covered by these simulations, peak temperatures ranging from 760 K to 1040 K were found.

Although this question has not been addressed, one could expect the field shape (i.e. triangular vs. trapezoidal) to have notable impact on the temperature field.

## VI. DISCUSSION

### A. On the 1D- assumption, influence of bonding wire feet

1D simulations average the device over its surface so as to exceedingly simplify the problem. In particular, current densities mismatch among cells, a phenomenon that cannot be captured by simple 1D models, can result in hotspots, thereby greatly reducing the device robustness [34].

2D models combine thermal and electrical aspects to simulate cells in details (J-FET, drift region, etc.). They can be useful to identify hotspots in cells. Though, high computational cost makes it difficult to study numerous cells simultaneously – except in papers such as [2] where the method can be used to simulate local mismatches.

3D simulations can be used to analyse the effects of die edges and non-active areas, bond-wire feet, and local irregularities (e.g. threshold voltage dispersion). However, due to the low in-plane diffusion of heat in the device, it is assumed in [14] that the heat removed from the die through the bond-wires can be neglected. As a matter of fact, given the time-scale of the study, the heat diffusion length is limited to a few tens of micrometres both in aluminium and SiC, which is much smaller than the distance between bond wires feet. It is most likely that the impact of bond wires would therefore be too highly localised to have notable effect on the die hottest spots – and therefore on the device robustness. For the same reasons, the non-active parts of the die will only be able to cool locally the die, thereby negligibly increasing its robustness. Extensive 3D electro-thermal simulations would nonetheless be required to validate this assertion.

## B. Influence of SiC doping on ( $\lambda, c_p$ )

The influence of the doping concentration on the thermal properties of SiC has been neglected in this study. Yet, the decrease of thermal conductivity [35] with doping might lead to a significant underestimation of the semiconductor peak temperature. Finding accurate models might however prove quite challenging.

## VII. CONCLUSION

A 1D thermal model of a SiC power MOSFET, its solder and top-side moulding was implemented in Matlab. The model was first used to assess the impact of loading the die moulding with nickel. Second, some parameters of the model were varied so as to assess the validity of some assumption commonly found in the literature. Simulations showed that applying Neumann boundary conditions on the top-side of the die leads to a small overestimation of the die temperature. It also appeared that taking into account the temperature dependence of the thermal properties of the materials (in particular SiC) greatly impact the calculated temperature field. Last but not least, we showed that the modelling used for the power source has a great impact on the simulation results, even though these parameters are difficult to define.

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