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# Study of the Impedance of the Bypassing Network of a Switching Cell – Influence of the Positioning of the Decoupling Capacitors

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**Abstract**—Mechanisms responsible for ringing and oscillations in power converters at transistors turn-offs are, first, studied using small signal modelling. It is explained why a 50 % derating must be applied to high-speed transistors. Experimental measurements validate the analytical predictions. The influence of the distance between a switching cell and its decoupling capacitors is then studied; it appears that using a low-inductance – though simple – layout results in a stray inductance as low as 11 nH when the capacitor is 30 cm away from the switching cell, enabling degrees of freedom for thermal management.

**Keywords**—bypass, DC-link capacitor, decoupling, GaN transistor, high speed switching, overvoltage, switching cell, switching transient

## I. INTRODUCTION

Wide BandGap (WBG) devices are much faster than their silicon counterparts. Parasitic elements due to layout, connections and to components themselves result in voltage overshoots, oscillations and losses that drive designers to oversize devices – a costly measure. One way to limiting stray inductances consists in placing the devices as close as possible to one another. This, however, may result in poor thermal performances whilst complicating system integration. There is therefore a trade-off between thermal performances, electrical stress, and Electro-Magnetic Compatibility (EMC).

Reaching optimal designs requires a comprehensive and quantitative understanding of this trade-off.

The aim of this paper is two-fold. First, in section II, a simple and linear model of a switching cell is proposed so as to predict turn-off oscillations frequencies and amplitudes. Then, in section III, given a specific layout, the relationship between the loop inductance and the distance between the switching devices and its decoupling capacitors is experimentally studied. Section IV concludes the paper.

## II. OSCILLATION MECHANISMS IN A SWITCHING CELL

### A. Introduction

Many research papers have developed models aiming at predicting oscillations frequencies and amplitudes, either at turn-off [1]–[4] or turn-on [5], [6]. These studies usually model switching loops with ladder linear RLC circuits and current- or voltage- sources. Oscillations are studied either in time- [3], [4], [7]–[9] or frequency- [7], [10] domain.

These models, however, usually require an extensive knowledge of the circuit parasitic elements. Even if this can partly be inferred from simulations, accurate values – and especially damping coefficients in semiconductors – can be difficult to obtain, in particular due to their dependences with frequency, bias and temperature. Similar comments can be made regarding switching times.

So as to avoid the cumbersome and unreliable task of estimating switching times and resistances, the model developed in this paper assumes zero-switching times, i.e. that edges are infinitely steep. The circuit is then studied in a worst-case scenario, resulting in an over-estimation of the oscillations amplitudes. This assumption will nonetheless prove to be quite reasonable when dealing with fast, WBG, devices.

### B. Modelling

#### 1) Introduction

Let us consider (Fig. 1) a switching cell bypassed by two capacitors: a small one,  $C_{X7R}$ , a priori ceramic-based, for local bypassing, and a bulkier DC-link capacitor  $C_{bulk}$ . The circuit is powered by a voltage source  $V_{bus}$  and supplies a load modelled as a current source. Some lumped parasitic inductances are shown in Fig. 1. This figure also highlights three loops that may oscillate:

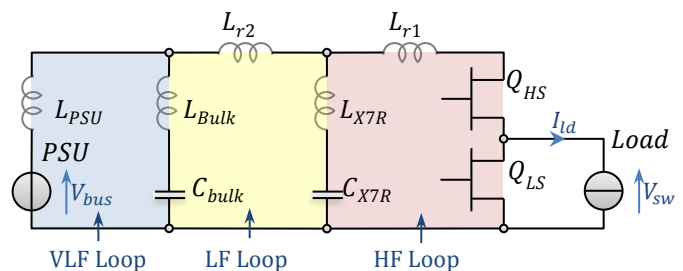


Fig. 1. Schematics of the converter under study: switching cell ( $Q_X$ ), bypass capacitors ( $C_X$ ), parasitic inductances ( $L_X$ ), input voltage ( $V_{bus}$ ) and output load.

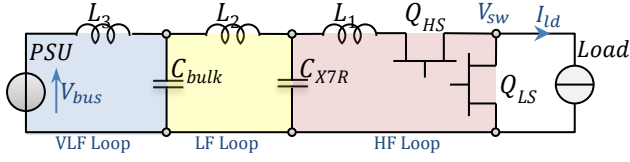


Fig. 2. Simplified schematic of the converter, with parasitic elements

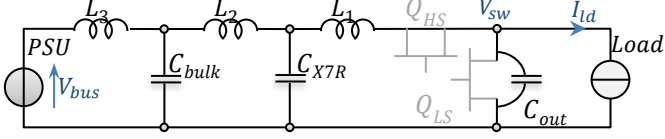


Fig. 3. Converter schematic with  $Q_{LS}$  off and  $Q_{HS}$  on.

- a High Frequency (HF) loop, including the switching cell itself and the local bypass capacitor;
- a Low Frequency (LF) loop, including both capacitors;
- a Very Low Frequency (VLF) loop, including the power source and the DC-link capacitor.

So as to simplify the analysis without losing the relevance of the study for field-use, it is assumed that the parasitic inductances fully decouple the loops: the oscillations can then be studied independently in each loop, which have distinct ringing frequencies and do not interfere. Papers have studied this matter, e.g. [7], [11]. The circuit of Fig. 1 can then be simplified (Fig. 2), were:

$$\begin{cases} L_1 = L_{r1} + L_{X7R} \\ L_2 = L_{r2} + L_{bulk} + L_{X7R} \approx L_{r2} + L_{bulk} \\ L_3 = L_{PSU} + L_{bulk} \end{cases} \quad (1)$$

are the HF, LF, and VLF loop inductances.

Furthermore, the equivalent circuit when  $Q_{LS}$  is off and the load current flows through  $Q_{HS}$  is given in Fig. 3.  $C_{out}$  models the parasitic capacitance of the switching node –  $C_{out}$  is a priori mainly due to the output capacitance of  $Q_{LS}$ . The asymptotic impedance diagram of the network, seen from the load is given in Fig. 4.

Loop capacitances can be defined as:

$$\begin{cases} C_1 = (C_{out}^{-1} + C_{X7R}^{-1})^{-1} \approx C_{out} \\ C_2 = (C_{X7R}^{-1} + C_{bulk}^{-1})^{-1} \approx C_{X7R} \\ C_3 = C_{bulk} \end{cases} \quad (2)$$

The series-resonant frequencies of the HF and LF loops are:

$$f_{r1} = (2\pi\sqrt{L_1C_1})^{-1}, f_{r2} = (2\pi\sqrt{L_2C_2})^{-1} \quad (3)$$

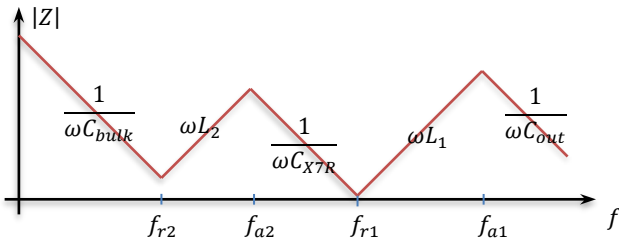


Fig. 4. Asymptotic impedance diagram of the bypass network (Fig. 3), seen from the load.  $L_3 = \infty$ , Log-log scale.

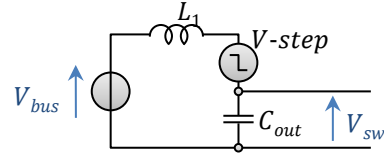


Fig. 5. Simplified converter schematic during the voltage switching.

The parallel-resonant frequencies are:

$$f_{a,i} = (2\pi\sqrt{L_iC_i})^{-1}, \quad i \in \llbracket 1, 3 \rrbracket \quad (4)$$

Assuming that the loops are decoupled was justified since, a priori and due to component sizes:

$$C_{out} \ll C_{X7R} \ll C_{bulk}, \quad L_1 \ll L_2 \ll L_3 \quad (5)$$

This leads to time-domain decoupling of transient phenomena – as will be detailed hereunder.

At  $Q_{LS}$  turn-off (and, more generally, in a hard-switching converter supplying an inductive load, at turn-off) the voltage is switched prior to current. Two transients, a voltage step and then a current one, are therefore generated, leading to oscillations due to distinct mechanisms. The next two subsections describe those mechanisms.

## 2) Voltage switching

During the first phase of the switching, the switching node voltage goes from 0 to  $V_{bus}$ . During this phase, the Low-Side (LS) transistor can be modelled as its output capacitance whereas the High-Side (HS) switch can be modelled as a voltage step going from  $V_{bus}$  to 0. This step will excite the loops one after the other, propagating to the power supply.

During the first instant following the step, before notable oscillations can be observed in the LF loop (i.e. such that  $t \ll f_{a2}^{-1}$ ) and since  $C_{out} \ll C_{X7R}$ , the voltage across  $C_{X7R}$  remains quite constant. The circuit can therefore be simplified as shown in Fig. 5. To put it another way: after the step and before the voltage across  $C_{X7R}$  has had time to notably change, since  $C_{out} \ll C_{X7R}$ , the circuit can be simplified as shown in Fig. 5. The HF loop therefore oscillates at frequency  $f_{a,1}$  and with amplitude  $V_{bus}$ , the voltage  $V_{sw}$  being expressed as:

$$V_{sw} = V_{bus} \cdot (1 - \cos(2\pi f_{a1}t)) \quad (6)$$

The overvoltage is then equal to  $V_{bus}$ . In other word: the peak voltage across  $Q_{LS}$  is twice the input voltage.

The step then propagates to the other loops but with decreasing amplitude, yielding oscillations of negligible amplitudes.

If the quality factor  $Q_1$  of the HF loop was not infinite, one could show that the overvoltage would be given by:

$$\hat{V}_{V,1} = V_{bus} \cdot e^{-\pi/\Lambda}, \quad \Lambda = \sqrt{4Q_1^2 - 1} \quad (7)$$

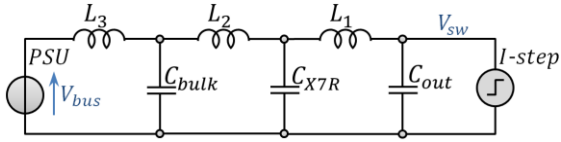


Fig. 6. Equivalent circuit during the current switching.

### 3) Current switching

After the voltage is switched, the current switching occurs. During this transition, the High Side (HS) transistor can then be modelled by a short, the LS one by its output capacitance and the load by a current step – Fig. 6.

The current step will excite resonances, leading to oscillations, in the HF, LF and VLF loops one after the other, propagating from the switching node to the input power supply. Under the assumption that the loops are decoupled, each one can be modelled as a simple circuit with inductance  $L_i$  ( $i \in \llbracket 1, 3 \rrbracket$ , cf. (1)), capacitor  $C_i$  ( $i \in \llbracket 1, 3 \rrbracket$ , cf. (2)), and a current step of amplitude  $I_{ld}$  in parallel. The oscillations have frequencies  $f_{a,i}$  (4) and amplitude:

$$\Delta V_{l,i} = I_{ld} \cdot Z_{c,i}, \quad Z_{c,i} = \sqrt{\frac{L_i}{C_i}}, \quad i \in \llbracket 1, 3 \rrbracket \quad (8)$$

Where  $Z_c$  is the characteristic impedance of loop  $i$ .

### C. Experimental validation

Voltage overshoots were measured on a prototype and compared to predictions from our model. An integrated GaN switching cell (LMG5200, 80 V – 10 A – 15 mΩ<sub>typ</sub>, from TI [12]) was used. It was bypassed by a MKP DC-link capacitor ( $C_{bulk} = 15 \mu\text{F}$ ) together with a X7R-ceramic bypass capacitor ( $C_{X7R} = 1 \mu\text{F}$ ). The supply voltage was set to  $V_{bus} = 30 \text{ V}$ . Typical switching waveforms are given in Fig. 7. Three ringing periods can be seen, corresponding to the three loops: HF loop between 2 ns and 20 ns; LF loop between 100 ns and 2 μs; VLF loop between 2 μs and 20 μs.

The amplitudes of the HF and LF oscillations were measured for various load current values. As shown in Fig. 8, the amplitude of the measured HF oscillations (red squares) do not depend upon the load current  $I_{ld}$  and are very close to the ones predicted by our model for the voltage switching (red line assuming  $Q_1 = \infty$ , yellow line using the measured  $Q_1$  –value). On the other hand, the amplitude of the measured LF oscillations (blue squares) increase linearly with  $I_{ld}$  (fit in blue), with a slope 1.4 Ω – close to the value predicted by our

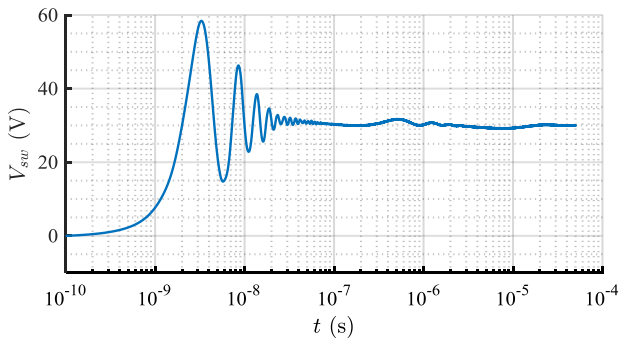


Fig. 7. Measured switching node voltage (zero-padding interpolated). Log. x-scale.

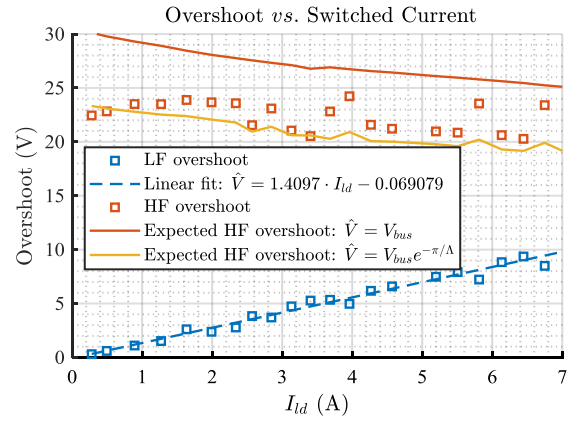


Fig. 8. Measured switching node voltage. Logarithmic X-scale.

model for the current step ( $\sqrt{\frac{L_2}{C_{X7R}}} \approx \sqrt{\frac{22 \text{ nH}}{68 \text{ nF}}} \approx 1.8 \Omega$ ).

It has also been observed that the amplitude and the frequency of LF oscillations have, as expected, a dependence in  $C_{X7R}^{-0.5}$  whereas the HF oscillations do not depend on  $C_{X7R}$ .

As a result, these measurements tend to validate the model developed in this section.

### D. Discussion: on the steep-edge assumption

It has been assumed that edges have zero-rise time, which implies that the edges are fast enough to excite oscillations in the loops. Formally, this means that the bandwidth of the edges, with rise time  $t_r$ , is greater than the loop oscillation frequency  $f_{res}$ . For the HF loop, this can be written:

$$\frac{1}{\pi t_r} > f_{res} \Leftrightarrow t_r < 2\sqrt{C_1 \cdot L_1} \quad (9)$$

For various  $C_{out}$  and loop inductance values, we give in TABLE 1 the maximum rise time so that the assumption is valid. The first three lines correspond to cells using GaN transistors, lines number 2 and 3 are more related to SiC and Si MOSFETs whereas the last one is given for reference, corresponding to a traditional power module. It appears that the switching times calculated are similar to those that can be measured in prototypes, validating the assumption in the case of switching cells using fast, WBG, transistors.

### E. Conclusion

The bypass network of a switching cell is composed of several loops that can oscillate when excited by switching events. A simple model that does not require extensive knowledge on the circuit under study whilst considering fast switching devices was developed. It shows that two mechanisms are involved in the oscillations: voltage and current switching. Both mechanisms yield to voltage

TABLE 1. Maximum rise time so that the steep-edge assumption is valid vs  $(C_{out}, L_1)$ .

$C_{out}$	$L_1$	$t_{r,maxi} = 2\sqrt{C_{out} \cdot L_1}$
100 pF	1 nH	0,63 ns
1 nF	1 nH	2 ns
1 nF	10 nH	6,3 ns
10 nF	100 nH	63 ns

overshoots in the switching loops, with various amplitudes and phase-shifts. Current switching yields oscillations with amplitude proportional to the switched current, whereas voltage switching yields oscillations with amplitude close to the switched voltage – i.e. close to the supply voltage. This last overshoot is highly detrimental since it requires a 50 % derating of the switch voltage rating. Assuming a minimal loop inductance, little can be done to avoid this overshoot but slowing down the switch (e.g. by artificially increasing the gate resistance) or increasing the cell output capacitance.

### III. ON THE INFLUENCE OF THE DISTANCE BETWEEN BYPASS CAPACITORS AND SWITCHING CELLS

#### A. Introduction

Being able to put bypass capacitors at some distance from the switching cell would simplify circuit design and reduce cost. As a matter of fact, it would enable several cells to share decoupling capacitors and heatsinks while loosening thermal constraints. It would also simplify mechanical designs and allow manufacturing circuits with unconventional form-factors.

This study aims at understanding to what extent the distance between a switching cell and its decoupling capacitors can be increased without excessively degrading EMC or increasing either thermal or electrical stress. To this end, the relationship between loop inductance and distance between a switching cell and its decoupling capacitors is studied.

To this end, a switching cell was built its output voltage measured given various decoupling network arrangements.

#### B. Circuit under study

An integrated GaN half bridge (LMG5200, 80 V – 10 A – 15 mΩ<sub>typ</sub>, from TI [12]) was used; dead-times were set to 5 ns. Its power supplied was decoupled by a DC-link capacitor (875 V – 15 μF, MKP, ref. B32678G8156K000 [13]) and a ceramic local bypass capacitor (X7R, 470 nF – 1 kV, ref. 2220Y1K00474KXTWS2). A 70 mm-wide, not terminated, Edge Coupled Microstrip transmission line was used between the capacitor and the switching cell. The distance between the decoupling capacitors and the cell are  $d_{bulk}$  and  $d_{X7R}$  (Fig. 9). The circuit was manufactured using the top-copper layer of a 35/370/35 μm-thick FR4-based PCB, the bottom copper layer being used as a ground plane. The circuit was powered by a voltage source  $V_{bus} = 30$  V. It was used in a double pulse test, supplying a broadband inductive load with a current  $I_{ld} = 5$  A.

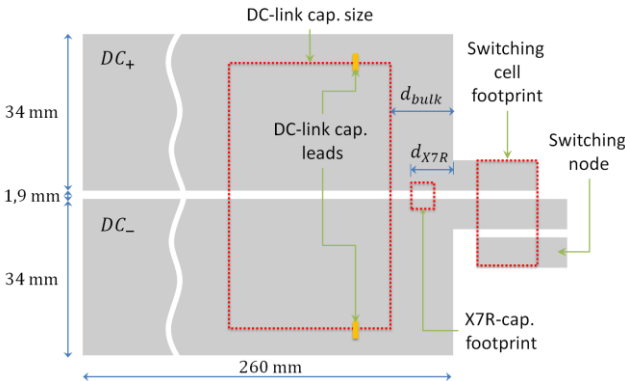


Fig. 9. Simplified circuit layout (bottom layer ground plane not shown).

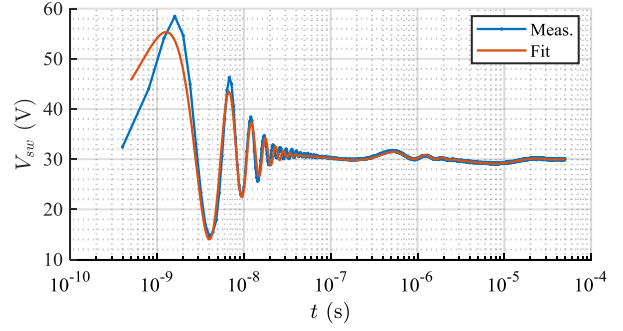


Fig. 10. Typical switching waveform: measurement (blue) and fit (red).  $n_L = 3$ . Logarithmic X-scale.

#### C. Measurement method

The switching node voltage was measured using a Teledyne-Lecroy HDO8108 oscilloscope (12 bit, 1 GHz, 2.5 GSa/s) and a PP008 10:1 passive voltage probe (500 MHz, 10 MΩ//9.5 pF), connected to the circuit with an ad-hoc, low-inductance setup [11].

The capacitances  $C_{out}$ ,  $C_{bulk}$  and  $C_{X7R}$  were measured using an E4990a impedance analyser, at 100 kHz and at 30 V biasing voltage:

$$C_{X7R,30V_{dc}} = 447 \text{ nF}, \quad C_{bulk,30V_{dc}} = 14.88 \text{ μF}, \quad (10)$$

$$C_{out,30V_{dc}} = 571 \text{ pF}$$

A model describing the oscillations of  $n_L$  loops:

$$V_{sw}^* = V_{dc} + \sum_{k=1}^{n_L} \hat{V}_k \cdot \sin(\omega_k t + \phi_k) \cdot e^{-t/\tau_k}, \quad (11)$$

$$\beta = [V_{dc}, \hat{V}_k, \omega_k, \phi_k, \tau_k]_k$$

was then fitted on the measurements, the vector  $\beta$  being used as fitting parameter. The  $\omega_k$  and capacitances values were then used to estimate the loop inductances using Thomson's formula [14], (3)-(4).

Model (11) appeared to be a good fit for the measurements (Fig. 10), the capacitances nonlinearities having limited impact on the result.

#### D. Loop inductance

##### 1) LF Loop

The effect of the distance  $d_{bulk}$  between the switching cell and the DC-link capacitor on the LF loop inductance was studied at  $d_{X7R} = 0$  (Fig. 11). As expected,  $L_2$  increases with  $d_{bulk}$ , due to the increase of the loop area. The rise is however very slow since it is limited to 18 nH (+64 %) when

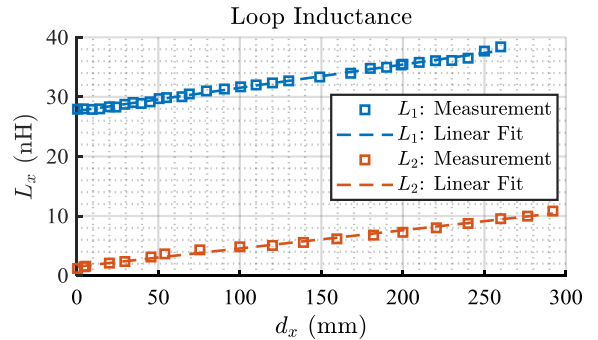


Fig. 11. HF loop inductance ( $L_1$ ) vs.  $d_{X7R}$  and LF loop inductance ( $L_2$ ) vs.  $d_{bulk}$ .

$d_{bulk}$  goes from 0 to 260 mm. Furthermore, the capacitor self-inductance (ESL:  $L_{bulk} = 18.4$  nH) accounts for up to 66 % of the overall loop inductance.

## 2) HF Loop

The DC-link capacitor having been removed from the circuit (i.e.  $d_{bulk} = \infty$ ), the impact of  $d_{X7R}$  on the HF Loop inductance was studied (Fig. 11). These measures show that the smallest achievable inductance is 1.2 nH and that the increase of  $L_1$  vs.  $d_{X7R}$  is very slow: 0.3 nH/cm.

The HF loop inductance is then only 11 nH when the switching cell is 30 cm away from its bypass capacitor.

## E. Small signal measurements

Another prototype was manufactured, with layout similar to the first one but incorporating a factice switching cell, with  $Q_{LS}$  replaced by its output capacitance and  $Q_{HS}$  shorted. The impedance seen from the load was then measured using an E4990a impedance analyser (stimuli amplitude: 500 mV, no bias). The linear model from Fig. 3 was then fitted on the measurements.

The measured inductances were in good agreement with those obtained with the first prototype. In particular the same slope of 0.3 nH/cm was found. Though, an offset due to the use of a factice switching cell, with geometry different from that of the real one, was found.

## F. Conclusion

This study dealt with the influence of the distance between a switching cell and its decoupling capacitors.

As expected, minimising inductances requires to put components as close to one another as possible. However, this study showed that the simple layout we used made loop inductances little sensitive to the distance between the cell and the decoupling capacitors.

Using a thin and grounded PCB is of primal importance to limit loop inductances. Furthermore, a capacitor's ESL can account for a major part of the overall loop inductance.

This study shows that, using the layout under study, the loop inductance sensitivity to the distance between a switching cell and its decoupling capacitors is rather low (about 300 pH/cm). Additionally, it showed that the DC-link capacitor can be placed quite far from the cell. These results highlight the relative freedom designers have regarding the arrangement of the components of a switching cell and its bypass network, thus facilitating, in particular, thermal design.

## IV. CONCLUSION

The first part of this study shows that, for devices with fast enough switching speeds, two mechanisms must be considered to predict oscillations. The first one results in an overvoltage that is as high as the full bus voltage  $V_{bus}$  whereas the other one induces an overvoltage of amplitude proportional to the load current.

The distance between the switching cell and its decoupling capacitors was then varied and the resulting stray inductance was measured both in frequency- and time-domains, using either an impedance analyser or an oscilloscope. The results show that the stray inductance remains rather low ( $< 11$  nH) even when the capacitor is far away from the switching cell (30 cm). Furthermore, the

sensitivity of this inductance vs. the distance is very low: about 0.3 nH/cm. Choosing a capacitor with low self-inductance (ESL) is therefore most important so as to limit the overall loop inductance. Constrains on the compactness may then, in some cases, be loosen so as to improve thermal management and system integrability.

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