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Realization of a monolithic multi-terminal Si-power chip integrating a 2-phase rectifier composed of vertical PiN diodes insulated by vertical P⁺ walls

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Abstract

This paper is within the context of mixed monolithic/hybrid integration of a generic multi-phase power converter (DC/AC or AC/DC). The technological results provided in this paper deal with the realization of a 300 μm deep P⁺ wall as well as with the realization of the monolithic 2-phase rectifier that consists of four vertical PiN diodes that are separated by P⁺ walls. These technological results are currently in use for the realization of a three terminal common cathode chip consisting of two RC-IGBTs as well as a monolithic H-bridge converter that consists of four RC-IGBTs.

Keywords

« Monolithic integration », « RC-IGBT », « multi-terminal Si power chip », « multi-phase Inverter »

Introduction

In the field of power conversion in power electronics, power modules are generally composed of diodes as well as IGBT chips. These chips are interconnected to each other and to the outside of the module using wire bonds. Wire bonds require an expensive wiring operation and are source of reliability problems [1]. Moreover, the stray inductance of wire bonds limits the frequency of operation of the power module [2]. The reduction of the number of chips in the module through monolithic integration is an interesting approach in order to minimize or eliminate wire bonds. The monolithic integration of the diode and the IGBT allowed the development of the RC-IGBT [3] that aims at replacing the association of two discrete chips by a single RC-IGBT chip. Consequently, the number of wire bonds in a power module can be reduced. At the converter level, the authors have already proposed two integration approaches: two-chip (Fig. 1) and single chip integrations (Fig. 2) [4-6]. The technological realization of some multi-terminal power chips requires the realization of a P⁺ vertical wall at the beginning of the process flow. In this paper, the technological realization of a 300 μm P⁺ deep wall is detailed. Then, this latter is integrated in a two-phase rectifier power chip that integrates monolithically four vertical PiN diodes.

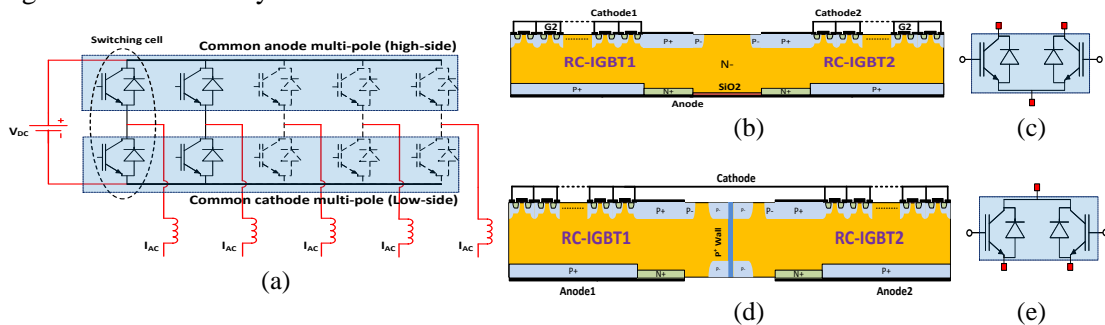


Fig. 1: (a) Multiphase converter, (b) cross-sectional view of the monolithic three-pole power chips [4-6]: (a) common anode structure (high-side) and (c) equivalent circuit, (d) common cathode structure (low-side) and (e) equivalent circuit.

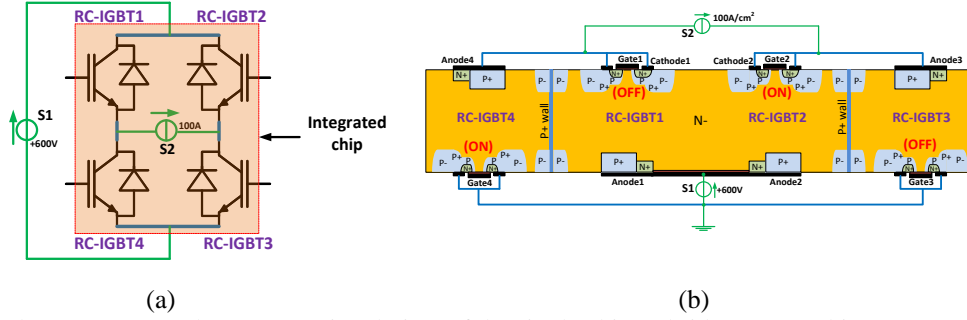


Fig. 2: (a) 2-phase converter, (b) cross-sectional view of the single chip H-bridge power chip [4-6] composed of four RC-IGBTs.

2D architecture of the 2-phase rectifier power chip

Fig. 3 gives a cross-sectional view of the integrated 2-phase rectifier. This multi-terminal chip derives from the single-chip H-bridge given in Fig. 2(b). The high-side two diodes of the rectifier are placed at the center of the chip and surrounded by a P^+ wall. Each of the two low-side diodes is placed on one side and surrounded by a P^+ wall.

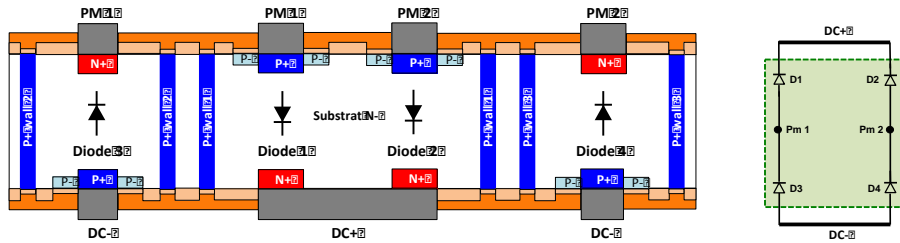
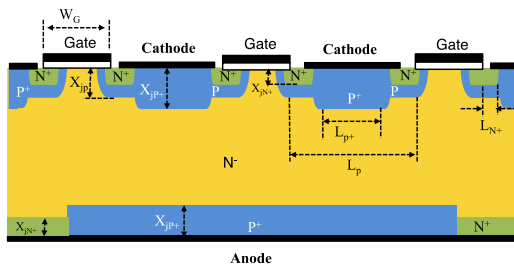


Fig. 3: Cross-sectional view of the simulated and realized 2-phase rectifier.

2D SentaurusTM simulations of the 2-phase rectifier power chip

The proposed chip is studied using 2D TCAD SentaurusTM simulations. The active area of each diode section in Fig. 5(a) is 1 cm^2 . The monolithic chip has to support the applied voltage both vertically and laterally, and to carry a current of 100 A. For illustration purposes, Fig. 4 shows a cross sectional view of the RC-IGBT chip and the main diffusion regions parameters of the IGBT technology process of the LAAS micro and nanotechnology platform. This process flow is used for the realization of the multi-terminal monolithic chip given in Fig. 3. Minority carrier lifetimes $\tau_{n0} = 5 \text{ } \mu\text{s}$ and $\tau_{p0} = 3 \text{ } \mu\text{s}$ were used in 2D simulations.



Symbol	Parameter	value	Doping concentration
W_G	Gate width	30 μm	
e_{ox}	Gate oxide thickness	55 nm	
L_p	P diffusion width	48 μm	$2,5 \times 10^{17} \text{ cm}^{-3}$
X_{jp}	P diffusion depth	5 μm	
L_{p+}	P+ diffusion width	26 μm	$5 \times 10^{19} \text{ cm}^{-3}$
X_{jp+}	P+ diffusion depth	7 μm	
L_{N+}	N+ diffusion width	18 μm	10^{20} cm^{-3}
X_{jN+}	N+ diffusion depth	1 μm	

Fig. 4: Schematic cross-sectional view of the RC-IGBT chip and the geometrical parameters used in 2D simulations.

The simulation conditions are given in Fig. 5(a). A 300 V DC-voltage source is connected between DC+ and DC- and a DC-current source of 100 A is connected between PM1 and PM2 electrodes. As shown in Fig. 5(b), a space charge region expands on both sides of the reverse biased P/N- junctions in diode1 and diode4. The separation distance between diode1 and diode2 sections used in these simulations is $d = 1 \text{ mm}$. The current density distribution in the structure is given in Fig. 5(c). Diode2

is in ON-state while diode1 is in OFF-state. The load current flows through diode2 section. The leakage current through the OFF-state section is negligible ($16 \mu\text{A}$).

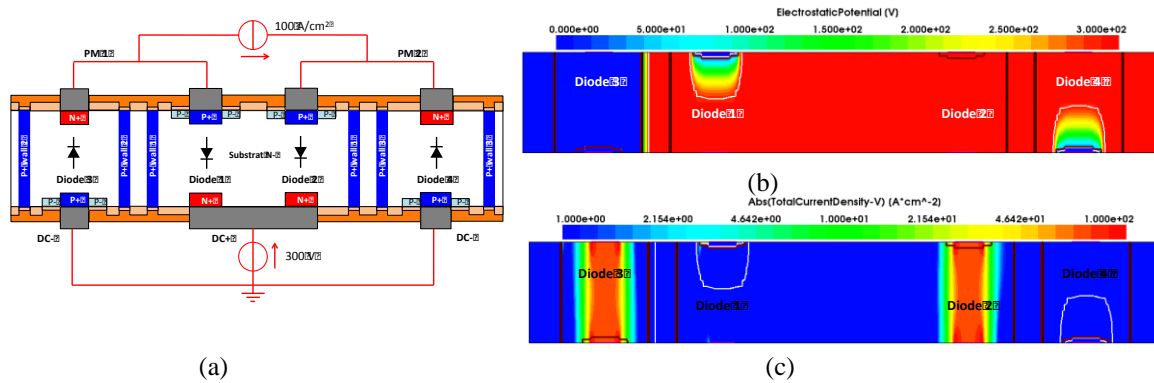


Fig. 5: SientaurusTM mixed-mode simulation results: (a) simulation conditions, (b) equipotential lines distribution in the off-state diode sections, (c) current density distribution in the on-state diode sections ($V_{\text{BUS}} = 300 \text{ V}$, $J = 100 \text{ A/cm}^2$).

Realization of the 2-phase rectifier power chip

The first realizations of the P^+ wall were carried-out by [7-8]. The P^+ wall allowed endowing the IGBT with symmetrical voltage capability. The P^+ wall is $300 \mu\text{m}$ deep. In this paper, numerous tests were carried-out in the micro and nanotechnology platform of LAAS in order to determine the dimensions of the openings and spacing between each two adjacent openings of the mask shown in Fig. 6. Moreover, solutions were proposed to improve the quality of trench filling with highly boron doped polysilicon. The deep etching of the trenches in silicon starts first by etching a thick oxide layer ($0.8 \mu\text{m}$) and then etching of a deep trench ($300 \mu\text{m}$). To that end, a thick photo-resist layer ($40 \mu\text{m}$) AZ40XT is used. Oxide etching is carried-out in a plasma etching system (ICP-RIE Omega 201). A CF_4 gas is used. The deep silicon etching is achieved in another system (Alcatel AMS 4200). SF_6 etching plasma is used for etching silicon and C_4F_8 is used for passivation. Two hours of etching time were required to realize a $300 \mu\text{m}$ deep and narrow trench. An important number of tests were necessary in order to set up the parameters necessary for a correct trench filling using boron doped polysilicon. The chemical vapor deposition of highly boron doped polysilicon is achieved in a vertical reactor developed at LAAS [8]. It allows a high speed polysilicon deposition ($2 \mu\text{m/h}$). Fig. 7(c) shows a SEM image after trench filling. One can notice that the trench is correctly filled from the front-side down to the backside. Indeed, as compared to the classical filling technique (Fig. 7(b)), the realized P^+ wall given in (Fig. 7(c)) does not contain micro-cavities.

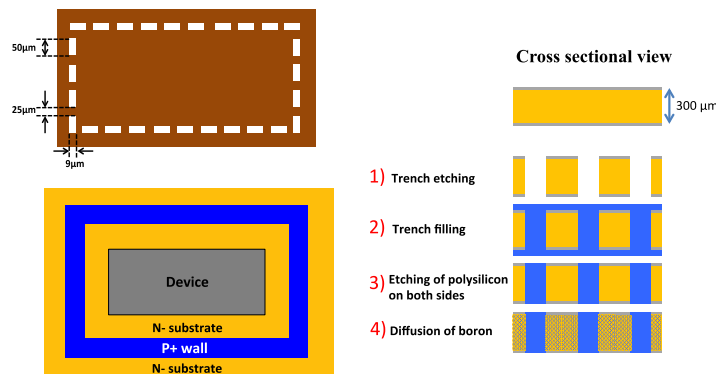


Fig. 6: Top view of the used mask and main steps for the realization of the P^+ wall.

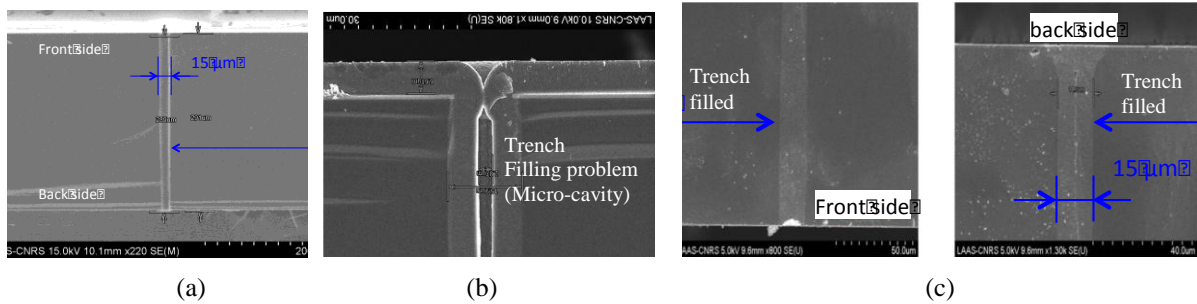


Fig. 7: (a) SEM view of the deep trench realized using DRIE etching (300 μm), (b) Highlight of the trench filling problem with the classical filling technique, (c) SEM image of a correctly filled trench with highly boron doped polysilicon (no micro-cavities in the P^+ wall).

At this stage the silicon wafer integrates the trenches filled with polysilicon. The wafer is also covered with polysilicon on both sides. It is therefore etched on one side then on the other as shown in Fig. 8. This was carried-out in the same etching system used previously for deep etching of silicon (AMS 4200). The thickness of the polysilicon layer on each wafer side is about 8 μm .

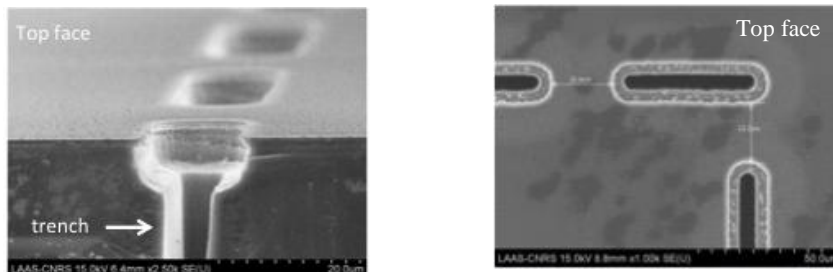


Fig. 8: (a) SEM view after polysilicon layer etching.

After the realization of the P^+ wall, another complexity concerns the alignment of the remaining IGBT process steps with respect to the P^+ wall. The first step that follows the P^+ wall is the junction termination P^- . The alignment masks are shown in Fig. 9. Fig. 9(a) shows the mask used for the P^+ wall while Fig. 9(b) gives the mask for the P^- region. Fig. 9(c) shows the alignment of the P^- region with respect to the P^+ wall and Fig. 9(d) shows the realized pattern. Once the P^- is aligned with respect to the P^+ wall, the remaining steps of the process flow will be aligned with respect to the P^- region as in the classical IGBT process.

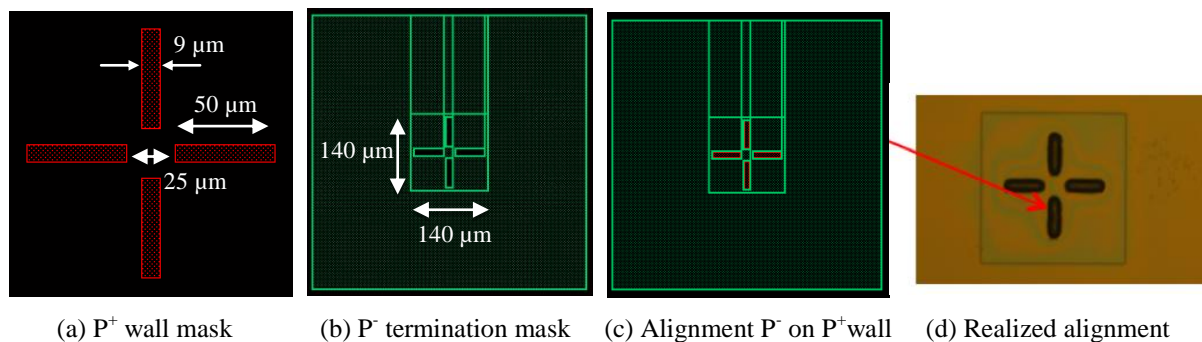


Fig. 9: Masks used for the aligning the P^- diffusion with respect to the P^+ wall.

Once the P^+ wall technology step is integrated in the IGBT process-flow, the monolithic 2-phase rectifier is realized. Fig. 10 gives an overview of the masks used for the realization of the monolithic 2-phase rectifier. The technological realization of the rectifier chip requires 13 mask levels. Fig. 11 shows the realized silicon chips. Three terminal common cathode chip as well as 2-phase rectifier power chip were realized.

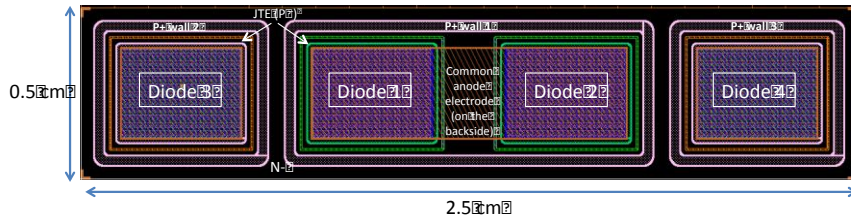


Fig. 10: Overview of the masks used for the realization of the 2-phase rectifier chip.

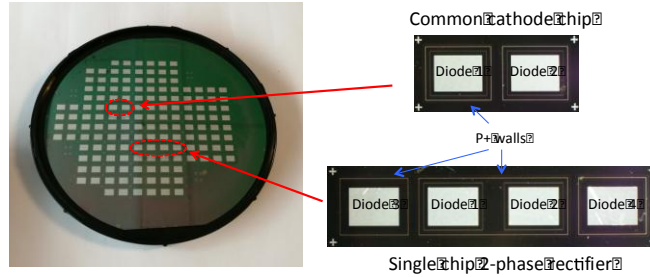


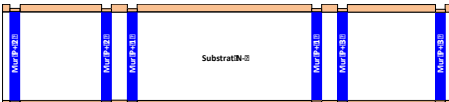
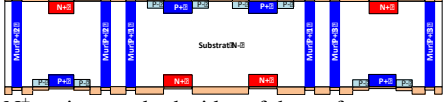
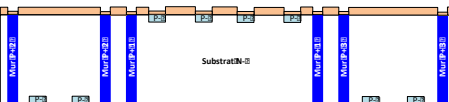
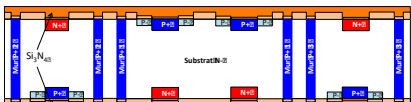
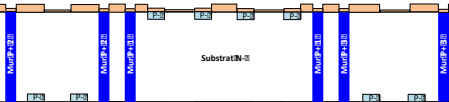
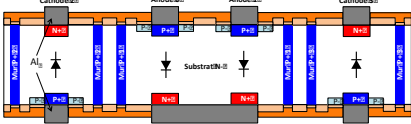


Fig. 11: Top view of the realized silicon wafer integrating the two-phase rectifier chips.

Table. 1 summarizes the different steps of the technology process used for the realization of the 2-phase rectifier chips. This process is mainly composed of 8 steps.

Table. 1: Main steps of the process for the realization of the 2-phase rectifier power chip

Step 1 : Thick oxide layer	Step 5: P ⁺ regions
 <p>The oxide layer of 800nm thick allows to protect the wafer surface during the whole process.</p>	 <p>The P⁺ regions were realized on both sides of the wafer to realize the anode regions of the diodes.</p>
Step 2 : P ⁺ wall realization	Step 6: N ⁺ regions
 <p>This step is detailed previously.</p>	 <p>The N⁺ regions on both sides of the wafer to create the cathode regions of the diodes.</p>
Step 3 : P ⁺ junction termination	Step 7: Deposition of Si ₃ N ₄ layer
 <p>The P⁺ junction termination regions in front side then in backside.</p>	 <p>The silicon nitride layer is deposited on both sides of the silicon wafer.</p>
Step 4: Active region opening	Step 8: Metallisation - electrodes
 <p>The 800 nm thick oxide is etched in areas where P⁺ and N⁺ implantations will be realized.</p>	 <p>The silicon nitride is etched and electrodes realized.</p>

Conclusion

The technological realization of compact multi-phase static power converters proposed by the same authors in the context of the mixed monolithic/hybrid integration of power converters require the use of an insulation region between RC-IGBT sections that share the same silicon chip. In the proposed approaches, electrical insulation using P⁺ wall is used. As a step towards the realization of the proposed power converter chips, we have set-up the parameters required for the realization of the P⁺ wall. The developed technique allows to improve the filling of the realized 300 μm deep P⁺ walls. Indeed, the realized P⁺ walls do not contain micro-cavities. We have then realized monolithic three terminal common cathode chips composed of two diodes and separated by a P⁺ wall as well as a single power chip integrating a 2-phase rectifier consisting of four PiN diodes that are separated by P⁺ walls. We are currently using these technological results for the realization of the proposed three terminal common cathode chip consisting of two RC-IGBTs as well a monolithic H-bridge converter that consists of four RC-IGBTs and separated by P⁺ walls.

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