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SiC Power Mosfet in Short-Circuit operation : ELECTRO-THERMAL MACRO-MODELLING COMBINING PHYSICAL AND NUMERICAL APPROACHES WITH CIRCUIT-TYPE IMPLEMENTATION

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Abstract – The purpose of this paper is to describe, for the first time, a global transient electrothermal model of (SiC) power MOSFETs during accidental short-circuit (SC) operations. The developed models allow to analysis an inverter-leg malfunctioning. A thermal model of the SiC MOSFET dies combined with extensive experimentations allow to develop models of the gate leakage current and of the drain saturation current during SC events. After verifying the robustness of the proposed elementary models, an original global circuit model with an easy implementation using a commercial circuit simulation tool is proposed and discussed. This circuit model can be used in order to develop protection schemes against SC faults.

Keywords – electrothermal simulation; model validation; MOSFET; short-circuit; silicon carbide.

1. INTRODUCTION

Nowadays, due to mass production from major manufacturers, SiC power MOSFET is gradually used in several power applications such as inverter for PV panels and grid, UPS and railway traction drive. In that kind of applications, short-circuit (SC) faults can appear leading to large transient power dissipation and a dramatic risk of failure. Examples of these faults-types are described on Fig. 1.

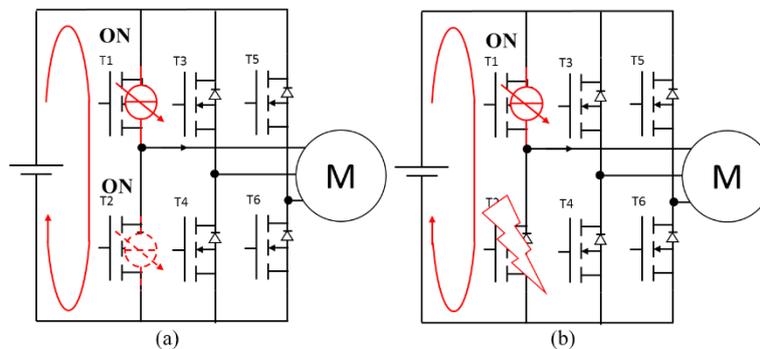


Fig. 1. (a) inverter-leg cross-conduction by faulty control signals (Type I SC). (b) Internal short-circuit by electrical breakdown of one of the two leg-switches (Type II SC).

In order to develop a dedicated fast and robust protection against these faults, studies on the ruggedness of SiC MOSFET under short-circuit have been carried out [1-3]. Nevertheless, until now, none electro-thermal models globally and accurately describe SiC power MOSFET behaviours under SC faults. Particularly, the gate-leakage current increases significantly during short-circuit, as depicted in Fig.3, and the saturation current evolution is unusual compared to silicon (Si) devices. Indeed, SiC material can support much higher junction temperature leading to behaviour that cannot be seen in Silicon at these temperature such as high temperature Fowler-Nordheim tunnelling [4] or high change in the channel mobility [5]. The significant gate-leakage current observed during the SC can directly affect the gate-voltage control of the device through the voltage drop across the gate driver resistor. Whatever the failure mode resulting of a SC event (failure of the gate with a short-circuit between gate and source or failure between drain and source after thermal runaway), the estimation of the critical energy capability and the corresponding junction temperature in short-circuit mode are necessary in order to determine the maximum delay time of the gate drive protection to be implemented.

The goal of the proposed study is to develop a new global and macro-model of SiC power MOSFETs. We focus in this paper on a particular device from ROHM™ (SCT2080KE) but the methodology and the model can be easily transposed to other devices from different manufacturers. Emphasis has been put on finding and fitting accurate models for transient gate leakage current (I_G) during the SC phase, drain saturation current (I_{Dsat}) and threshold voltage ($V_{GS(th)}$) according to complex and several parameters, particularly using estimated maximum junction temperature (T_j) at the top of the die. The original contribution of this paper to the classical MOSFET model is highlighted in Fig. 2. During SC events, large value of drain to source voltage and very large value of drain saturation current lead to a very large dissipated power density in the die resulting in a very fast increase of the junction temperature. A thermal model is developed and used in order to estimate the junction temperature during the SC event and then to develop models of the transient gate leakage current (I_{Gleak}) drain saturation current (I_{Dsat}) and threshold voltage ($V_{GS(th)}$).

Combining the gate-current and drain saturation current behaviour, the aim of this paper is to present how the electro-thermal modelling methodology of a SiC MOSFET under extreme stress has been built and evaluated for a practical use. In Section 2, after an introduction, a first dipole-type gate-leakage current model function of four different parameters (dissipated energy, gate driver output-voltage eq. to V_{buffer} , gate resistance and drain to source voltage) is developed and presented. In Section 3, a 1D estimation model of the temperature distribution inside the chip is described. In Section 4, based on the results from this estimation, a physical model is fitted in order to precisely represent the drain saturation current evolution during the SC phase. Finally, in Section 5, simulations and robustness of the global behaviour, using PLECS software, are presented and compared with experimentations.

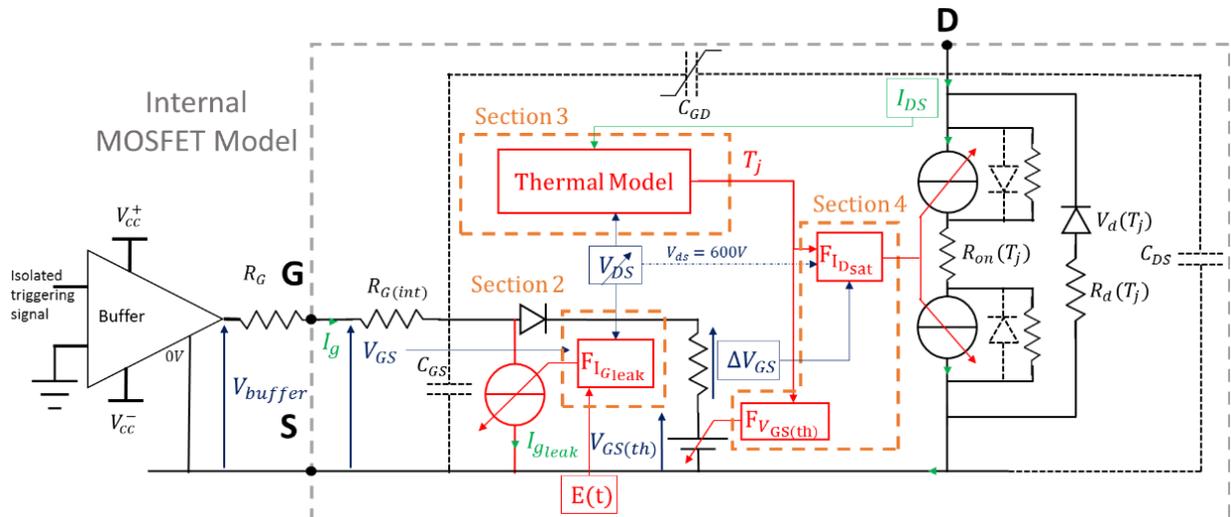


Fig 2. Enhanced electro-thermal SiC MOSFET circuit-type modelling. In black line, the classical MOSFET model. In red line, new features proposed in this article for short-circuit operation.

2. GATE-LEAKAGE CURRENT MODELLING

2.1. MODEL DETERMINATION

After few micro-seconds of short-circuit, a great transient current surge appears across the thin MOSFET gate oxide (typically a thickness close to 50nm). This current is most likely caused by a highly temperature dependent Fowler-Nordheim tunneling effect [3] considering the important energy dissipated inside the chip (up to 10J/cm² in 12μs) combined with a great electric field (higher than 400V/μm) applied between the polysilicon-gate and the SiC substrate of the device through the SiO₂ gate-oxide. However, the SC duration is much lower than the thermal time constant of the component die ($\tau_{die} \cong 350\mu s \gg \tau_{SC} = 12\mu s$). In these conditions, only the die will be considered by the

temperature increase during SC events and dissipated energy can be considered instead of the junction temperature in order to explain the time dependence of the gate leakage current during SC. Furthermore, as depicted in Fig.3a, 3d, the gate-leakage current dynamic also depends on the gate voltage bias imposed by the gate-driver ($V_{\text{buffer(ON/OFF)}}$), the drain to source voltage (V_{DS}) and the external gate resistor (R_{G}) (not displayed). The aim of this section is to explain how the influence of each parameter has been identified and modelled. In order to reduce the complexity of the study, only the gate current increase, along the sequence n°3 in Fig. 3, is accurately modelled. As a result, the surge occurs from a fixed energy (0.8J or 5.9J/cm² of active chip area for all measurements as presented in Fig 3c) so the model will be valid from this value only. In practice, this threshold energy of the gate-stress represents a value close to the half of the failed critical energy of the device. For the other parameters, the model validity has to be large: $V_{\text{DS}} \in [400\text{V}, 600\text{V}]$, $V_{\text{buffer(ON)}} \in [18\text{V}, 21.5\text{V}]$, Energy $\in [0.8, 1.5\text{J}]$. A “dipole-type” model has been chosen (Fig.2) as an equivalent non-linear controlled current-load F_{IGleak} between gate and source electrodes supplied by the driver voltage. This source is made of a voltage source (V_{buffer}) and a series gate resistor (R_{G}).

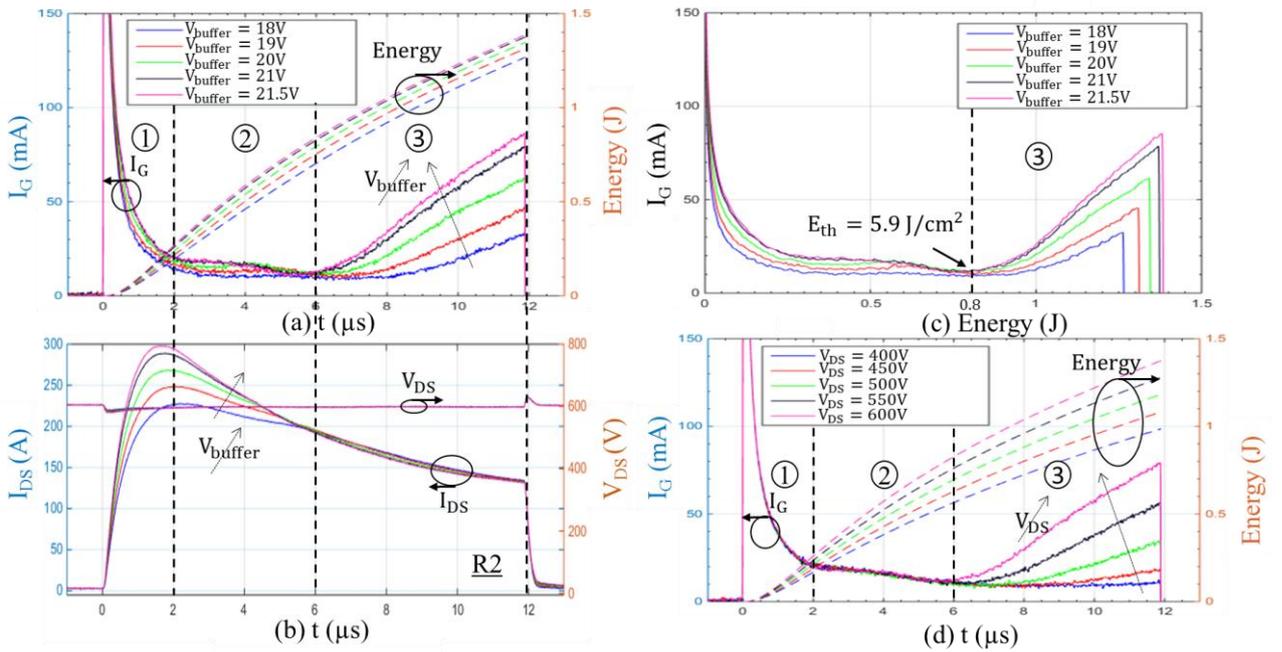


Fig. 3. Experimental waveforms, from a lab. . set-up, during type-I SiC MOSFET short-circuit. (a) gate-leakage current and dissipated energy inside the chip. (b) drain current during SC (saturation current) and drain-source voltage. (c) $I_{\text{GS}}(E)$ for $\neq V_{\text{buffer(ON)}}$, $R_{\text{g}} = 47\Omega$ & $V_{\text{DS}} = 600\text{V}$. (d) $I_{\text{GS}}(t)$ for $\neq V_{\text{DS}}$, $R_{\text{g}} = 47\Omega$ & $V_{\text{buffer(ON)}} = 21\text{V}$.

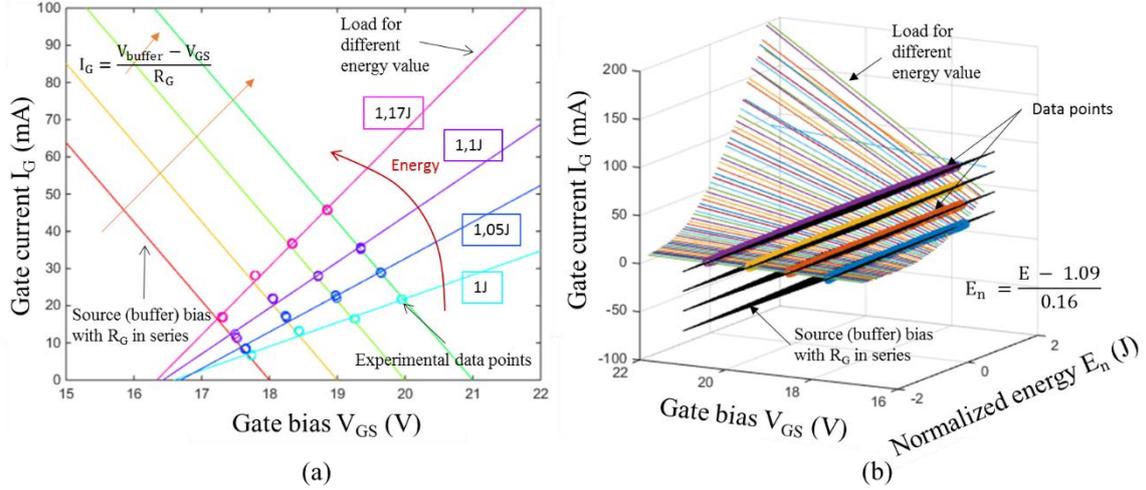


Fig. 4. Measured data points at the intersection between the driver characteristic and the equivalent current-load characteristic I_{IGleak} (a) in the plane (I_G, V_{GS}) (b) in the space (I_G, V_{GS}, E_n) for $R_G=47\Omega$, $V_{DS}=600V$ and different dissipated energy values.

On Fig. 4a are plotted current-load equations for four different buffer voltages, 18, 19, 20 and 21V. Different experimental points are also plotted on this figure (circles). For each buffer voltage, for points of identical dissipated energy (1, 1.05, 1.1 and 1.17 J) have been reported. It is remarkable that for a given energy and different buffer bias a load straight line, as a perfect ohmic behavior, is clearly identifiable and is significantly energy (temperature) dependent. In order to analyse the energy influence on the current-load equation, load straight lines are displayed in 3D representation (I_G, V_{GS}, E_n) in Fig.4b. This representation is basically the same as depicted in Fig.3. But the load characteristic of the gate driver can be visualised as a surface. Therefore, a polynomial surface (1) has been chosen and fitted with MATLAB™ to model the current-load variation function of V_{GS} and the dissipated energy (E_n) on the validity area of the model.

$$I_g = a_1(E_n) \cdot V_{GS} + a_2(E_n) \quad (1)$$

With

$$a_1(E_n) = p_{01} + p_{11}E_n + p_{21}E_n^2 \quad (2)$$

$$a_2(E_n) = p_{00} + p_{10}E_n + p_{20}E_n^2 + p_{30}E_n^3 \quad (3)$$

(p_{00}, p_{01}, \dots) are the estimated factors.

This "response surface" approach has two main advantages. On one hand, MATLAB™ polynomial surface fitting algorithm from the *fit* function is powerful and robust. On another hand, the polynomial function and dipole-type model makes it easily computable and to be embedded into a commercial-type software. At this point, the model represents effects of V_{buffer} , R_G and E_n on the gate leakage current value.

However, V_{DS} variation, in Fig. 3d, is not yet added in the model. To do that, factors (p_{00}, p_{01}, \dots) are, themselves, estimated for different V_{DS} bias and pre-calculated in a table. It appears that these factors are linearly varying with V_{DS} . Finally, the variation has been estimated and added to the model. The parameters value can be found in Table I.

I. Estimated factors function of V_{ds}

p_{00}	$174.2161 - 0.5505 \cdot V_{ds}$
p_{10}	$192.8417 - 0.5720 \cdot V_{ds}$
p_{01}	$-11.8436 + 0.0356 \cdot V_{ds}$
p_{20}	$52.8609 - 0.1482 \cdot V_{ds}$

$p11$	$-13.7143 + 0.0386.V_{ds}$
$p30$	$-0.9317 + 0.0026.V_{ds}$
$p21$	$-4.1480 + 0.0111.V_{ds}$

2.2. RESULTS

The model has been estimated with experimental data from the component SCH2080KE from ROHM™. In order to determine the model robustness, two different tests were made. The proposed model was first compared with new experimental results which are different from those used for the model fitting (Fig. 5a). In a second step, the proposed model was compared with data obtained from another component SCH2080KE, i.e. for new experimental results (Fig.5b). Moreover, the model can be easily adapted for other SiC MOSFET components from Rohm or other manufacturers. Indeed, in Fig. 5c, the model parameters has been estimated with experimental data from the component C2M0080120D from Wolfspeed™. The simulation results are, in each case, very close to the experimental data. In conclusion, these results clearly validate the proposed numerical model and show its robustness in its full domain of validity.

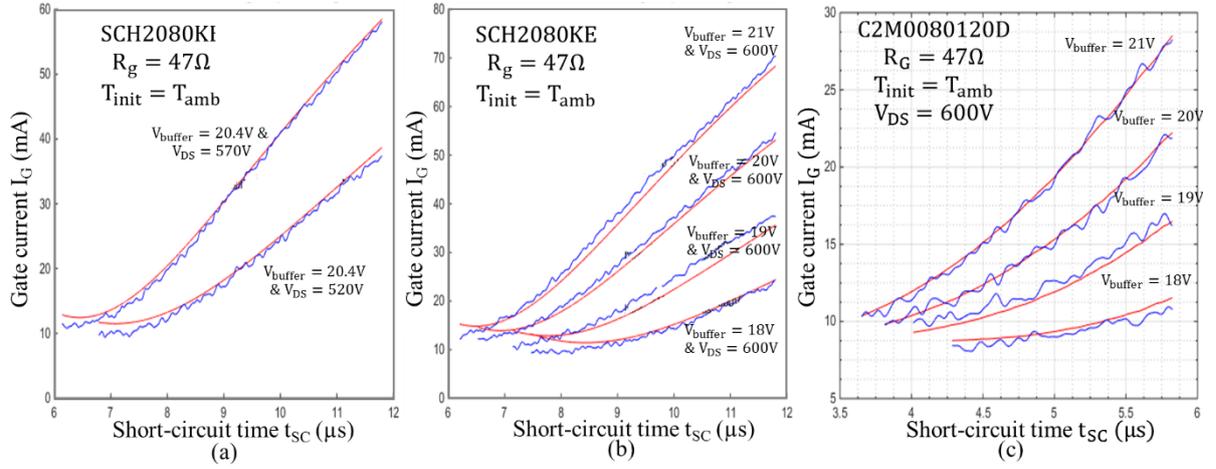


Fig. 5. Model output (red lines) and experimental results (blue lines) of the gate leakage current evolution during SC. (a) Robustness results and validation obtained from test data which are not used for the model fitting but with the same device. (b) Robustness results and verification obtained from test data not used for the model fitting and with another device of the same reference. (c) New fitting results obtained with data used for another reference component C2M0080120D

3. TEMPERATURE ESTIMATION

3.1. MODEL CONSTRUCTION

During a short-circuit event, strong electrical field is distributed along the low doped epi-layer and a strong current density flows through the chip. This particular configuration induces a high and fast transient temperature gradient inside the chip within few micro seconds. With encapsulated components, the temperature gradient is not measurable in real time because the external case temperature do not represent the junction temperature of the chip [6]. In order to fit physical models function of the temperature, such as dependant electron mobility or threshold voltage, an accurate temperature estimation is needed. All these physical models are required in order to model the drain saturation current during the SC. Moreover, the thermal model must be accurate and low simulation time consuming. To do that, the best compromise is a one dimensional transient thermal model across the chip depth [2]. Two models were developed: a “simple model” with fast computation time (Fig. 6a) designed to be embedded into a circuit simulation tools named PLECS™ and a more complex model developed in order to simulate more finely the thermal physical effects (Fig. 6b).

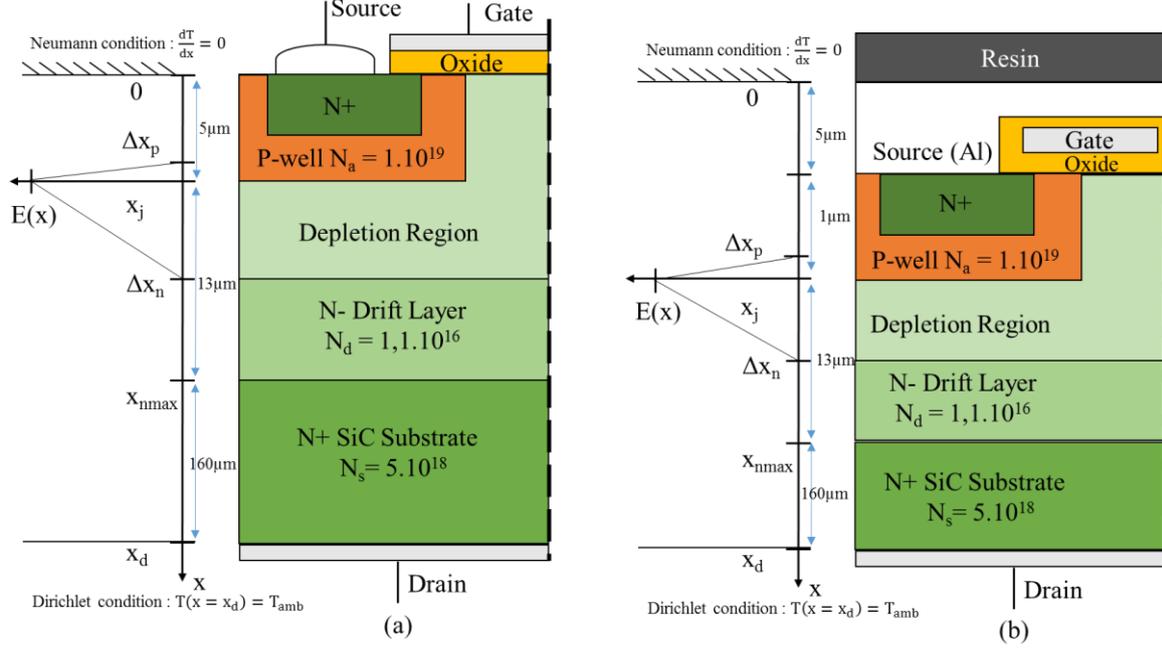


Fig. 6. 1D thermal model of the SiC MOSFET (a) first thermal model with only SiC material and physical parameters not thermally dependent (b) 2nd model with aluminum on top, and physical parameters thermally dependent.

3.1.1 Model construction common to the two models

During short-circuit transient, the dc bus voltage, V_{DC} , is applied across the power device and leads to depletion layers with a width x_p in the P-well (highly doped N_a) and x_n in the N-drift region (low doped N_d). The resulting electric-field distribution in the space charge region is given by the integration of the Gauss' law as described in [2] as an example, neglecting the effect of the current, i.e. the charge displacement on the depleted charges.

$$E(x) = \frac{qN_a}{\epsilon_s} (x + \Delta x_p - x_j) \text{ for } x \in [x_p, x_j] \quad (4)$$

$$E(x) = -\frac{qN_d}{\epsilon_s} (x - \Delta x_n - x_j) \text{ for } x \in [x_j, x_n] \quad (5)$$

$$E(x) = 0 \text{ for } x \in [0, x_p] \cup [x_n, x_d] \quad (6)$$

Where ϵ_s is the total dielectric constant for 4H-SiC material and q is the electron charge. V_{DS} is the electric field integral along the space dimension.

$$V_{ds} = \frac{E(x_j) \cdot \Delta x_n}{2} + \frac{E(x_j) \cdot \Delta x_p}{2} \quad (7)$$

Doping values and dimensions, presented in Fig 6. are chosen according to the literature [7]. It results that $\Delta x_n = 7.6\mu\text{m}$ and $\Delta x_p = 8\text{nm}$ at $V_{DS}=600\text{V}$. The 1D approximation of the heat flux profile in the volume $Q(x, t)$ [W/m^3] is depending on the electric field [V/m] function of the variable "x" and the drain- saturation current function of the variable "t" with the following formulation based on the scalar product between the electrical field profile and the density current :

$$Q(x, t) = \frac{E(x, t) \cdot I_D(t)}{S_{\text{chip}}} \quad (8)$$

Where $I_D(t)$ is the experimental short-circuit current and S_{chip} (10.4mm^2) the active area of the die.

Fig.6 depicts the boundary conditions. The top surface of the chip is assumed adiabatic due to the thick plastic coating around the die and the bottom is considered at a constant temperature (ambient temperature) due to the fact that the heat diffusion depth is much lower than the thickness of the die at the end of the short-circuit stress. This hypothesis has been confirmed by changing the boundary conditions (not presented here).

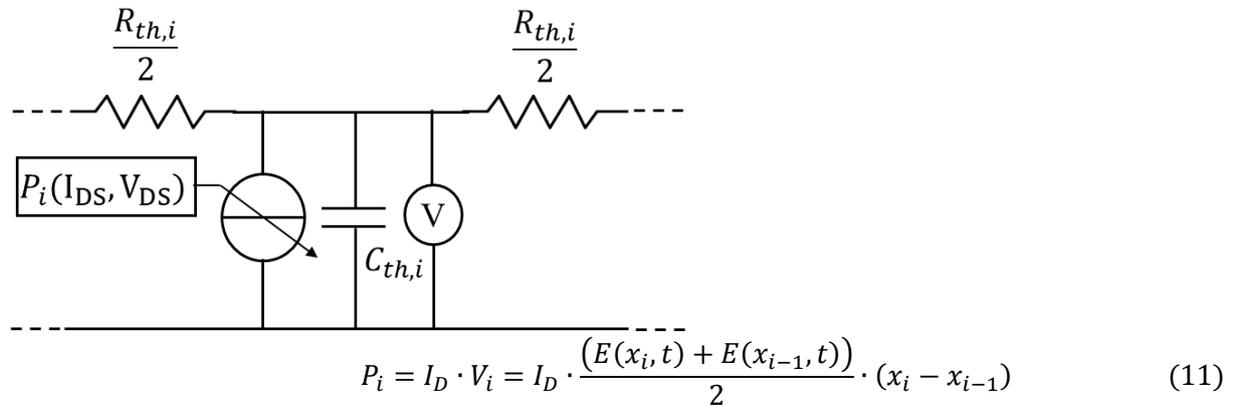
3.1.2 Model 1 distinctive characteristics

In the model 1, the thermal properties of the SiC: thermal conductivity (λ_{SiC}) and specific heat (C_{SiC}) have been chosen as constant values. Moreover, the aluminium top layer is not simulated, to overcome this, a thicker P-well have been chosen. Finally, this model has been implemented on two software:

- with COMSOL™ software by solving the heat equation in 1D.
- with PLECS™ by the mean of a Cauer network of RC-elements with a distributed power source. The Cauer model have been constructed by using a vectorised model [8] of 180 RC cells. The thermal resistors (R_{th}) and capacitances (C_{th}) are calculated as presented in (9). With n , the number of RC cells, λ the thermal conductivity of the material, C_p the specific heat capacity, ρ the material density, the active area of the die and d_{chip} the chip depth. .

$$R_{th,i} = \frac{1}{\lambda} \cdot \frac{d_{chip}}{S_{chip} \cdot n} \quad \& \quad C_{th,i} = C_p \cdot \rho \cdot \frac{d_{chip}}{n} \cdot S_{chip} \quad (9)$$

The power source is sampled in the depletion layer, following the trapezoidal rule:



However, this power source represent the mean value of the power between 2 sampled points, as a consequence the Cauer network has been built as presented Fig.7.

3.1.3 Model 2 distinctive characteristics

In the model 2, the aluminium top layer has been taken into account and included in the model. Moreover, the dependences of the thermal properties of SiC and aluminum with the temperature have been added into the model. The evolution of thermal conductivity and specific heat with the temperature can be found, respectively, in [9] and [10], as well as the melting latent heat of aluminium (933K). The model has been implemented in COMSOL™ software.

Fig. 7 : presented Cauer RC network

3.2. RESULTS

In Fig. 8, the junction temperature $T_j(x_j, t)$ is presented function of the short circuit duration for different drain biases. The presented results have been estimated from the two proposed models with two different solving process. In fig. 8a, the model 1 is solved with the two methods presented previously and the difference between the results is lower than 1%. The estimated temperature increases up to 1300K for 12 μ s of SC duration, these temperature values are close to results already observed in the literature[2], [11] but obtained with other estimation methods. As the temperature is not measurable, the results between models can only be compared.

In the other hand, the model 2, presented Fig. 7b, is giving very different results: the temperature can be 500K higher from results obtained from the model 1, although model 2 is more realistic. This difference can be explained by the SiC thermal conductivity which tends to decrease with the temperature increase while the heat capacitor tends to increase. This behavior induces a great decrease of the thermal diffusivity of the heat and then a significant increase of the local temperature around the maximum power density region. Therefore, the more the temperature is high, the less the component can dissipate the heat flux. Moreover, this model hasn't been implemented in PLECS software with a vectorized RC network due to convergence issues and long computation time.

Finally, the Model 1 implemented in PLECS has been chosen as temperature reference for the saturation current fitting as well as for the electrothermal circuit-type model.

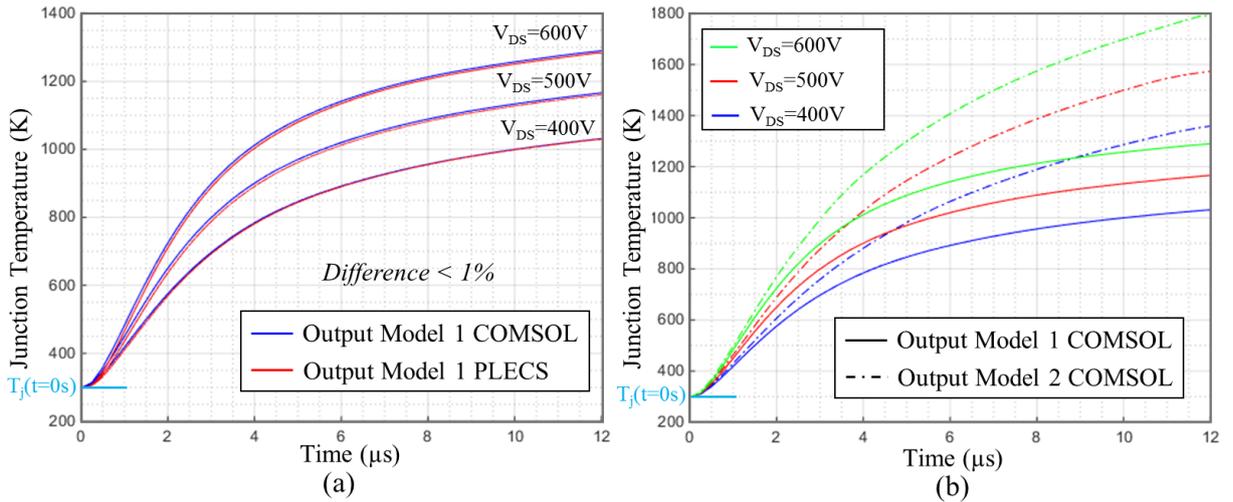


Fig. 8. Estimated junction temperature $T_j(x_j, t)$ in a short-circuit operation at $V_{buffer}=21V$, $T_{init}(t=0)=298,15K$.
(a) Estimated temperature between Model 1 solved but COMSOL and solved by a Cauer network with PLECS.
(b) Estimated temperature with model 1 and model 2 solved by COMSOL.

4. DRAIN SATURATION CURRENT MODEL

To accurately model the drain saturation current, as shown in Fig. 3, a representative physical model is needed. Available models depend of a lot of physical parameters that are not known over a wide temperature range. In order to estimate them, data from experiment are needed. Methodology is summarized in Fig. 9. Different models have been tested but finally, the following MOSFET model has been chosen due to its classical form [12]:

$$I_{Dsat}(T_j) = \frac{K_{gm}(T_j)}{2} \cdot (V_{gs} - V_{gs(th)}(T_j))^2 \quad (9)$$

With

$$K_{gm}(T_j) = \frac{\mu_n(T_j) \cdot C_{ox} \cdot Z}{L} \quad (10)$$

Where, C_{ox} is the oxide capacitance per square area, Z and L are the width and length of the channel respectively. The carrier mobility in the channel, μ_n , is at least the parallel combinations of three different mobility functions with different sensitivity toward temperature [5]. The Matheissen's rule gives:

$$\mu_n(T_j) = \frac{\mu_{a0} \left(\frac{T_j}{T_0}\right)^a}{1 + \frac{\mu_{a0}}{\mu_{b0}} \left(\frac{T_j}{T_0}\right)^{b-a} + \frac{\mu_{a0}}{\mu_{c0}} \left(\frac{T_j}{T_0}\right)^{c-a}} \quad (11)$$

Where μ_{a0} , μ_{b0} , μ_{c0} are mobility parameters at ambient temperature and a, b, c are sensitive thermal coefficients that have to be estimated in order to obtain a wide range temperature model. Otherwise, literature [12], gives a linear threshold voltage dependence with temperature:

$$V_{gs(th)}(T_j) = x_1 \cdot T_j + x_2 \quad (12)$$

Where x_1 and x_2 are unknown parameters.

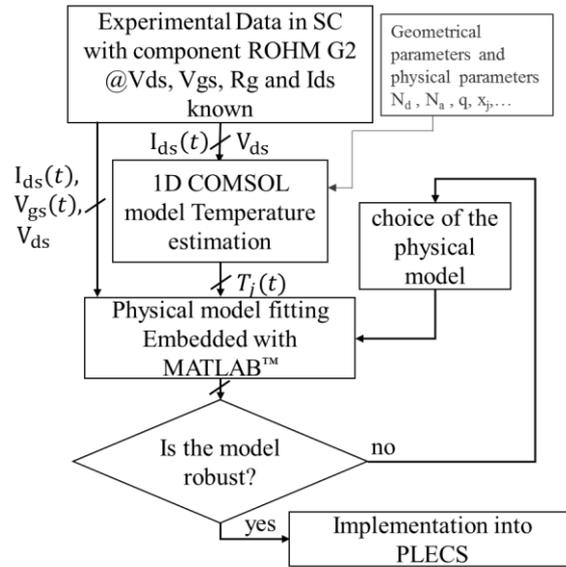


Fig. 9. Saturation current determination methodology

All the previous parameters are determined in two steps. At first, K_{gm} and $V_{gs(th)}$ are determined function of the temperature. To do that, an algorithm has been developed to find the best pair of parameters (x_1, x_2) which minimize the difference between calculated K_{gm} with the equation (9) for different experimental data. Results are displayed in Fig. 10 (b), with the couple $(x_1=-0.025, x_2=15.4)$ and K_{gm} remain the same for different buffer bias (19V, 20V, 21V). In a second time, the mobility model (11) is fitted on K_{gm} profile previously determined using MATLAB's function *fit*. Results are evaluated in Fig.10 (a).

Unfortunately at the current state, the model is not robust to V_{ds} variation. Other models have been tested to take this parameter into account but without success. In these conditions, the proposed model will be used for a fixed voltage. The work will have to be continued in order to develop a model taking into account the voltage applied on the drain

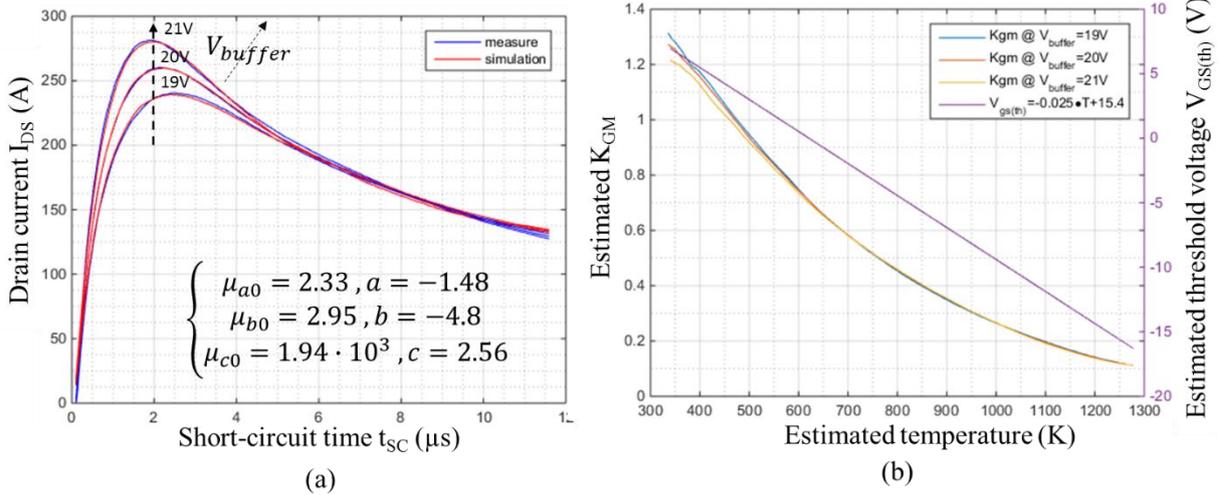


Fig. 10. (a) Model results of the saturation current obtained after fitting for different gate bias (experimental results in blue lines and simulation results in red lines). (b) K_{gm} and $V_{GS(th)}$ fitting based on the 1D thermal model and experimental data acquired with different gate bias and $V_{DS} = 600V$.

5. IMPLEMENTATION IN PLECS

The models have been implemented in PLECS™, a software for simulations of electrical circuits. PLECS™ presents the advantages of being embedded in MATLAB and of being able to quickly simulate complex electric topologies. The aim of this section is to present all the previous results implemented into a single circuit-type model as summarized in Fig. 2. The classical MOSFET model (in Fig.2 black line) is completed (in red line) adding the previously presented gate leakage current model " F_{IGleak} ", the drain saturation current model " F_{Idsat} " and finally the gate threshold voltage model by " $F_{V_{GS(th)}}$ ". The different models are performed by PLECS function block or by code-C script. Moreover, the thermal model is constructed with a vectorized Cauer RC network as presented in the previous section. The PLECS schematic is displayed in Fig.11a. This MOSFET model is itself connected to a voltage source between drain and source and connected to a MOSFET driver to turn it on/off (not displayed).

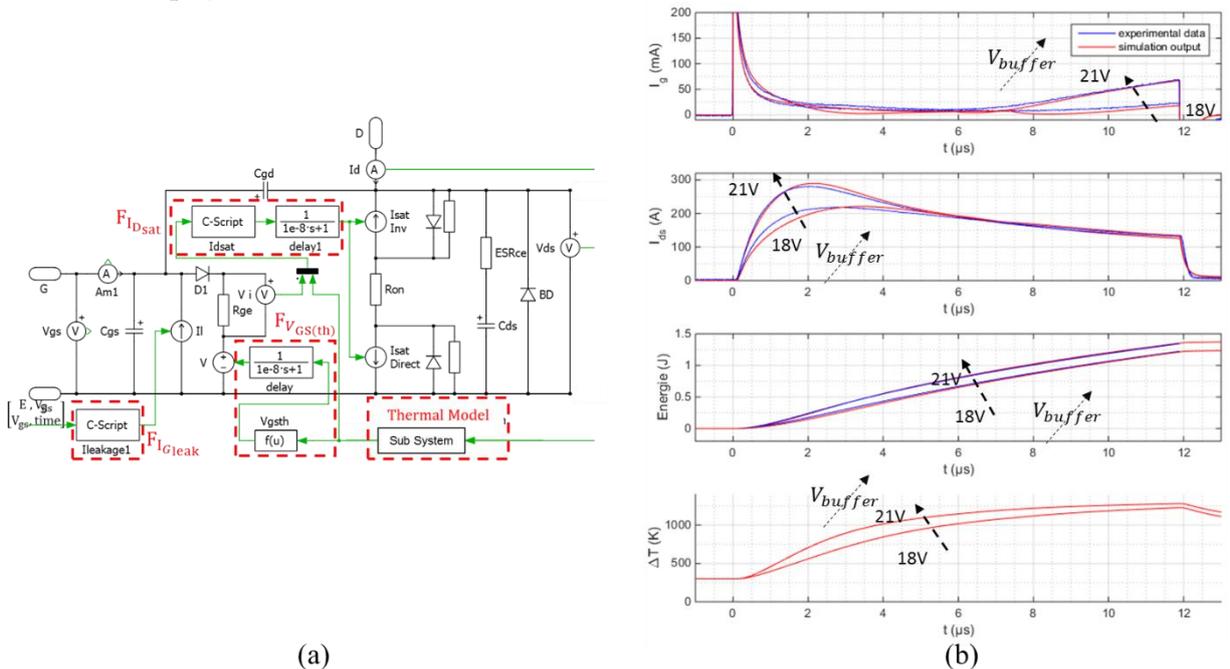


Fig. 11. (a) Proposed SiC MOSFET model in PLECS software. (b) Simulated waveforms from the proposed PLECS circuit-type model compared with measures for different buffer voltages bias (@V_{ds}=600V, T_{jinit}=298,15K (25°C) and R_g = 47Ω), temperature estimation at x=x_j with constant physical parameters

The results of the whole simulation are shown in Fig.11b. Clearly, the simulation results are much closed to the experimental waveforms during SC and the estimation error on the gate current surge is less than 1%. Our objective is fulfilled: the simulation is well working and will be able to be used in more complex circuit, for example, short-circuit detection and more generally concerning the safety analysis of critical system. Moreover, the model clearly represents the effect of the buffer voltage bias variation. All the modelling procedure is automatized in MATLAB and this model could be easily obtained for other SiC MOSFET devices. However, strong coupling with PLECS circuit and COMSOL 1D model should be implemented and drain saturation current robustness to V_{DS} voltage variation has to be also investigated in future works.

6. CONCLUSION

The aim of this paper was presenting a complete and new modelling methodology for SiC power MOSFET devices in high-current and high-temperature conditions. Firstly, the gate transient leakage current is modelled. In a second step the temperature is estimated inside the chip through two models and finally a physical model of the drain saturation current is given. After validating these different elementary models all the previous models are embedded into a circuit-type MOSFET model. This “block” could be used, as it is, to simulate fault operation into applications using SiC MOSFET components like a motor drive, for example. Moreover, the proposed model enhancement does not add a lot of calculation time and is fully compatible with classical numerical or circuit-type MOSFET models. The whole modelling has been performed on the ROHM component SCT2080KE but the method is clearly practical for other SiC MOSFET such as Wolfspeed or STMicroelectronics as demonstrated for the gate current modelling.

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