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Analog and Mixed-Signal Test

Haralampos-G. Stratigopoulos, Bozena Kaminska

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Haralampos-G. Stratigopoulos

Université Grenoble Alpes, CNRS, TIMA, France

Bozena Kaminska

Simon Fraser University, Canada

Analog and Mixed-Signal Test

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1 Introduction

Integrated circuits (ICs) are fabricated using a series of photolithographic, printing, etching, implanting, and chemical vapor deposition steps. This process is subject to imperfections that may cause complete failure in the operation of individual ICs, or variations in performance amongst ICs on the same wafer or across different lots. The performance of an IC could also shift in the post-silicon production flow during the packaging process. For all the above reasons, each fabricated IC must be tested, in order to ensure that it meets its design specifications.

The current practice for testing the analog and mixed-signal (AMS) functions of ICs is specification-based testing [1, 2, 3, 4]. Specification-based testing involves direct measurement of the performances that are promised in the specification data sheet one by one. However, despite the ease of interpreting the test result, specification-based testing incurs a very high cost since it relies on specialized Automatic Test Equipment (ATE) with advanced capabilities and running the tests takes a long time. In fact, testing the AMS functions of modern Systems-on-Chip (SoC) is responsible for the largest fraction of the test cost despite the fact that AMS circuits occupy a much smaller area on the die compared to their digital counterparts [5]. With the ever-increasing levels of integration of SoC designs, more and more of which include AMS circuits, ATE cost, test development and test execution times are being increasingly impacted and will keep increasing as we move towards more advanced technology nodes. AMS testing is nowadays an area of focus and innovation for the microelectronics industry.

It is thus necessary for design and test engineers to work together, early in the SoC architecture design phase, in order to keep the testing costs under control. Alternative low-cost test techniques need to be developed that can effectively replace standard specification-based tests. These techniques should target reducing test times and/or alleviating the need to rely on specialized ATE. Introducing alternative test techniques, however, should not sacrifice the high accuracy of specification-based testing, which is measured by test metrics such as test escape (e.g. faulty circuits passing the test) and yield loss (e.g. functional circuits failing the test). Therefore, any alternative test technique should be assessed by estimating the resultant test metrics that will be met in production.

This chapter will focus on generic alternative test techniques, such as inferring the outcome of specification-based testing from low-cost measurements (broadly known as “alternate test”), eliminating redundant specification-based tests and applying a reduced set, structural test techniques where the test problem reduces to checking for the presence of faults contained in a pre-defined list, as well as on practical integrated test techniques for different types of AMS circuits, such as analog-to-digital converters (ADC), digital-to-analog converters (DAC), phase locked loops (PLL), and radio-frequency (RF) circuits. This chapter will also review tools to assess the feasibility of alternative test techniques. All these techniques and tools are seen as an enabling technology to break the cost trend.

2 Integrated Test - An Overview

Integrated test techniques are grouped into Design-for-Test (DFT) and Built-In Self-Test (BIST) techniques.

DFT techniques can be broadly grouped into two approaches. The first DFT approach is to facilitate test access into the design by implementing test signal buses according to the IEEE Standards 1149.1 [6] and 1149.4 [7], as illustrated in Fig. 1. The IEEE 1149.4 architecture in Fig. 1 comprises a test bus interface circuit (TBIC) with analog test stimulus (AT1) and analog test output (AT2) pins, analog boundary modules (ABM) on each analog I/O, digital boundary modules (DBM) on each digital I/O, and a test access port (TAP) controller with test data in (TDI), test data out (TDO), test mode select (TMS), test clock (TCLK), and test reset (TRSTn) pins. This test bus architecture provides the means for bypassing functional blocks in the circuit under test (CUT), in order to apply test stimuli directly to internal blocks and reading out the test responses. Therefore, the test bus can be used to enhance the overall testability, as well as to enable system diagnostics and silicon debugging in post-manufacturing. In addition, the test bus can be used for testing for open- and short-circuits among the interconnections of circuits in a printed circuit assembly. The second DFT approach is based on reconfiguring the CUT to enhance its testability. A first well-known example is the generic oscillation test where the CUT is reconfigured to oscillate by connecting it into a positive feedback loop, as shown in Fig. 2. The oscillation frequency and magnitude are information-rich signatures that can be used to gain insight about the functionality of the CUT and to detect abnormal behavior [8, 9]. A second example is the loop-back test for RF transceivers where the test signals are generated in the baseband and the transmitter’s output is switched to the receiver’s input through an attenuator to analyze the test response also in the baseband [10, 11, 12, 13, 14, 15, 16], as shown in Fig. 3. We will revisit these two DFT techniques in more details in Sections 7 and 10.

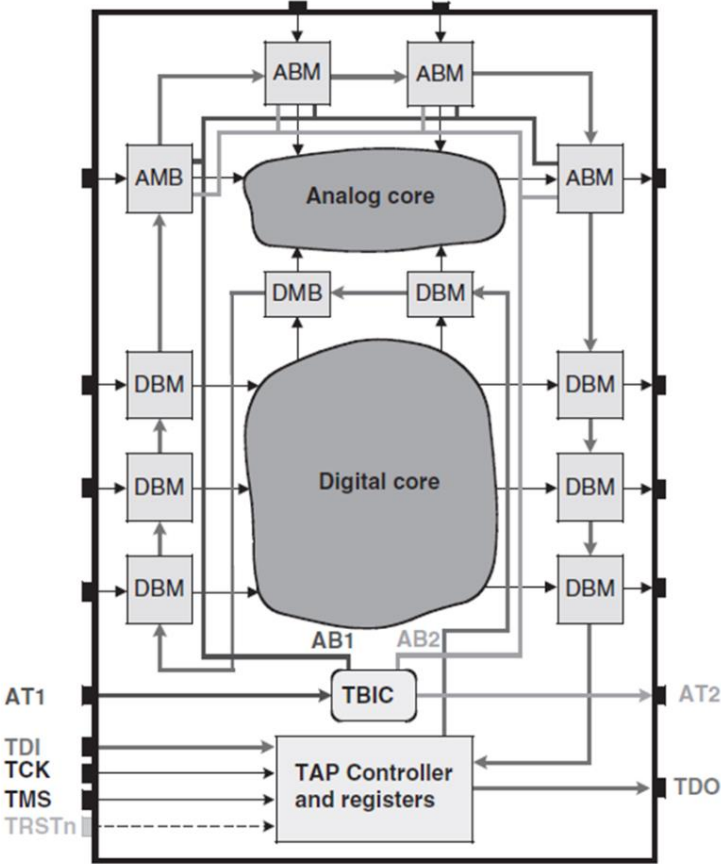


FIGURE 1 : IEEE 1149.4 architecture.

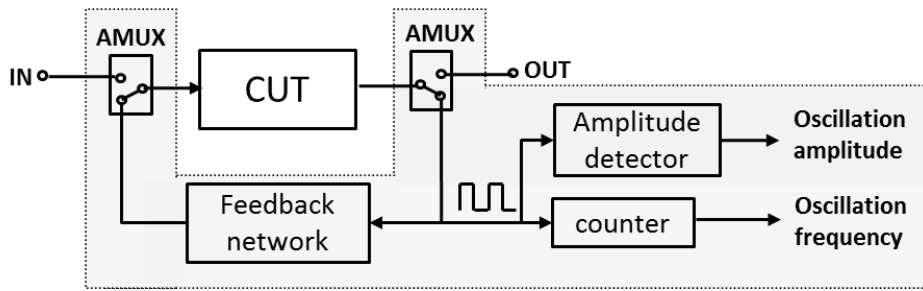


FIGURE 2 : Oscillation-based test architecture.

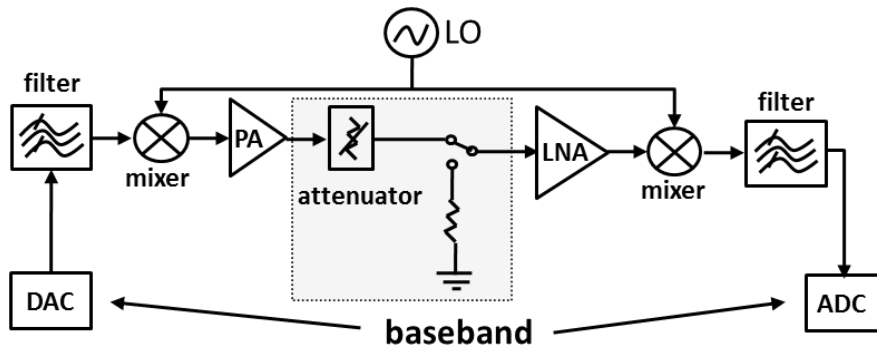


FIGURE 3 : Loop-back test for RF transceivers.

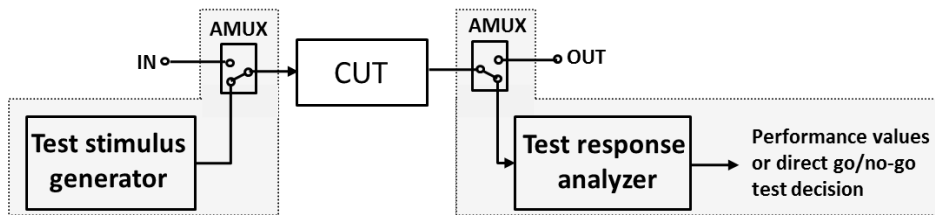


FIGURE 4 : BIST employing an on-chip test stimulus generator and an on-chip test response analyzer.

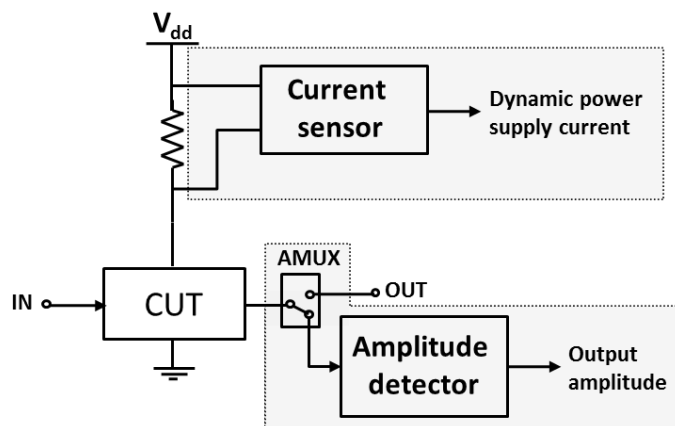


FIGURE 5 : BIST employing on-chip sensors.

BIST techniques can also be broadly grouped into two approaches. The first approach consists of embedding a signal generator and a test response analyzer into the chip [17, 18, 19, 20, 21, 22, 23],

as shown in Fig. 4, whereas the second approach consists of embedding sensors into the chip to extract off-chip information-rich, low-cost test signatures from which the status of the performances can be implicitly inferred [24, 25, 26, 27, 28], as shown in Fig. 5. The impetus for BIST techniques is to facilitate the use of low- performance ATE or perhaps to eliminate any need whatsoever by adding self-test capabilities, strategic control, and observation points within the IC.

DFT and BIST are very often ad hoc and largely a matter of early engagement with the design community to specify the test architecture. Great strides have been made to make DFT and BIST techniques successful for AMS ICs, but robust, production deployment of these techniques is not yet widespread. This is due in part to the challenge of evaluating their efficiency with respect to the standard specification-based test, which requires accurate simulation models and speeding up circuit simulation. In addition, DFT and BIST techniques should not consume a disproportionate amount of silicon die area and should neither be intrusive to sensitive circuits and design methodologies nor impede the post-silicon debugging process. Trade-offs between DFT and BIST techniques and traditional specification-based testing need to be considered and the test resources need to be intelligently partitioned between integrated and external test methods. Finally, given the rather high development time of DFT and BIST techniques, it is important to focus on their portability, such that they can be reused in different Intellectual Property (IP) blocks or cores.

Despite the above challenges, the pressing demand to reduce test cost has sparked an immense effort to materialize DFT and BIST techniques since they arguably constitute very attractive alternatives. This rationale stems from the fact that much of the ATE will be on-chip or in the form of partitioned test that can be executed much faster.

DFT and BIST techniques become of vital importance in the case of ICs that are part of a larger safety-critical, mission-critical, or remote-controlled system. During its lifetime, an IC may fail due to aging, wear-and-tear, harsh environments, overuse, or due to defects that are not detected by the production tests and manifest themselves later in the field of operation. In such cases, DFT and BIST can be used to support on-line test during normal operation by detecting early reliability hazards and gaining in- sight about environmental conditions that can jeopardize the system's health [29, 30, 31, 32, 33, 34, 35, 36, 37, 38, 39, 40, 41]. They can also provide valuable feedback for achieving fault-tolerance through calibration, tuning, or even reconfigurability [42, 43, 44, 45, 46].

Finally, DFT and BIST techniques can provide valuable feedback for diagnosis purposes [47, 48, 49, 50, 51, 52, 53, 54, 55, 56, 57, 58, 59]. Diagnosing the root-causes of failures in the first prototypes helps to reduce design iterations and to meet the time-to-market goal. In a high-volume production environment, diagnosing the root-causes of failures can assist the designers in gathering valuable information for enhancing yield in future IC generations. Diagnosis is also of vital importance in the case of failures in the field for safety-critical applications. Here, it is important to identify the root-causes of failures so as to repair the system if possible and apply corrective actions that will prevent failure re-occurrence and, thereby, will expand the safety features. DFT and BIST techniques vary depending the type of the AMS block and very often even for a particular design style or architecture. In Sections 8, 9, and 10, we will review popular DFT and BIST solutions for different AMS blocks in detail.

As mentioned in the introduction, the standard approach for testing AMS circuits is to measure directly the performances that are promised in the data sheet. The IC is declared faulty or functional by simply comparing the measured performance values to the design specifications. In this context, the necessary ATE resources are employed and overall the test approach is easy to interpret and implement since the same test benches are used as during the design and prototype characterization phases.

Alternate test aims to circumvent specialized ATE resources and speed up the test execution time by relying solely on measurements that can be rapidly extracted using a low-cost assortment of test equipment [60, 61, 62]. The grounds for achieving the objective of inferring the performances implicitly from low-cost alternate measurements is that both the performances and the alternate measurements are subject to the same process variations. Thus, in the presence of process variations, both performances and alternate measurements vary and the objective boils down to identifying alternate measurements that correlate well with the performances, such that any performance shift can be predicted from the corresponding shift in the alternate measurement pattern, as illustrated in Fig. 6. For the method to succeed, it is needed first to (a) identify such information-rich alternate measurements and second to (b) build the mapping between alternate measurements and performances.

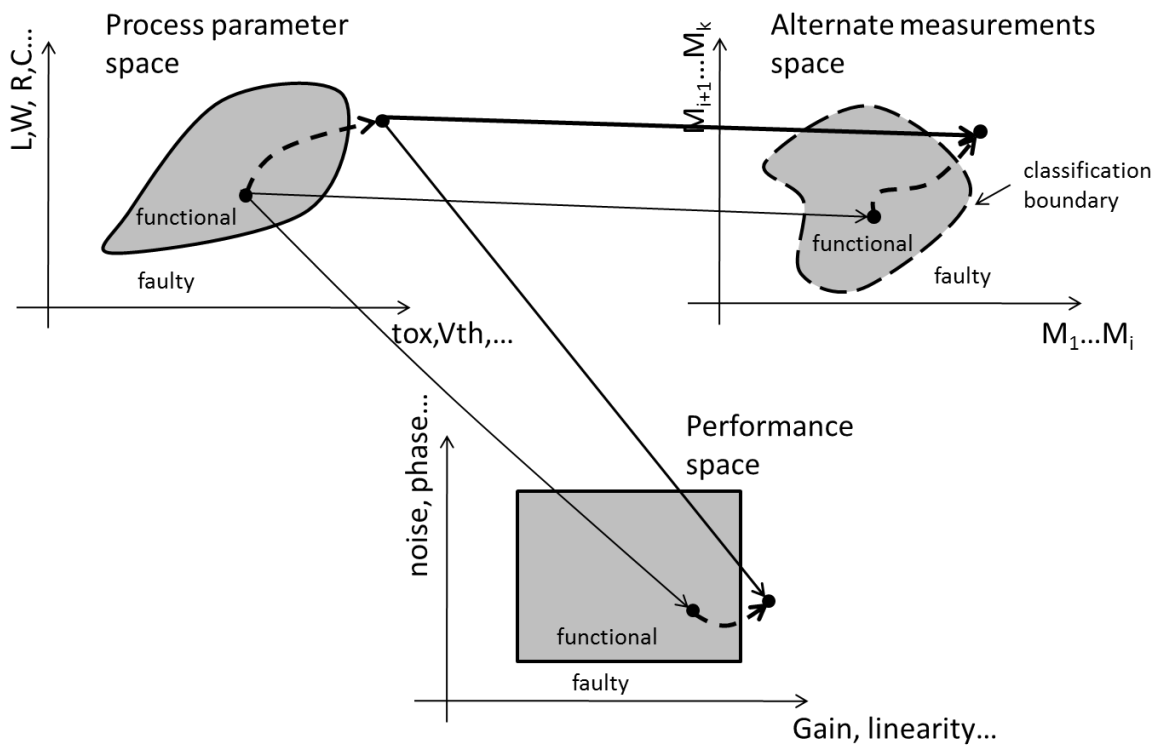


FIGURE 6 : Principle of alternate test.

The identification of appropriate alternate measurements is a circuit-specific problem since the input, output, frequency band, transfer function, etc., depend on the type of the IC, as well as its architecture. In the recent years, the alternate test paradigm has been proven for different types of ICs, including, baseband analog [60, 63], RF [64, 65, 66, 67], data converters [68, 69], PLLs [70], and

MicroElectroMechanical Systems (MEMS) [71]. Very often, the alternate measurements are extracted ad hoc without a clear rationale. Through simulations it is demonstrated that they can be used in- deed to predict the performance values and in the next step the concept is demonstrated experimentally in silicon. The reason is the large number of process parameters and their intricate interactions which makes impossible to justify that an alternate measurement captures all variation scenarios that can occur in practice. A typical approach is to identify as many alternate measurements as possible and then compact this set using feature selection algorithms [60, 72, 73, 74, 75], such as genetic algorithms [76], floating search algorithms [77], etc. Another approach is to craft the test stimulus such that the output response becomes appropriate for alternate test [60, 78].

Examples of alternate measurements for baseband analog circuits include sampling the output response when applying at the input a piecewise linear test stimulus [60, 63], a multi-tone sinusoidal [72], or a pseudo-random bit sequence [73]. Popular approaches to extract alternate measurements from RF circuits include (a) applying a baseband multi-tone sinusoidal, up-converting it using a mixer that exists on the test load board or on-chip, down-converting the RF output using again a mixer, and sampling the demodulated baseband test response [64, 65, 73]; (b) sensors that tap into the RF signal path, for example, amplitude detectors [79, 80, 25, 24, 81, 82, 83] and current sensors [84, 26, 82].

The intricate relationship among performances and alternate measurements makes impossible to build a mapping in the form of a closed-form mathematical equation. For this reason, the mapping is built through statistical learning. In particular, a set of N circuit instances that is representative of the fabrication process is collected. The d performances $P = [P_1, \dots, P_d]$ and alternate measurements M are obtained on each circuit instance. Part of the circuit instances are used to train a regression function $f_i: M \rightarrow P_i$ for each performance P_i . The circuit instances that are left out are used as an independent validation set. Target performances for the circuit instances in the validation set are assumed to be unknown and they are only used to estimate the test error. In particular, the alternate measurements are given as arguments to the regression functions to obtain performance predictions \hat{P} . If the test error $P - \hat{P}$, averaged over all circuit instances in the validation set, is deemed to be small, then the alternate measurements are satisfactory.

It should be noticed that outliers should be excluded from the training phase since they are inconsistent with the statistical nature of the bulk of the training data stemming from circuits with process variations and will adversely affect the regression fit results. In fact, outliers are non-statistical in nature since their real cause is physical defects that are induced or enhanced during the IC manufacturing in a random fashion. Likewise, the learned regression functions are not designed to predict the performances of outliers as the test outcome will be somewhat random. Thus, in the testing phase, all ICs should be checked to verify that they are not outliers before the learned regression functions are applied to reach a test decision. This indispensable step in the flow of alternate test makes use of a defect filter [85].

Instead of predicting the actual values of the performances, it is also possible to predict directly whether the performances satisfy their specifications, that is, a form of go/no-go test. In this case, a classifier is used that implements a function $g: M \rightarrow [\text{pass}, \text{fail}]$ [86, 87, 88, 89, 72, 73]. The classifier should be able to allocate a non-linear decision boundary in the space of alternate measurements such that the population of functional circuits is separated from the population of circuits that violate

at least one specification, as illustrated in Fig. 6. Various classifiers can be used in this context, including Support Vector Machines (SVM) [90], decision trees [91], ontogenic neural networks [92], feed-forward neural networks [93], etc. Similarly to the regression functions, the better the correlation among performances and alternate measurements is, the smaller will be the overlap between the two populations and the better the classification rate will be. Furthermore, the classifier can be implemented on-chip towards a stand-alone BIST [94].

The advantage of using regression functions is that it offers the possibility of predicting the performance values, which allows binning of functional circuits and a better insight into the performance distributions. The classifier has the advantage that it can screen out circuits with defects on top of circuits with excessive process variations. However, this is at the expense of requiring to include circuits with defects in the training set which may be difficult to collect in the production environment in a short period of time. To this end, an one-class classifier can be used that avoids this requirement [95].

Finally, as any other indirect test method, alternate test is prone to error. To improve confidence in the test decision, it is possible to identify the small fraction of circuits that will be likely erroneously predicted and forward them to a second test tier where more thorough testing is performed. Several techniques exist for this purpose, including the use of guard-bands in the case of classifiers [73], using multiple regression functions [96], and a pair of defect filters [95].

4 Specification-Based Test Compaction

A plausible direction towards decreasing test cost is to identify and eliminate information redundancy in the set of specification-based tests, thereby relying only on a subset of them in order to reach a pass/fail decision. Such redundancy is likely to exist since groups of performances refer to the same portion of the IC and are subject to similar process imperfections. However, it is highly unlikely that it will manifest itself in a coarse and easily observable form of superfluous tests that can be summarily discarded. Hence, more advanced statistical analysis methods are likely to be required.

In the linear error-mechanism model algorithm (LEMMA) [97], availability of a linear model $y = Ax$ is assumed [98], where y is the $m \times 1$ measurement error vector, x is a $n \times 1$ process parameter error vector, A is a $m \times n$ sensitivity matrix, and m corresponds to the number of measurements required for complete specification testing. The method aims to predict the complete vector y by carrying out only a subset \tilde{y} of y . The cardinality p of \tilde{y} ($p \geq n$) is a compromise between the permitted measurement cost and the maximum tolerable prediction error. The selection process is performed through QR factorization [99] and minimizes the normalized prediction variance. This is equivalent to maximizing the determinant $\tilde{A}^T \tilde{A}$, where \tilde{A} designates the $p \times n$ row-reduced matrix A . In [100], an iterative selection approach is followed, which considers subsets rather than individual measurements. Next, the complete measurement vector is predicted by $y = A(\tilde{A}^T \tilde{A})^{-1} \tilde{A}^T \tilde{y}$. A leisurely look at this approach and some refinements are provided in [101].

In [102], a fault-driven test selection approach is proposed. The set of needed tests is cumulatively built by adding to the current set the test for which the yield, as computed by considering only the specifications of the remaining tests, is maximized. The algorithm terminates when the desired fault coverage is reached. In [103], in addition to fault coverage, the test selection is driven by the degree to which faults are exposed. After the redundant tests have been eliminated, a test ordering

algorithm can be run, aiming to reduce the average test time. The tests that have higher priority of being placed at the beginning of the sequence are those that have a high probability of detecting failures, are low-cost, and are independent of the previous tests in the sequence. Test ordering algorithms that appear in the literature include trial of various test permutations based on a heuristic approach to estimate whether a permutation is likely to improve average test time [102], dynamic programming of a directed flow graph [104], which results in the optimal order, and a variation of the latter, called A* algorithm [102], which, in the worst case, requires the same computational cost while maintaining optimality.

In [105], specification testing is simplified using a technique called predictive subset testing. It requires measurement of all performances for a set of circuit instances, which is assumed to be representative, reflecting accurately the statistical mechanisms of the manufacturing process. The technique is based upon establishing regression mappings between correlated pairs of performances. In this situation, we seek to predict one (untested) performance using another performance that is explicitly tested. Then, new test limits are assigned to the tested performance, such that they guarantee the compliance of the untested performance to its specifications with the desired confidence levels.

The problem of specification-based test compaction can also be viewed as a binary pass/fail classification problem [106, 107, 108]. This approach entails two components, namely a feature selection algorithm for searching in the power-set of specification-based tests and a prediction model for predicting based solely on a select subset the outcome of the remaining specification-tests that are excluded from this subset, as shown in Fig. 7. Different feature selection algorithms can be employed, for example, genetic algorithms [76], floating search algorithms [77], etc., and the prediction model can be built using binary classifiers, such as Support Vector Machines (SVM) [90], decision trees [91], ontogenic neural networks [92], feed-forward neural networks [93], etc. The search progresses towards a low-cost, low-dimensional specification-based test subset based on which the classifier predicts correctly the pass/fail outcome of the complete specification-based test suite.

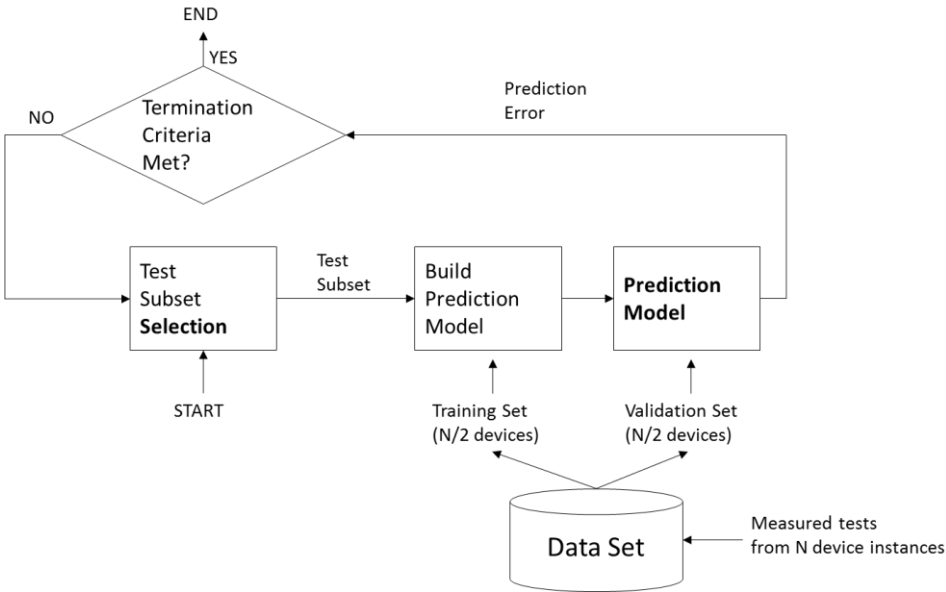


FIGURE 7 : Feature selection algorithm for specification-based test compaction.

5 Probabilistic Test Metrics Estimation

As it has been made clear so far, the general objective of the research conducted in the AMS test domain is to develop alternative tests that can replace effectively the costly specification-based tests. Despite the high number of proposals, few have materialized to date. One of the primary reasons is the lack of automated tools to evaluate alternative tests in terms of the resultant test error. Indeed, although it is straightforward to provide claims about the test cost reduction and overhead in the case of DFT and BIST techniques, it is not as straightforward to provide estimates of test escape and yield loss and project such test metrics in Parts Per Million (PPM) values, as shown in Fig. 8. Test metrics estimation has to take place during the test development phase through simulation before moving to production test. Otherwise, significant test resources and time must be dedicated without any guarantee that the alternative test will be proven indeed effective. Preferably, we would like to estimate test metrics early in the process so as to refine alternative tests or even abandon them indefinitely in time.

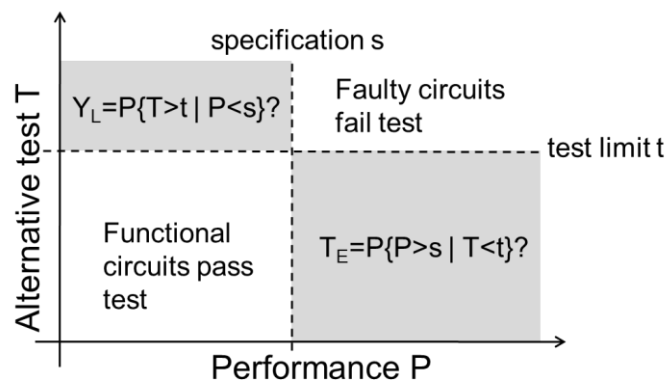


FIGURE 8 : Areas of test escape TE and yield loss YL assuming that the specification-based test targeting performance P has been replaced by an alternative test T .

Broadly speaking, the faulty behavior of a circuit can be due to two reasons: (a) defects in manufacturing that translate into topological changes in the form of short- and open-circuits, in which case we refer to catastrophic faults, and (b) variations in the process parameters, in which case we refer to parametric faults. While catastrophic fault coverage can be evaluated given a list of probable catastrophic faults, evaluating parametric fault coverage (or, equivalently, parametric test escape) and yield loss is a far more complex problem. The reason is two-fold. First, the set of circuits that give rise to yield loss and the set of parametric faults are infinite. Second, we would like to be estimate parametric test escape and yield loss metrics as low as a few tens of hundreds of PPM, whereas a standard Monte Carlo approach by default samples the most likely statistical events and, thereby, we would require an intractable number of runs that we cannot afford. The problem essentially boils down to speeding up Monte Carlo simulation.

The general idea is to substitute the circuit with an equivalent model that can be simulated much faster, as shown in Fig. 9. Using N initial simulations that we can afford to run, we build a model of the circuit and thereafter we simulate it to generate $N' \gg N$ circuit instances. Thereafter, we can approximate test metrics using relative frequencies.

For example, the model could consist of a set of regression functions that map any point in the design space (e.g. process and design parameters) to the output parameters of the circuit (e.g. performances and test measurements) [102, 109]. As an alternative for the regression functions, one can use symbolic models that are fitted using genetic programming [110]. If the accuracy of these models is deemed to be insufficient at the tails of the design space, then we can choose to perform circuit-level simulations for the points that are identified to lie at the tails of the design space [111].

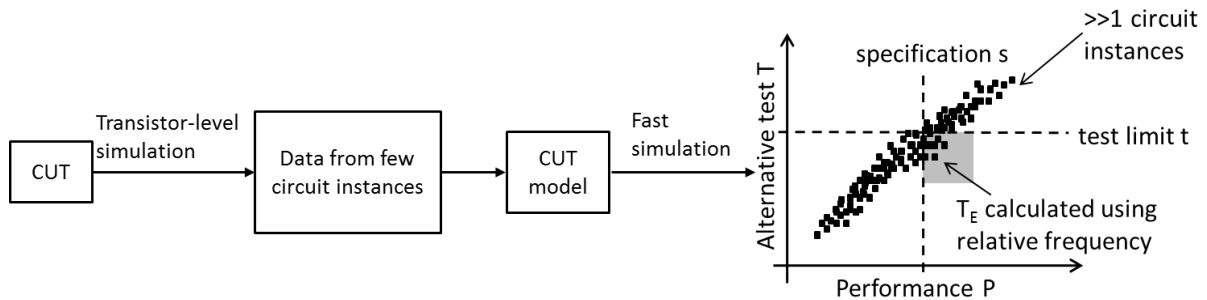


FIGURE 9 : Principle of test metrics estimation using fast statistical simulation.

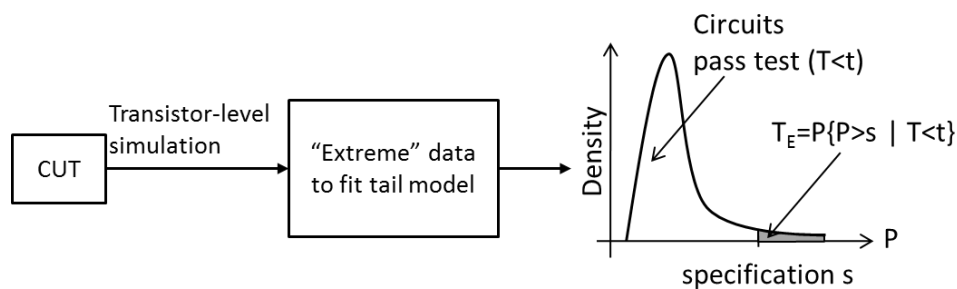


FIGURE 10 : Principle of test metrics estimation using statistical blockade and extreme value theory.

An alternative approach is to use the initial N simulations to estimate the joint probability density function (PDF) of output parameters [112, 113, 114]. The joint PDF can be sampled very fast to generate the N' new circuit instances. Other solutions related to PDF estimation are based on the theory of Copulas [115] or on linear error-mechanism models [116].

The most recent approach to test metrics estimation is based on the statistical blockade technique and extreme value theory [117, 118]. The statistical blockade technique [119] is used to bias the Monte Carlo simulation so as to quickly simulate a set of most probable "extreme" circuits that lie close to the tails of the distribution of performances and alternative tests and give rise to test escape and yield loss. Thereafter, this set of "extreme" circuits is used to fit a probability model for the parametric test escape and yield loss using the extreme value theory [120], as shown in Fig. 10. This technique has the advantage that it focuses directly at the tails of the distributions where the test escape and yield loss events occur.

For circuits that are hard to simulate, such as data converters and PLLs, to estimate test metrics simulations are performed at the behavioral level [121, 122].

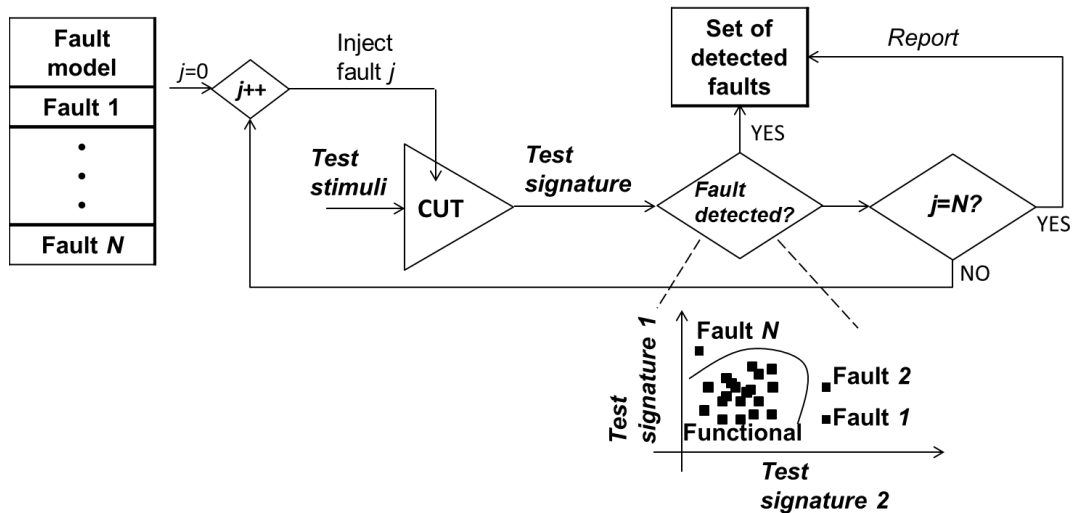


FIGURE 11 : Estimating test escape of an alternative test approach based on a fault model.

6 Fault Modeling and Structural Test

The introduction of the stuck-at fault model for digital circuits enabled digital testing to cope with the exponential growth in the digital circuit size and complexity. Indeed, the stuck-at fault model enabled functional testing to be replaced by structural testing, acted as a measure to quantify the quality of the test plan, and paved the way for the development of efficient DFT and BIST strategies.

Intense efforts have been made to borrow from the success of the stuck-at fault model and develop an appropriate and comprehensive fault model for AMS circuits that accounts for all fault mechanisms in the manufacturing process. In general, a fault model is defined as a set of circuit instances, each representing a scenario in the manufacturing process that results in faulty circuit behavior, such that all possible catastrophic and parametric fault scenarios are accounted for.

Fault models can be used to evaluate the test escape as a result of replacing specification-based tests with alternative tests. The approach consists of injecting one fault at a time into the netlist of the circuit and checking whether the alternative test is capable of detecting the fault, as shown in Fig. 11. Detection implies that the alternative test is capable of clearly distinguishing the response of the faulty circuits from the response of functional circuits. In addition, fault models can be used for structural test. For a given fault model, the structural test generation problem boils down to generating a set of tests that detect all faults in the model. To this end, many test generation algorithms have been written to craft a test stimulus and select the output test signature such that the distance between the functional circuits and the faulty circuits is maximized [123, 124, 125, 126, 127, 128, 129, 130, 131].

A fault model that accounts for catastrophic faults can be developed based on inductive fault analysis on physical layouts [132, 133, 134, 135, 136, 137]. This requires a description of defect statistics, which, when mapped onto the layout, provide a list of probable faults. At the circuit level, the fault list consists of short- and open-circuits. This approach has led to defect-oriented test techniques [58, 59, 138] which can be applied for wafer-level testing to detect dies with gross defects or for final testing of robust designs that are highly unlikely to fail due to process variations.

The definition of a parametric fault model poses a greater challenge [139]. The reason is that there is an infinite number of combinations of process parameters that result in specification violation, that is, the size of the parametric fault model is limitless. Thus, we need to consider parametric faults according to their probability of occurrence and define a parametric fault model that contains the most probable parametric faults. Previous proposals for parametric fault modeling made certain assumptions to be able to deal with this challenge [137, 140, 141, 142, 143, 144, 145]. The widespread approach has been to build a parametric fault model at a higher level of abstraction, for example, by modeling faults as variations in passive components and in transistor parameters, i.e. transconductance, geometry, oxide thickness, threshold voltage, etc., or by considering behavioral simulation instead of transistor-level simulation and modeling faults as variations in the parameters of the behavioral model. Furthermore, a common assumption is that parameters vary independently, which is known as single fault assumption, and that a circuit fails a specification when one parameter exceeds a specific tolerance. These simplified fault models make simulation more traceable, yet their ability to capture correctly faulty behavior due to process variations has never been proven.

A fault model that consists of the most probable parametric faults generated naturally by a Monte Carlo analysis that makes use of the actual Process Design Kit (PDK) remains an open challenge [146]. A technique was proposed recently in [147] that employs the statistical blockade algorithm to speed up Monte Carlo analysis. The underlying idea is to bias the Monte Carlo analysis such as to avoid simulating circuits that are functional and, thereby, are of no use for generating a fault model.

7 Oscillation-Based Test

Oscillation-based test is a generic DFT/BIST technique [8, 9]. It relies on converting the circuit to an oscillator and subsequently measuring the oscillation frequency and magnitude, as shown in Fig. 2. The reconfiguration of the circuit is accomplished by using digital circuits to control analog switches and multiplexers, which are designed to have a minimal impact on the measurement. The oscillation frequency and magnitude are information-rich alternate measurements that are a function of the process parameters and also the elements that are added in the feedback path to enable oscillation. As a result, by repeating these measurements under varying voltage conditions, for different frequency selection, and for different feedback topologies with different attenuation levels, it is possible to infer implicitly the status of the performances. In particular, test limits can be placed on the oscillation frequency and magnitude to guarantee with some level of certainty that the performance values lie within the specification range. The test limits can be found through simulation and can be selected such that a desired trade-off between test metrics is achieved [148].

Oscillation-based test has several advantages: (a) it is adaptable virtually to all AMS circuits including baseband analog [8, 149, 150, 151, 152, 153, 154, 9, 155, 156], data converters [157, 158, 159], RF [160], and MEMS [161]; (b) it is vector-less since the circuit is self-excited without requiring signal generators; (c) the oscillation frequency can be processed to obtain digital test signatures that can be easily extracted off-chip for analysis; (d) it is immune to noise since the frequency is averaged over many periods; (e) it delivers excellent fault coverage for catastrophic and parametric faults [162].

ADCs and DACs are characterized by dynamic specifications, such as total harmonic distortion (THD), signal-to-noise ratio (SNR), signal-to-noise-and- distortion ratio (SNDR), etc., and static specifications, such as differential non-linearity (DNL), integral non-linearity, offset, gain error, etc.

The standard approach to measure the dynamic specifications of an ADC is to apply a high-resolution sinusoidal at the input and compute the Fast Fourier Transform (FFT) at the output. The resolution of the sinusoidal typically needs to be at least two bits higher than the effective resolution of the ADC, which poses a great design challenge for BIST implementation. A classical approach for generating on-chip an analog sinusoidal is to employ a closed-loop oscillator that involves a highly selective bandpass filter and a comparator [163, 164], as shown in Fig. 12. To improve the resolution of the sinusoidal generators they can be combined with harmonic cancellation techniques [165, 166, 167, 168]. Another classical approach is to employ an open-loop oscillator, as shown in Fig. 13. The starting point is to use an ideal $\Sigma\Delta$ modulator in software that converts a high-resolution sinusoidal to a bit stream which, thereafter, is loaded and periodically reproduced in an on-chip circular shift register [19]. Bit streams can also be generated by on-chip digital oscillators [169, 170]. The bit stream can be converted on-chip to a high-resolution sinusoidal by passing it through an 1-bit DAC followed by a low-pass filter to remove the quantization noise [171, 172]. Digital techniques can be used to cancel harmonic components at the output of the DAC [173]. Interestingly, in the case of switched-capacitor (SC) $\Sigma\Delta$ ADCs, the bit stream can be fed directly into the modulator by adding simple circuitry at its input [174, 175, 176, 177]. Another possibility is to replace the conventional sinusoidal test stimulus with a step-wise exponential [178] or, in the case of $\Sigma\Delta$ ADCs, with a pseudo-random pattern sequence [179]. For analyzing the test response, performing a FFT on-chip incurs a high area overhead [180]. If the FFT cannot be performed in a DSP, then for a full BIST implementation, it is required to replace the FFT algorithm with an alternative less computationally-intensive algorithm. Well-known algorithms are the sine-wave fitting [181, 182, 183] and the Goertzel algorithm [184]. A variant of the sine-wave fitting algorithm with reduced complexity and, thereby, more efficient digital implementation, is proposed in [175] in the case of stereo SC $\Sigma\Delta$ DC. Another variant is proposed in [185] and makes use of the COordinate Rotation DIgital Computer (CORDIC) algorithm.

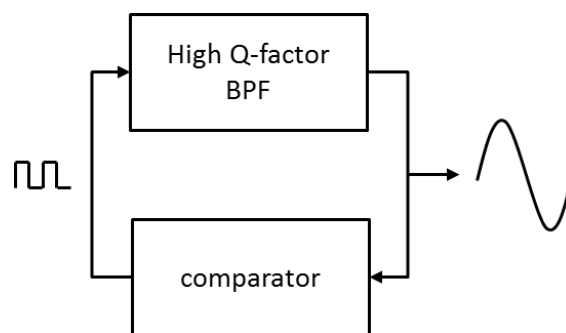


FIGURE 12 : Closed-loop sinusoidal signal generator.

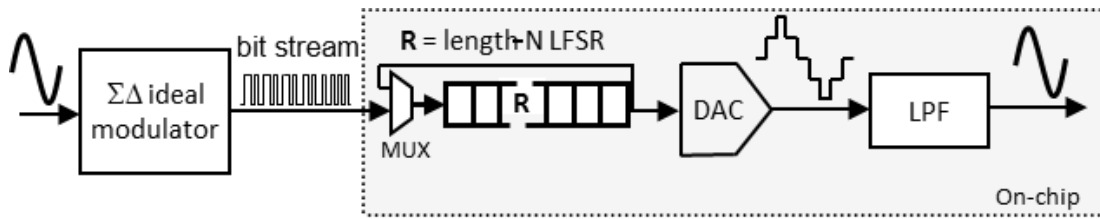


FIGURE 13 : Open-loop sinusoidal signal generator based on $\Sigma\Delta$ bit streams.

The standard approach to measure the static specifications of an ADC is to apply a ramp at the input and obtain the histogram of the number of occurrences of each code at the output. On-chip adaptive ramp generators are proposed in [186, 187]. A ramp generator that relies on the oscillation-based test principle is described in [158]. Alternatively, an exponential waveform can be employed in the analysis [188, 189]. Another interesting approach is based upon first identifying and computationally removing the source non-linearity and then accurately estimating the ADC static performances [190, 191, 166]. For analyzing the test response, it is required to store both the experimental and reference histograms and use the DSP to perform the comparison. Efficient BIST implementations of the histogram analysis are proposed in [192, 193]. For ADCs having a repetitive structure, such as pipeline, cyclic, and successive approximation ADCs, we can also apply what is broadly known as reduced code testing [194, 195, 196, 197]. Only a few codes need to be judiciously targeted and from this information we can extrapolate the complete histogram.

Instead of targeting a functional BIST approach aiming at measuring directly the dynamic and static specifications, it is also possible to consider a structural DFT approach where the aim is to obtain measurements that re-veal important design parameters, such as the poles and settling errors of the integrators in the case of $\Sigma\Delta$ ADCs [198]. A DFT approach proposed also specifically for pipeline ADCs is to reconfigure consecutive pipeline stages to form $\Sigma\Delta$ modulators and then test instead the $\Sigma\Delta$ modulators through digital means [199]. A generic approach virtually applicable to any ADC is to obtain information from process control monitors that are scattered across the die and use this information to make judgements about the performances of the ADC [200].

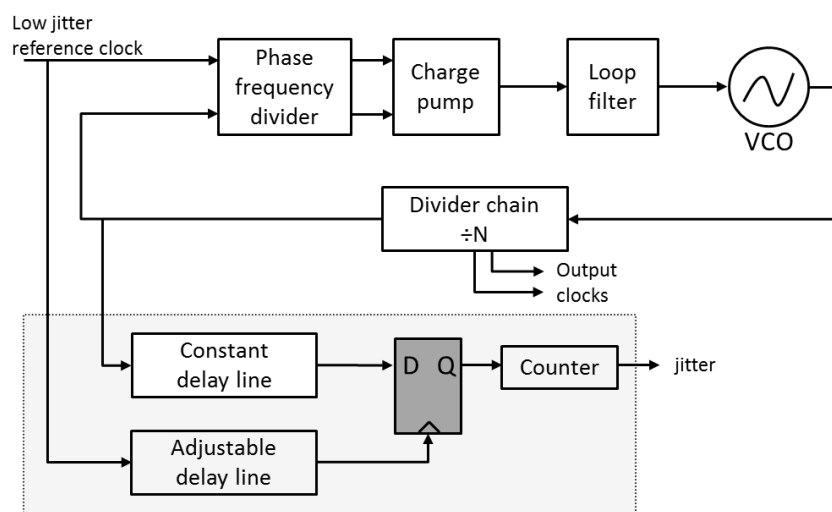


FIGURE 14 : On-chip jitter measurement circuit that uses an adjustable delay line.

Regarding a DAC, the standard approach to measure the dynamic specifications is to apply a digital signal at the input that encodes a high-resolution sinusoidal and compute the FFT at the output. For a BIST implementation the digital signal can be stored on-chip in a memory. However, for analyzing the test response, performing the FFT on-chip [22, 23, 201, 202, 203] seems to be unavoidable, unlike in the case of ADCs where there exist alternatives, as discussed above. The standard approach to measure the static specifications is to apply a digital ramp at the input that contains all possible digital codes and measure the output with a digital voltmeter. A BIST implementation is proposed in [204].

Finally, in the case of SoCs that comprise a set of ADCs and DACs, a technique to test them altogether in a fully digital set-up is proposed in [205].

9 PLL DFT and BIST

PLLs are fundamental building blocks for processors and communication systems since they are used to synthesize clocks for data synchronization and to provide the frequency sources for up-conversion and down-conversion in RF transceivers. The standard functional tests for PLLs include measuring the loop gain, the lock time, defined as the time it takes for a PLL to acquire phase lock after an abrupt change in the phase of its reference signal, and the lock range, defined by the minimum and maximum frequencies that a PLL can lock to within its lock time.

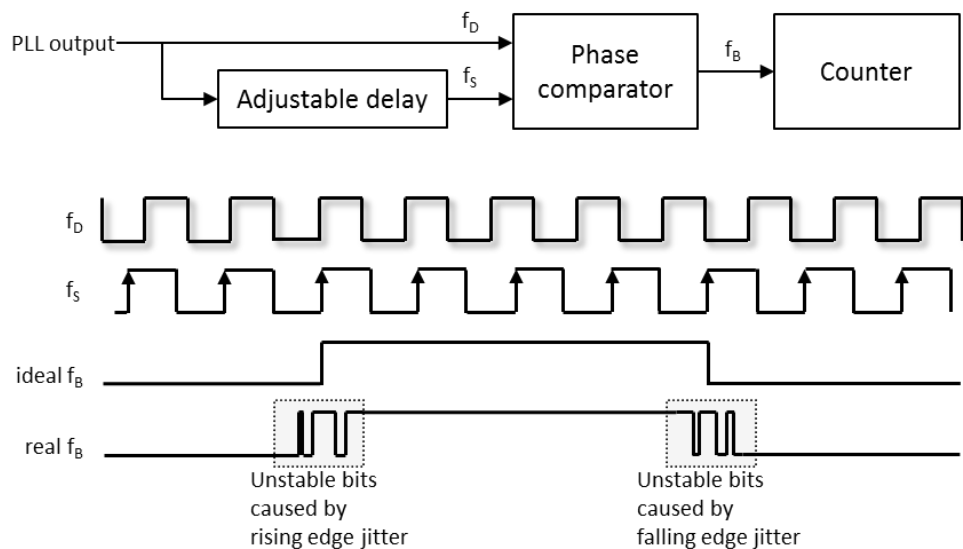


FIGURE 15 : On-chip jitter measurement circuit that uses a phase comparator.

However, perhaps the most important performance of a PLL is the jitter which defines, in turn, the Bit Error Rate (BER) in communication systems. The most common types of jitter are the timing jitter, defined as the edge timing variation relative to the ideal edge timing, the period jitter, defined as the variation of each period relative to the average period, and the cycle-to-cycle jitter, defined as the variation in each period with respect to the preceding period. Within these types, jitter can be random or deterministic. The jitter, despite being the most important performance of a PLL, happens to be the most challenging one to measure on an ATE. The reason is two-fold. First, the standard method that uses high-speed sampling oscilloscope requires tens of seconds which is

prohibitive for production testing. Second, as the PLL output is transferred off-chip, significant jitter is added due to capacitive coupling to other signals on-chip and transmission line effects off-chip. In addition, sampling the PLL output to extract the PLL jitter introduces even more jitter and, thus, the measurement ends up being imprecise. For these reasons, measuring jitter exactly at the PLL output using BIST is the recommended method, especially for multi-GHz PLLs that may have RMS jitter as low 0.1-5 ps.

An on-chip jitter measurement technique based on an adjustable delay line is shown in Fig. 14 [206]. The PLL output edge timing is compared to a delayed version of the input reference clock edge that has low jitter.

For digitally-controlled incrementing delays, we can deduce a cumulative histogram of the output jitter relative to the reference clock edges. However, the fact that the delay line adds jitter and the fact that the PLL and the BIST share the same power supply which increases the jitter in the PLL limit the resolution of the measurement to 10 ps. Similar resolution can be achieved by other on-chip jitter measurement techniques based on Vernier delay lines and Vernier oscillators that also incur similar area overhead [207, 208, 209]. Better resolution down to the resolution required by multi-GHz PLLs can be achieved with the scheme in Fig. 15 that employs a phase comparator [210, 211]. The idea is to under-sample the PLL output that has frequency f_D by a slightly lower clock frequency $f_S = f_D \times N / (N + 1)$, where N is a positive integer. The resulting low-frequency digital waveform has a beat frequency $f_B = f_D - f_S$. At the time where we sample the rising and fall edges of the PLL output the output of the phase comparator will be unstable due to the presence of jitter at the PLL output. The level of instability of the bits at times where the rising and falling edges occur is directly related to the PLL jitter and, thus, by using a counter we can extract a signature that can be mapped to the PLL jitter.

Finally, BIST techniques to measure the jitter transfer function of PLLs are described in [212, 213]. BIST techniques to measure various PLL parameters, including VCO gain, lock time, lock range, phase offset, etc., are described in [206, 214, 70, 215]. Structural test techniques targeting catastrophic faults that employ DFT are described in [216, 217].

10 RF DFT and BIST

Perhaps the earliest system-level DFT strategy for RF transceivers is the loopback architecture shown in Fig. 3 [10, 11, 12, 13, 14, 15, 16]. Digitally modulated baseband test signals are transmitted through the RF transceiver chain and the baseband response signals are sampled to evaluate the performance of the RF transceiver. In this case, the Digital Signal Processor (DSP) can serve as both a test stimulus generator and a test response analyzer. The transmitter is connected to the receiver through an attenuator such that the Power Amplifier's (PA) output is suitable for the dynamic range of the Low Noise Amplifier (LNA). This approach presents many challenges related to the signal-path mismatch, crosstalk, and signal-leakage, which can obscure the faulty behavior, and the area overhead of the loop-back connection. Analytical techniques to decouple the transmitter and the receiver in loopback mode and measure I/Q imbalances and non-linearity are presented in [218, 219, 220, 221]. Alternate test of RF transceivers in loopback mode is discussed in [222, 223].

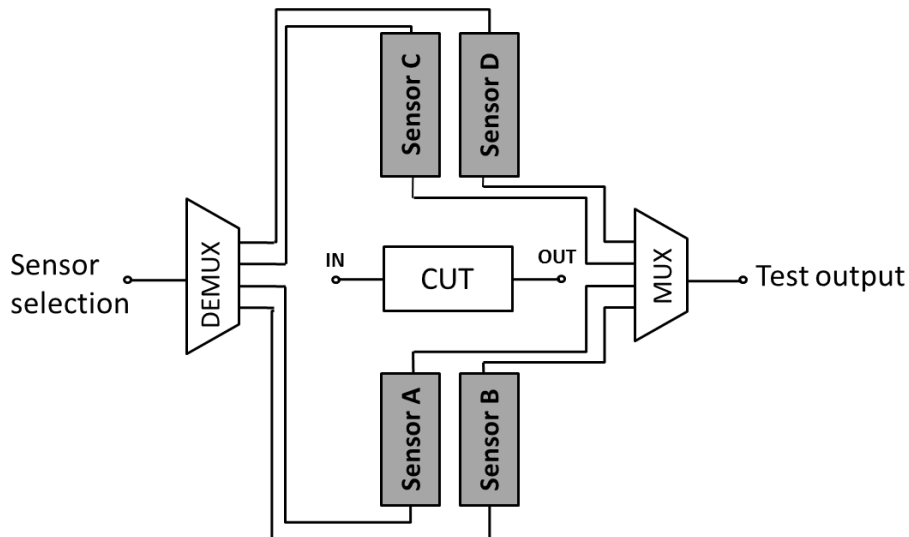


FIGURE 16 : BIST based on non-intrusive sensors.

Instead of performing a system-level test based on a loop-back connection, another possibility is to target BIST of the blocks inside the RF transceiver. A popular BIST strategy is to employ on-chip sensors, as shown in Fig. 5. Two types of sensors are most commonly used. The first type is an amplitude (or envelope) detector which provides a DC signature that carries information about the RF amplitude [79, 80, 25, 24, 81, 82, 83]. The second type is a current sensor which takes advantage of the small parasitic resistor (it can reach several ohms) of the line that connects the core of the CUT to the power supply pad [84, 26, 82]. The current sensor offers dynamic power supply current monitoring and its output can be switched to an amplitude detector, in order to obtain a DC signature that carries information about the RF amplitude of the power supply current. Using two amplitude detectors at the input and output of the CUT we can measure the gain and the 1-dB compression point. Alternatively, the DC signatures of the sensors can be used to perform an alternate test.

A common disadvantage of the loop-back test and sensor-based test is that they require to add on-chip circuits that tap into sensitive RF paths and, thereby, they unavoidably degrade the RF performances. For this reason, these DFT and BIST approaches must be considered early in the design process and the degradation must be compensated during design, in order to meet the intent design specifications. This finds designers rather reluctant since it increases design iterations and it does not allow aggressive design to exploit the features that the technology has to offer.

To this end, non-intrusive BIST techniques have been proposed recently that leave the design intact. The idea is to employ sensors to monitor the CUT while being totally transparent to the CUT, as shown in Fig. 16. Two types of sensors can be considered. The first type consists of variation-aware sensors that include process control monitors (PCMs), such as single layout components (i.e. transistors, capacitors, etc.) and dummy analog stages (i.e. level shifters, bias stages, gain stages, etc.) [28, 82]. If PCMs are placed in close physical proximity to the CUT, then they can offer an image of the process variations affecting the CUT. In this way, measurements on PCMs can track the RF performances since they are both subject to the same inter-die and correlated intra-die process variations. In turn, the RF performances can be implicitly predicted using the alternate test paradigm. This approach can be virtually applied to any RF circuit since any RF circuit can be decomposed into

PCMs. The objective is to layout the PCMs in close physical proximity to the corresponding structures in the RF circuit such that they are well- matched, in order to minimize uncorrelated intra-die process variations.

However, variation-aware sensors cannot detect the presence of defects within the CUT since they are not electrically connected to it. For the purpose of detecting defects, a second type of non-intrusive sensor can be used that is based on temperature monitoring [224, 225, 226, 227, 228]. The underlying observation is that when the CUT operates, part of its electric power is dissipated, that is, it is converted to heat due to the electrothermal Joule effect. The heat is mostly conducted through the silicon substrate and the temperature in a sensing point near a dissipating device of the CUT varies due to the power dissipated. The idea is that a defect will necessarily shift the dissipated power which, in turn, will change the temperature profile close to the CUT. Thus, a temperature sensor can capture this change to indicate the presence of the defect. The heat transfer has a low-pass filter behavior with a time constant defined by the thermal path of a few tens of kHz. It appears that only DC spectral component of the dissipated power induces a temperature variation near the CUT. Nevertheless, since the dissipated power is the product of current flowing through the dissipating device and the voltage across its terminals, this DC component carries information about both the DC biasing and the RF amplitude of the signals. By extension, by measuring temperature near a dissipating device of the CUT, we can monitor both the DC biasing point and RF operation of the CUT.

11 Summary

We presented a concise overview of AMS testing and practical DFT and BIST techniques. The aim of this chapter was to explain basic concepts and provide references where the interested reader can find a more detailed presentation of the material as well as experiments that demonstrate these concepts. Finally, we should note that, in general, we did not include traditional test approaches that have been for many years the practice in industry. These approaches are presented in great detail in [2, 4]. The aim was instead to collect in a comprehensive manner the latest research results in the field and describe techniques that have a high potential and are close to industrialization.

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