Wideband compact antenna for K-band applications

Marjorie Grzeskowiak, Philippe Descamps, Jean Vindevoghel

Active devices such as MESFETs are attractive since they can provide conversion gain as well as mixing operation. This allows the array to send amplified signals towards the source location without including additional amplifiers, which will increase circuit size and cost [4]. In this Letter we present a new phase conjugator with active devices for retrodirective antenna arrays, which also makes it possible to use the same polarisation for both transmitting and receiving when placed in a retrodirective array. This allows each element to be made very small, which is very important since the scanning range of a retrodirective antenna array depends on the array spacing.

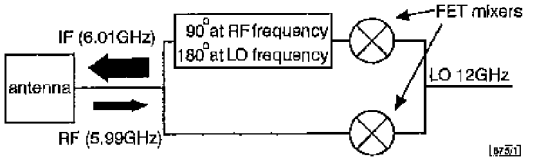

Fig. 1 *Schematic diagram of proposed phase conjugating element*

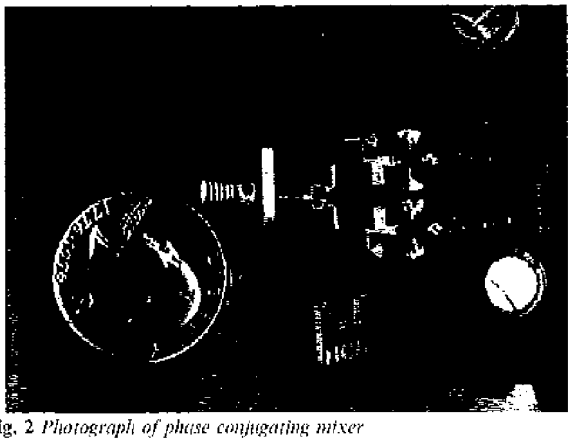

Fig. 2 *Photograph of phase conjugating mixer*

Phase conjugator concept: A schematic diagram of the new dual-channel phase conjugator is shown in Fig. 1. The circuit contains two ports, one for the LO which is applied in phase to the two channels and a second combined RF/IF port. The channels are identical except for a 90° phase delay line at the RF frequency. This delay line causes RF cancellation at the RF/IF port for isolation. Since the LO frequency is twice that of the RF frequency, the LO from the two channels will experience a 180° delay when combined at the RF/IF port, providing good LO isolation. This novel architecture allows an extremely compact design. When placed at the feed of an antenna, the retransmitted signal will have the same polarisation as that of the incoming signal.

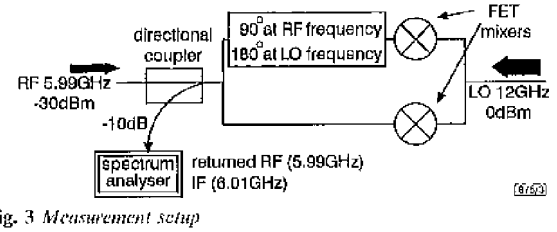

Fig. 3 *Measurement setup*

Circuit performance: A prototype circuit was fabricated on RT/Duroid (25mil thickness, $\varepsilon_r = 10.2$) and is shown in Fig. 2. The circuit performance was tested by using an SMA connector at the RF/IF port instead of an antenna. The measurement setup is shown in Fig. 3. Two synthesisers were used to provide RF (5.99GHz, –30dBm) and LO (12GHz, 0dBm) signals. The signals going towards the output port are tapped off through a directional coupler with 10dB attenuation to a spectrum analyser. As shown in Fig. 4, the circuit achieved an RF/IF isolation of 20dB and a conversion gain of 3.2dB at the output port.

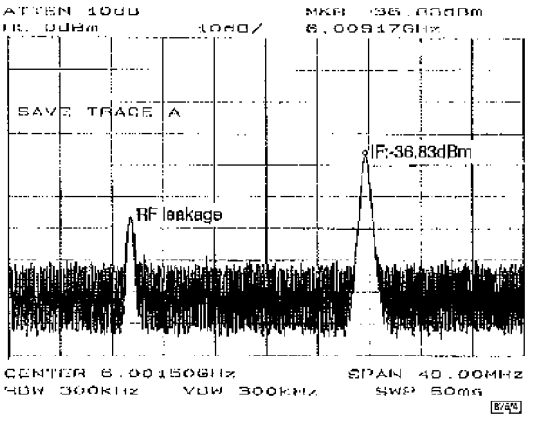

Fig. 4 *Measurement results*

Conclusion: A new compact phase conjugator has been proposed. This new structure allows high RF/IF isolation due to its hybrid structure, and uses FET mixers for conversion gain. The circuit uses one port for both input and output, and shows high RF/IF isolation as well as conversion gain. This compact architecture can be used as the building block for a wide range retrodirective antenna array due to its compactness, which means that it can be easily incorporated into an array, as well as its excellent performance. Current efforts are being directed towards developing a retrodirective array based on this architecture.

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Wideband compact antenna for K-band applications

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A compact coupled microwave active antenna is presented. This antenna is proximity fed, and consists of a square radiating element array on a polymer dielectric layer. The compactness of the antenna is obtained through technological optical processes and the parasitic patch phenomenon which increases the bandwidth.

Introduction: K-band and millimetre-wave active applications, such as tracking or people identification, require compact antenna designs. The use of the proximity-fed antenna in the millimetre-wave range allows small-sized and light antennas to be obtained.

To date, most active multilayer antennas have been realised by fabricating the active components directly on the antenna substrate [1]. To avoid poor connections due to air gaps, and provide an accurate feeding position, the antenna is fully realised by means of photolithography processes. In this Letter we report an integrated proximity-fed antenna array, the configuration of which allows the optimisation of both the antenna and active substrate. The active component substrate is gallium arsenide and the substrate of the antenna is an ultrathick polymer dielectric, Amoco Ultradel 7505 [2] (a photosensitised epoxy resin). To increase the bandwidth, the patches are strongly coupled in the H-plane [3].

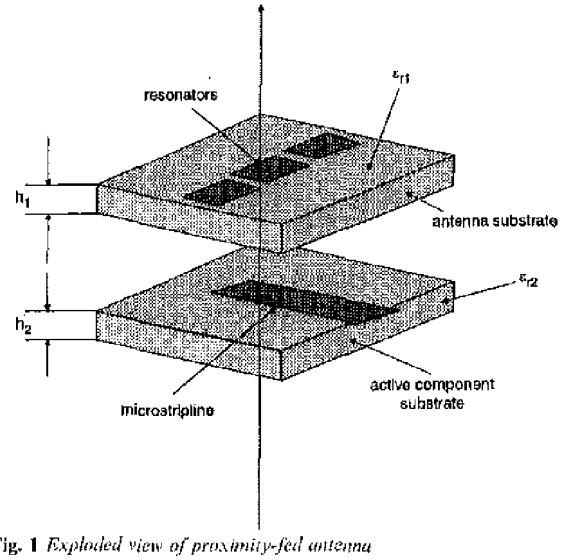

Fig. 1 *Exploded view of proximity-fed antenna*

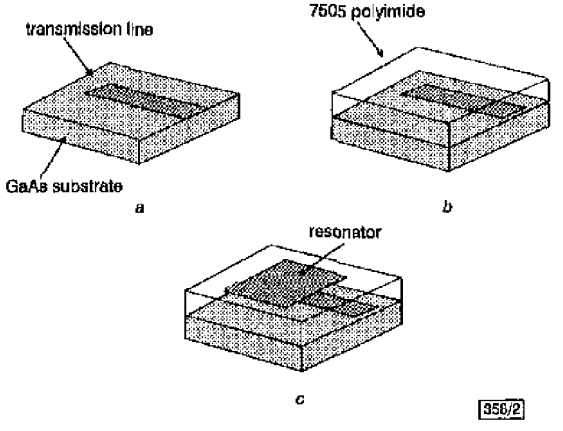

Fig. 2 *Fabrication steps for compact antenna*

Antenna substrate: The antenna design is shown in Fig. 1. The driving patch is electromagnetically coupled to a microstrip line, and is loaded by parasitic patches which form the array of the antenna. These parasitic patches are electromagnetically influence-coupled together and involve an increased bandwidth. The patches are fabricated on a low-loss dielectric substrate with a thickness of $h_2 = 40\mu m$ and a low relative permittivity of $\varepsilon_{r2} = 2$, which provides good radiating efficiency. The transmission lines are fabricated on a high permittivity substrate with thickness $h_1 = 400\mu m$ and a relative permittivity of $\varepsilon_{r1} = 12.8$. The CAD software Ensemble (Boulder, Co) [4] has been used to design the antenna. The dimension of the square resonators is taken to be 1.86mm and their resonant frequency is 26GHz. The distance between the resonators is 0.5mm. The parasitic patches enable the bandwidth to be increased from 600MHz for a single patch to 1.2GHz for a three-element linear array. The dimensions of the feeder are adjusted to match the input impedance of a 50Ω load at the resonant frequency. We obtained a maximum bandwidth of 5% for the array antenna instead of 2.5% for a single resonator.

Antenna fabrication: The fabrication process is shown in Fig. 2. On one side of the GaAs substrate a transmission line is deposited by thermal evaporation of Ti (200Å) and Au (5000Å) (Fig. 2*a*). Polymer 7505 is then applied by spin-coating to achieve the desired thickness of the dielectric (Fig. 2*b*). Following a pre-bake at 100°C on a hotplate, the polymer is exposed to near ultraviolet light. After pre-bake in a 175°C nitrogen oven, we then carry out development using D510 developer, and finally a post-bake on a hotplate at 100°C is carried out for ~3min. The resonators are then deposited on the dielectric by thermal evaporation of Ti and Au (Fig. 2*c*). This final structure can be seen in Fig. 3.

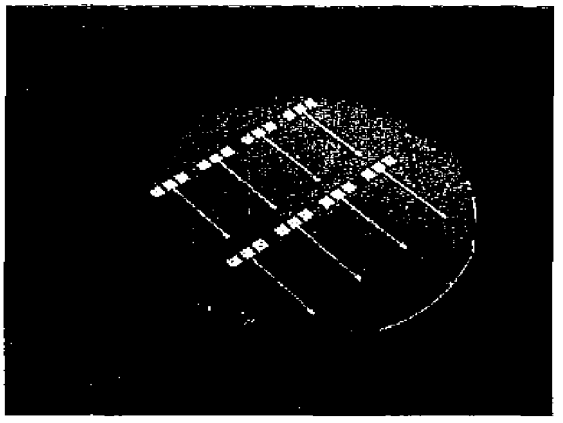

Fig. 3 *Final antennas on 2.5in GaAs wafer (8 times photorepeated)*

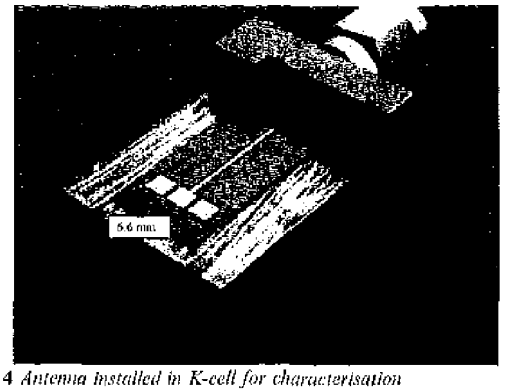

Fig. 4 *Antenna installed in K-cell for characterisation*

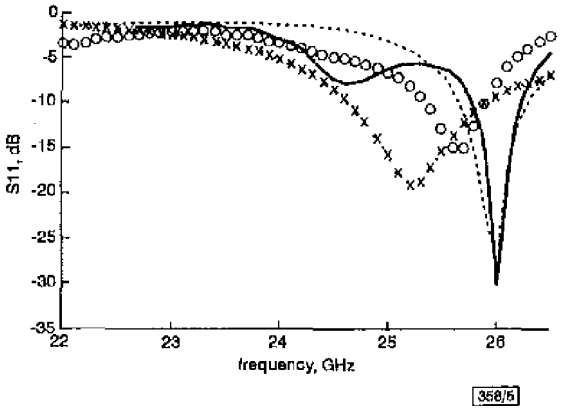

Fig. 5 *S11 parameter measurements*

- - - - simulated (resonator)
—— measured (resonator)
-·-×-·- simulated (array)
-·-○-·- measured (array)

Experimental results: The antenna mounted in a K-cell is shown in Fig. 4. The measured and simulated results are presented in Fig. 5. The measured and simulated frequencies are the same (26GHz) in the case of a single resonator; in the case of the antenna array, a slight discrepancy can be noted (25.7 when meas-

ured instead of 25.2GHz when simulated). The results are presented in Fig. 5.

When the parasitic patches operate, the bandwidth is increased from 400 for a single resonator (1.6%) to 640MHz for an array antenna (2.7%). The adaptation at the resonant frequency ($S11 = -15$dB at 25.7GHz) is not good enough to obtain the expected 1.2GHz bandwidth.

The gain of the array antenna is 3dB at the resonant frequency instead of 5dB as expected. This difference between the simulated and measured results can be explained by a mismatch of the antenna.

Conclusion: We have fabricated a compact monolithic photolithography antenna with a widened bandwidth. The discrepancies between the simulated and measured values of the gain and bandwith can be attributed to rather incomplete knowledge of the losses in the dielectrics. These points have to be investigated further.

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Low-power CMOS current conveyor

A.M. Ismail and A.M. Soliman

A novel second-generation CMOS current conveyor based on a new adaptive biasing technique is proposed. It is shown that the use of this circuit offers an excellent performance and leads to a significant reduction in the standby power dissipation. PSPICE simulation results assuming 0.5μm CMOS process are also given.

Introduction: Although lower supply voltage directly translates to lower power consumption in digital circuits, a similar conclusion cannot be drawn for analogue circuits. Low-power analogue design, therefore, raises its own challenge [1 – 7]. Owing to economic constraints, the standard CMOS technology is suitable for use in many applications. Recently, analogue CMOS current-mode circuits have received a great deal of interest because they can operate under low voltage supplies since the current-mode substitutes current swings for voltage swings in the signal propagation [1 – 3]. The second-generation current conveyor (CCII) is the most versatile building block in current-mode signal processing [1, 2]. Many realisations of the CCII in the literature based on a feedback-stabilised voltage follower have been developed in order to obtain accurate voltage-following action between node Y and node X [4 – 6]. In these realisations, differential amplifiers with high current tails are required to obtain high open-loop gain. This leads to high power consumption in addition to a slew rate limited performance. In this Letter, a novel CMOS realisation based on an adaptively biased differential pair structure is introduced.

Circuit description: Consider the circuit shown in Fig. 1. In this circuit, which is the class AB version of that reported in [4], a negative feedback is applied on two long tail differential pairs (LTP) in such a way as to force them to follow the same value of current driven from the node X. The local feedback actions on the drains of M2 and M3 lead to an exact voltage following with a negligible DC offset and a small input resistance [4]. A sufficiently high current source value I_B should be chosen in order not to limit the maximum current driven from node X.

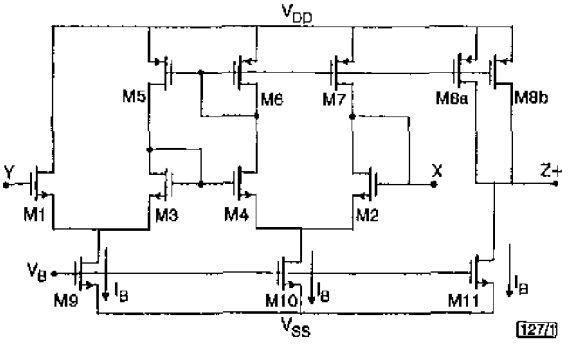

Fig. 1 *Circuit configuration of class AB long tail-based CCII*

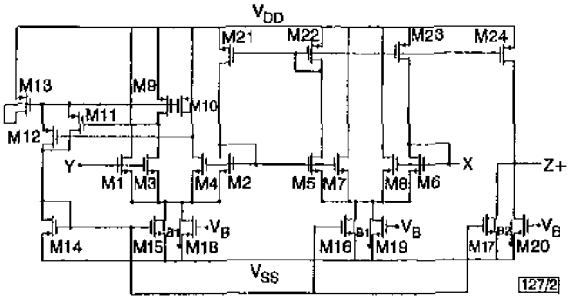

Fig. 2 *Circuit configuration of proposed CCII*

Consider the circuit shown in Fig. 2. Transistors M1–M2 and M5–M6 have the same role as in the circuit shown in Fig. 1. To control the value of the current tails of the two LTP structures, an adaptive biasing action is effected by means of transistors M3–M4, the high-speed current-mode maximum sub-circuit M9–M13 (reported in [7]) and the current mirrors M14–M17. Consequently, the larger the current driven from node X, the higher the biasing current for the two LTPs. Standby current sources (M18–M20) are needed to prevent the LTP structures from turning off, thus avoiding cross-over distortion and frequency response limitation. It is noted that, to obtain low power consumption, the aspect ratios of transistors M3–M4 and M7–M8 are small compared with those for M1–M2 and M5–M6. Also, the aspect ratios of all the remaining transistors are optimised as shown in Table 1. The current at node X is reproduced at node Z+ through current mirrors M17, M20 and M24.

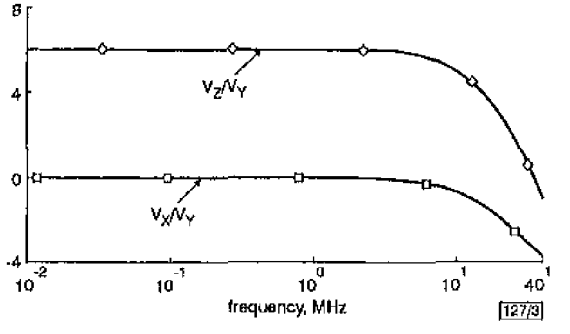

Fig. 3 *Frequency characteristics of CCII*

□ *DB* (*V(x)*)
◇ *DB* (*V(cc)*)