Reduced-Code Techniques for On-Chip Static Linearity Test of SAR ADCs

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***Abstract*—This work presents reduced-code strategies for the static linearity test of successive-approximation analog-to-digital converters. Reduced-code techniques for ADC static linearity test may drastically reduce the test time for static linearity characterization. These techniques take advantage of the repetitive operation of SAR ADCs for reducing the number of necessary measurements for static linearity testing. In this paper we discuss the implementation of these techniques for three widely used SAR ADC topologies. Namely, we consider SAR ADCs based on binary-weighted capacitive DACs, split-capacitor DACs and segmented DACs. The proposed techniques are validated by behavioral simulations on three SAR ADC case studies.**

I. Introduction

In the latest years the integrated successive approximation register (SAR) ADC has become a popular ADC topology. Mainly due to its good compromise between power efficiency and speed, it is used in a diverse range of applications. Additionally, SAR ADCs are digital-friendly topologies that leverage very well the advantages and attenuate the drawbacks of CMOS technology scaling.

However, SAR ADC topologies are very prone to static errors that may degrade their linearity. Static linearity tests are then necessary in order to assure the correct functionality of the converter, but they can be a very demanding and costly task. Indeed, the mixed-signal sections of a complex System-on-Chip (SoC) are amongst the more critical in terms of test time and cost [1]. The standard in industry is the histogram test method, in which the whole set of codes available on the ADC is measured [2]. The main practical issues for an accurate static linearity characterization are the need for an accurate and linear test stimulus that excites the input full-scale of the ADC under test and the very large volume of samples that have to be collected and processed. Indeed, the number of samples to be acquired scales exponentially with the resolution of the ADC. Moreover, each code has to be measured multiple times for averaging noise.

A promising solution to these issues is the development of alternative test techniques to reduce test time in the production line, which may enable a significant speed-up of test time and a consequent reduction of test cost. Moreover, moving part of the test apparatus into the chip in a built-in self-test (BIST) fashion has the potential of further reducing test cost and complexity. In this work we present three reduced-code techniques, suitable for on-chip implementation, that take advantage of the architecture of different SAR ADC topologies in order to reduce the number of required measurements for a full static characterization. In particular, we consider three SAR ADC case studies based on different DAC topologies, namely the binary-weighted capacitive DAC (CDAC), the split-capacitor DAC (SC-DAC), and the segmented DAC.

The rest of the paper is organized as follows. Section II reviews relevant previous work on reduced-code static linearity testing. Section III present the proposed reduced-code techniques for different SAR ADC topologies. Section IV provides general guidelines for a practical on-chip implementation of these techniques. Section V validates the feasibility of the presented reduced-code techniques based on realistic behavioral simulations. Finally, Section VI summarizes our main contributions.

II. Previous Work

In general, reduced-code test methods are based on exploring the repetitive operation of a particular ADC architecture (e.g. SAR, pipeline, cyclic, algorithmic, etc.), where the static errors are correlated and caused by the same set of components. In this line, the work in [3] uses a piecewise ramp in order to excite a carefully selected subset of codes of a SAR ADC under test. The width of the excited codes are measured and then mapped to the complete transfer function and the full static nonlinearity can be inferred. One limitation of this method is that missing codes might not be detected. Also, the generation of the ramp excitation may be challenging in a BIST application. Similar approaches were developed for pipeline ADCs in [4] and [5], while a model-based reduced-code strategy is presented in [6].

The test strategy described in [7] characterizes the static linearity of a capacitive SAR ADC (CDAC ADC) by extracting the weights of each bit from the set of Major Carrier Transitions (MCTs). As an additional advantage, MCTs are internally generated through a modified operation of the SAR ADC without the need of an input stimulus. Measurements are performed using an auxiliary capacitive array for test, in a similar fashion to the approach of self-calibration proposed in [8].

The approach in [9] deals with a differential split-capacitor SAR ADC (SC-SAR ADC) topology. One branch of the

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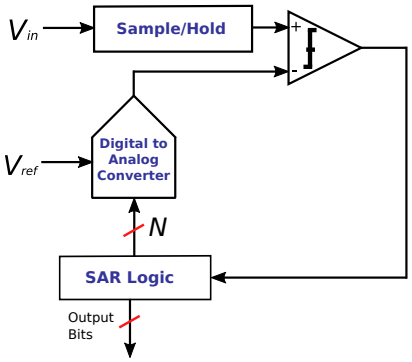

Fig. 1. Conceptual block diagram of a SAR ADC.

differential SC-SAR ADC measures the other, and similarly in [10] for a single-ended case, one of the sub-DACs extracts the bit-weights of the adjacent sub-DAC. The advantage of not needing extra analog circuitry is traded with higher test times, since multiple iterations are needed to converge to an accurate measurement.

In our previous work, we have introduced reduced-code techniques for CDAC and SC-DAC strategies that take advantage of the repetitive operation of these topologies while focusing on an on-chip implementation that may enable a full-BIST implementation [11], [12]. In this paper, we review our previous reduced code solutions, introduce a novel reduced-code technique for the segmented SAR topology, and finally we compare the developed test strategies in terms of test time reduction, implementation complexity and measurement accuracy.

III. Reduced-code techniques for SAR ADCs

A. SAR ADC operation

The block diagram of a generic SAR ADC is shown in Fig. 1. Basically, it consists of a Sample-and-Hold (S/H), comparator, DAC and digital control logic. Its operation relies on a binary search. In the first cycle, the input is sampled and the logic sets the DAC voltage to the mid-range. The DAC is used to approximate the analog input voltage by performing an iterative approximation search. The DAC code in the last iteration is the converted digital output. In general, an N-bit SAR ADC takes N successive approximation cycles for converting a given input sample.

In a first-order approximation, the static performance of a SAR ADC is primarily dependent on the DAC accuracy. The comparator will add offset and gain errors, which can be easily corrected in post-processing. Thus, by characterizing the static linearity of the DAC, it should be possible to estimate the linearity of the complete SAR ADC. This has the additional advantage of not requiring an analog input stimulus, since the DAC inputs are purely digital and can be easily programmed by modifying the SAR logic. This makes this solution very appealing for on-chip implementations since on-chip analog stimulus generators are complex to design and usually demand a higher linearity than the ADC under test [13]–[15].

In our work we propose to take advantage of the architecture of the DAC in order to define efficient reduced-code linearity test techniques for SAR ADCs. In particular, we will consider three ubiquitous SAR ADC topologies using CDAC arrays, SC-DAC arrays and segmented DACs. In this line, CDAC and SC-DAC arrays are binary-weighted DACs that can be fully characterized by adapting techniques based on Major Carrier Transitions (MCTs), while segmented DACs can take advantage of their inherent segmented operation to reduce the number of necessary measurements.

B. MCT-based reduced-code techniques

Let us first review briefly the MCT-based approach, that we introduced before in [11], [12] and that is suitable for binary-weighted DACs such as CDACs and SC-DACs. For illustration, Fig. 2a and b show conceptual block diagrams for SAR ADCs based on CDACs and SC-DACs, respectively. If we consider an N-bit DAC, we can define N MCTs, where the i-th MCT is defined as the transition from code $2^i - 1$ to code 2^i [16].

Neglecting the offset voltage, the output voltage V_{DAC} of a binary-weighted DAC can be written as

$$V_{DAC}(D_{N-1}...D_0) = D_{N-1}W_{N-1}+...+D_1W_1+D_0W_0, \quad (1)$$

where the weights W_i are determined by the DAC capacitor ratios and the input binary code is $D_{N-1}D_{N-2}...D_0$. Note that by performing only N measurements it would be possible to reconstruct its full transfer function. The most direct approach to achieve that is by setting $D_i = 1$ and all the remaining bits to 0, and calculating W_i for $i = 0, ..., N-1$. Alternatively, it is also possible to measure the code widths associated to the MCTs of the CDAC by measuring the voltage difference V_i between codes 2^i and $2^i - 1$. Then, the values of W_i can be computed by simple manipulation of equation (1), as detailed in [16]. This alternative measurement strategy has the advantage that the code widths are expected to be relatively constant, which allows to adjust the Full Scale (FS) of the measurement instrument for an accurate characterization.

This MCT-based test methodology can be directly applied to the CDAC SAR ADC in Fig. 2a, just by monitoring the output of the binary-weighted DAC, labelled V_X in the figure, and programming the CDAC for generating the code widths associated to the MCTs. As detailed in [7], [11], the voltage corresponding to the i-th transition is generated by performing the following steps. First, the bottom plate of the capacitor C_i is charged to V_{ref} while all other capacitors in the DAC are grounded. After that step, the usual SAR operation is performed using capacitors C_{i-1} to C_0, while the bottom plate of C_i is connected to ground. At the end of this modified SAR operation, it can be shown that V_X converges to the code width of the MCT related to the i-th transition, while the output binary code carries the information related to the missing codes. It is important to remark that this modified SAR operation for generating the widths of the codes associated to the MCTs allows the detection of missing codes, as described in [11].

A similar reduced-code strategy can be developed for the SC-SAR ADCs as the one in Fig. 2b, but in this scenario we

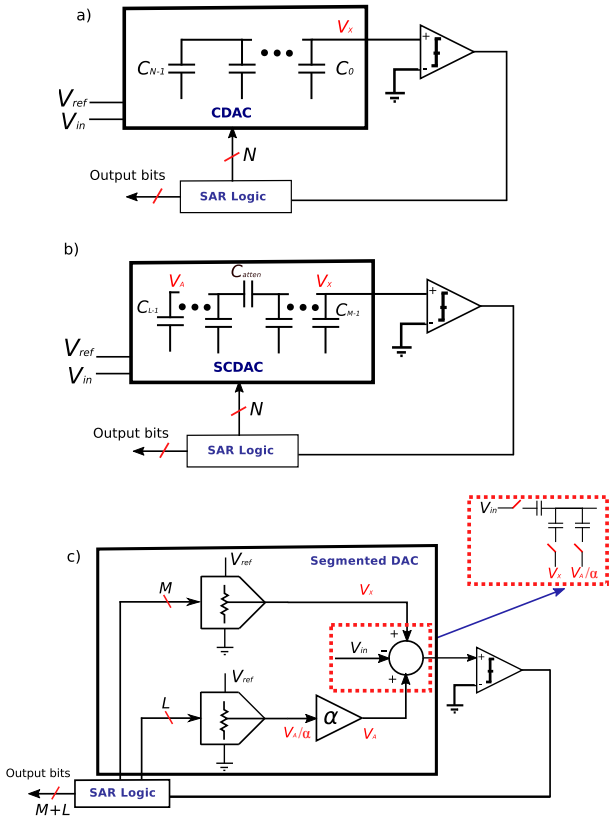

Fig. 2. Conceptual schematics of the three different SAR topologies studied in this work based on its DAC topology: a) binary-weighted capacitive DAC, b) split-capacitor DAC and c) segmented DAC.

can take advantage of the scaling due to the bridge capacitor and measure each partial CDAC independently. Thus, instead of monitoring only V_X, we can monitor node voltages V_X and V_A, relaxing the requirements on the acquisition instrument. It is important to note that even though the partial CDACs are being measured separately, the mismatches of the adjacent CDAC and bridge capacitor are taken into account because their equivalent capacitance has influence on the linearity of each CDAC segment. As an additional advantage, the partial MCTs can be generated in only two clock cycles, without the need of modified SAR operation, while the detection of missing codes can be performed in the digital domain as a post-processing stage [12].

C. Superposition-based reduced-code techniques

A segmented DAC is composed of a number of low-resolution DAC stages, whose LSB is scaled in a way that the outputs can be combined to form a higher resolution DAC. For instance if we consider two $(N/2)$-bit DACs, one "fine" DAC whose LSB is equal to 1 and a "coarse" DAC whose LSB is equal to $2^{N/2}$, we can build a N-resolution DAC just by summing the outputs of both fine and coarse DACs. In order to provide a practical example, Fig. 2c shows a conceptual block diagram of a SAR ADC based on a segmented DAC. In this topology, the binary search is performed using each of the resistive sub-DACs while the relative scaling of the fine and coarse DAC LSBs is achieved by a capacitive divider. This capacitive array is also responsible for sampling the input.

MCT-based reduced-code techniques are not appropriate for testing segmented DACs where coarse and fine DACs are usually built using a thermometer-code resistive divider rather than a binary-weighted structure. Instead of that we propose to measure all the codes of each partial DAC independently and then use superposition to infer the full characteristic of the composite DAC.

In a general case where we have an L-resolution fine DAC and an M-resolution coarse DAC, a full all-code linearity test would take at least 2^{L+M} measurements. However, by performing two partial all-code tests, the total number of measurements is reduced to $2^M + 2^L$ highly reducing the total test time. After the sub-DAC voltages are measured, the actual output can be reconstructed by adding the coarse and fine contributions [16]

$$\begin{aligned} V_{DAC}(i) \quad = \quad & V_{DAC}^{FINE}(i \ \& \ 0...001...11) \\ & + V_{DAC}^{COARSE}\left(\frac{i \ \& \ 1...110...00}{2^L}\right), \end{aligned} \tag{2}$$

where V_{DAC}^{FINE} is the LSB DAC contribution, V_{DAC}^{COARSE} is the MSB DAC contribution and $\&$ is the AND bitwise operator.

IV. Practical BIST Implementation

The proposed reduced-code static test strategies have the advantage of not requiring a test stimulus. This greatly simplifies the on-chip implementation of the technique and opens the door to an efficient full-BIST approach. A general block diagram of an on-chip implementation of the proposed test methodology is illustrated in Fig. 3. During test mode, switch S is closed and the output voltage of the DAC is digitized by an embedded instrument. This digitized voltage is further post-processed by a digital circuit to compute the static linearity performance of the DAC from the reduced-code measurements. The key element for the on-chip implementation of the proposed technique is this embedded test instrument that acquires and digitizes the DAC output voltages.

A suitable candidate for performing this task is a first-order IΣΔ ADC, which, conceptually, is a mix between a dual-slope and a ΣΔ ADC [17]. This topology is suited for measuring DC voltages such as in digital voltmeters and instrumentation and measurement applications, while the simplicity of the circuitry makes it suitable for BIST applications. Moreover, for a switched-capacitor implementation, it is possible to merge the input sampling capacitor of the IΣΔ ADC with the capacitor array in the SAR ADC. For the three topologies discussed in this paper, this can be done by reusing the CDAC, SC-DAC, or capacitive divider arrays by using the same operation principle of a multiplying DAC (MDAC) [18], which further reduces the overhead and simplifies the implementation.

With respect to the resolution and the FS of the IΣΔ ADC, a good trade-off is to relax the resolution of the IΣΔ while adjusting its FS to the magnitude of the target measurements, in such a way that the effective resolution of the IΣΔ, compared to the resolution of the ADC under test is larger. In

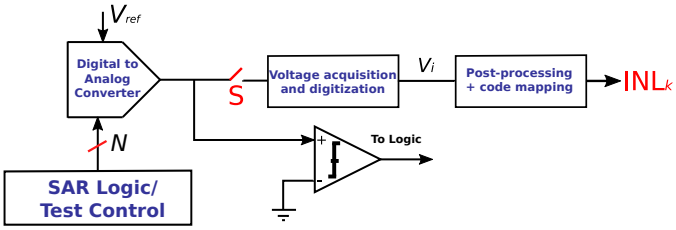

Fig. 3. Conceptual block diagram of the proposed embedded reduced-code linearity test setup.

order to provide some guidelines for the system-level design of the IΣΔ ADC, the following subsections discuss the trade-offs between the resolution and FS of the IΣΔ ADC and the test time savings derived from the reduced-code techniques, for the three considered ADC topologies.

A. CDAC SAR ADC

Regarding the CDAC SAR ADC in Fig. 2a, during test mode the IΣΔ ADC is connected directly to node V_X and the CDAC is operated to generate the widths of the codes associated to the MCTs as detailed in [7], [11]. The FS of the IΣΔ can be then easily estimated by determining the worst case MCT code width as

$$A_{max} \approx \frac{V_{ref}}{2^N}\left(1+3\sigma\sqrt{2^N-1}\right), \tag{3}$$

where σ is the standard deviation of the unit element capacitor due to mismatch and V_{ref} is the SAR ADC reference voltage (that is reused for the IΣΔ ADC). Then the FS of the IΣΔ can be designed as $\mathrm{FS}_{I\Sigma\Delta} = \xi A_{max}$, where $\xi > 1$ is a scaling factor introduced in order to provide an extra design margin.

Taking into account the conversion time of each of the IΣΔ measurements, the test time for a complete static linearity characterization can be also estimated. Applying the measurement algorithm in [11] for the CDAC SAR ADC in Fig. 2a, test time can be expressed as,

$$T_{CDAC} = T_{ck}2^{R-1}(N^2+N+4), \tag{4}$$

where T_{ck} is the clock period (assuming that both the SAR ADC under test and the IΣΔ ADC share the same clock for simplicity) and R is the resolution of the IΣΔ ADC. It should be noticed that this is a lower limit value, since in a practical implementation the clock frequency of the IΣΔ modulator may be decreased to reduce the complexity of the BIST design.

B. SC-DAC SAR ADC

For the SC-SAR ADC in Fig. 2b the idea is similar with the particularities addressed in section III-B. During test mode, the embedded IΣΔ ADC is first connected to the V_X node and the SC-DAC array is programmed to generate the code widths of the MCTs corresponding to the MSB section of the array as detailed in [12]. Subsequently, the IΣΔ ADC is connected to node V_A and the SC-DAC array generates the code widths of the MCTs for the LSB section. The FS of the IΣΔ ADC can be designed following the same guidelines by adjusting the FS to the magnitude of the partial MCTs. Total test time can be estimated as,

$$T_{SC\text{-}DAC} = 3T_{ck}2^R N. \tag{5}$$

It has to be noted that MCT generation is faster for the SC-DAC in comparison to the CDAC, as detailed in [12].

C. Segmented DAC SAR ADC

Regarding the segmented DAC SAR ADC in Fig. 2c, we propose a reduced-code technique that applies superposition of the all-code measurements of each individual sub-DAC. During test mode the IΣΔ ADC is subsequently connected to nodes V_X and V_A for characterizing the MSB and LSB DAC segments, respectively. In this case the FS of the IΣΔ ADC can be separately adjusted to match the output range of the MSB and LSB sub-DACs. For the MSB sub-DAC the maximum output voltage to be measured can be expressed as $V_{ref}(2^M-1)/2^M$. For the LSB sub-DAC the maximum output voltage is scaled by a factor of 2^L, which alleviates the constraints on the BIST instrument. Even if making the FS programmable adds further complexity to the design, the proposed reduced-code technique offers a significant reduction of static linearity test time. The total test time for a full static linearity characterization can be expressed as

$$T_{SEG} = T_{ck}\left(2^{M+R_{MSB}} + 2^{L+R_{LSB}}\right). \tag{6}$$

where R_{MSB} and R_{LSB} are the resolution of the IΣΔ ADC for measuring the MSB and LSB segments, respectively. This reflects the fact that the FS of the IΣΔ is independently adjusted for each segment.

It has to be noted that for this topology, the quantization error introduced by the IΣΔ for the measurement of the MSB sub-DAC can significantly degrade the measurement. Thus R_{MSB} has to be designed so that the quantization error is negligible in comparison to one LSB of the complete N-bit ADC.

In oder to provide a visual comparison of the potential test time reduction for the presented reduced-code techniques, Figs. 4a,b show the time savings with respect to a complete 128 hits-per-code histogram test as a function of the SAR under test resolution. As an illustrative example, the resolution of the IΣΔ is kept constant as 6 bits for the two MCT-based tests and as 14-bits/10-bits for the MSB/LSB, respectively, for the segmented architecture. It can be observed that, as expected, the superposition-based method yields the longest test time. However, it is still considerably faster than the complete histogram test. Note also that as the resolution N increases the relative savings in test time improves.

V. Results

The feasibility and performance of the proposed reduced-code static linearity test techniques were verified by realistic behavioral simulations of three SAR ADCs with embedded first-order IΣΔ ADCs. The proposed case studies include a 10-bit CDAC SAR ADC, a 6×4 SC-DAC SAR ADC, and

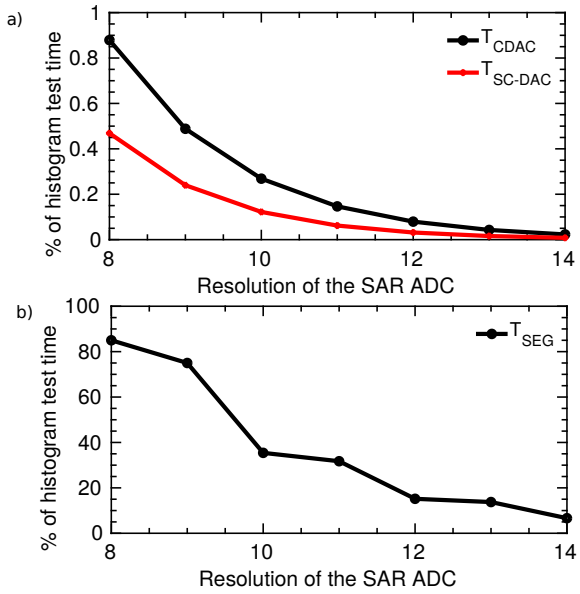

Fig. 4. Comparison between test time of different topologies in comparison to 128 hits-per-code histogram test, using: a) 6-bit IΣΔ for MCT-based test and b) 14/10-bit IΣΔ for superposition-based test.

a 5×5 segmented SAR ADC based on resistive-divider sub-DACs. The IΣΔ ADC for each case study was dimensioned as described in the previous section. For the two purely capacitive architectures the resolution of the IΣΔ ADC is set to 6 bits. For the segmented case the resolution is set to $14/10$ bits for characterizing the MSB/LSB segments, respectively. As previously explained, this value is chosen in order to make sure the quantization error is negligible and does not compromise the overall test accuracy. Behavioral models were implemented in Matlab using the guidelines in [19].

Fig. 5 shows the obtained INL measurements for the three case studies obtained both by a complete 128 hits-per-code histogram and by applying the proposed reduced-code technique. These simulations were performed for typical mismatch values in nanometric technologies. Capacitor mismatch was modeled with σ=0.3 %, and resistor mismatch is set to σ=1 %. The INL estimation error is illustrated in Fig. 6. It is obtained by calculating the difference between the INLs retrieved by histogram and reduced-code methods. As it can be observed, the test results for the reduced test methodologies are very close to the results obtained with the all-code histogram tests. Total test times were 0.27 %, 0.12 %, and 35.42 % of the 128 hits-per-code linear histogram test time for the CDAC, SC-DAC and segmented DAC SAR ADCs, respectively. However, it is convenient to remark that these test estimations are optimistic, since a practical implementation may require to clock the IΣΔ modulator at a lower frequency to relax the design effort of the BIST circuitry.

Finally, Fig. 7 illustrates the effect of the IΣΔ ADC resolution in the accuracy of the INL estimation. Since the constraints for the segmented-based SAR ADC are more stringent for the MSB segment, we fix R_{LSB}=10 bits and sweep R_{MSB}. As it was previously discussed, it can be observed that for the MCT-based methodology Fig. 7a confirms that the scaling of

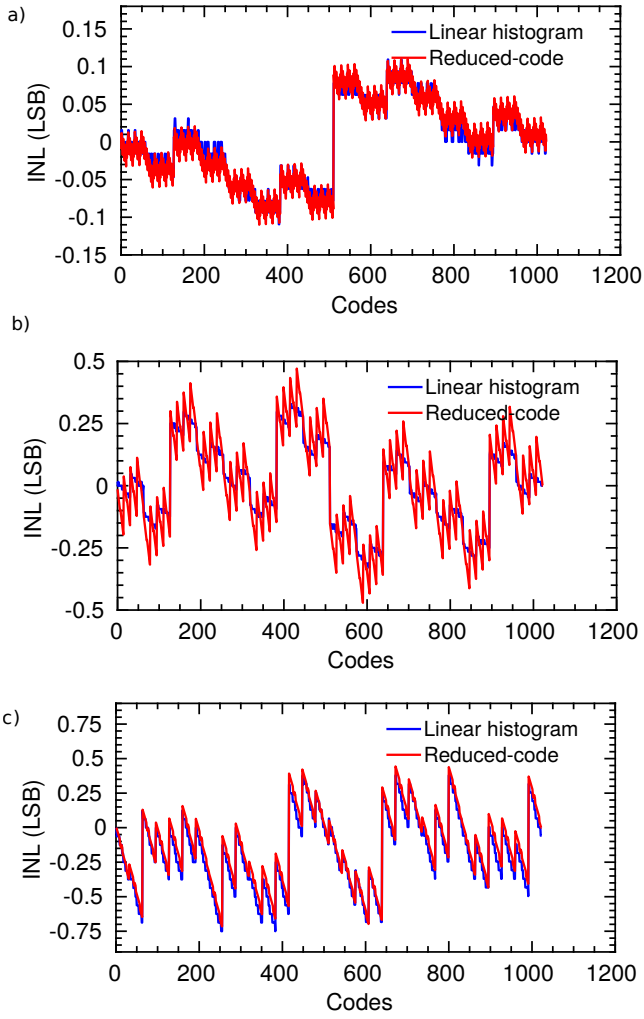

Fig. 5. INL results for histogram and reduced-code test for the three considered SAR ADC architectures: a) binary-weighted capacitive DAC, b) split-capacitor DAC and c) segmented DAC.

the FS relieves the constraints for the embedded instrument. In contrast to that, Fig. 7b confirms that for the segmented-based technique the IΣΔ has to be designed with a resolution that is larger than the SAR ADC itself in order to mitigate the measurement errors. It is also important to observe that errors are higher when characterizing the SC-DAC SAR ADC in comparison to the CDAC SAR ADC, mainly due to error accumulation between the required partial measurements.

VI. Conclusion

This work presented three reduced-code test strategies for three different SAR ADC topologies and discussed their practical on-chip implementation. Namely, two reduced-code techniques based on the measurement of MCTs and one based on the superposition principle were presented for the static linearity test of CDAC, SC-DAC and segmented SAR ADCs, respectively. The proposed test techniques do not need an analog test stimulus, simplifying its practical implementation. It has been shown that the complete static linearity

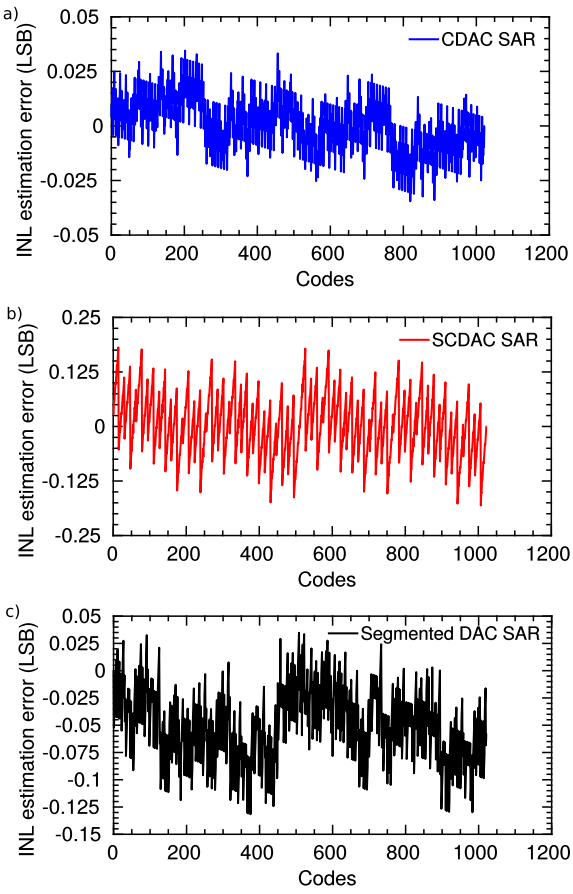

Fig. 6. INL estimation error results for histogram and reduced-code test for the three considered SAR ADC architectures: a) binary-weighted capacitive DAC, b) split-capacitor DAC and c) segmented DAC.

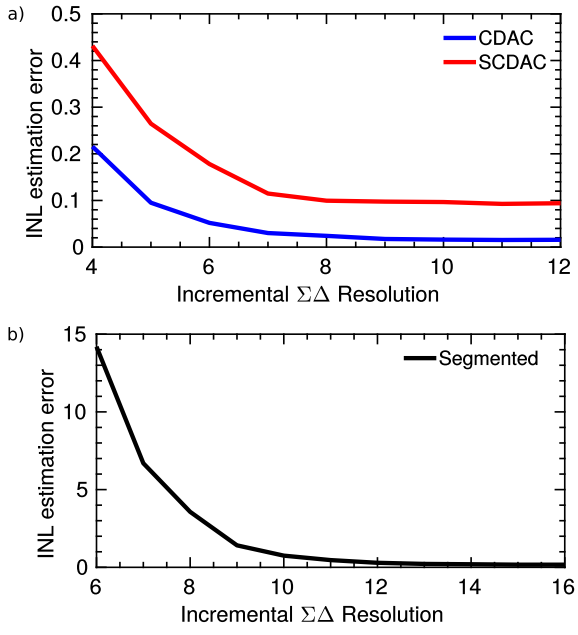

Fig. 7. INL estimation error results as a function of the resolution of the IΣΔ for the three considered SAR ADC architectures: a) binary-weighted and split-capacitor DACs and b) segmented DAC ($R_{LSB} = 10$ bits).

characteristic of an N-bit SAR ADC can be inferred with only N measurements for MCT-based test and $2^M + 2^L$ measurements for segmented test, which may yield significant test time reductions. Obtained simulation results show that INL estimation errors were contained while significant test time savings are achieved. Future work in this line includes the extension of the proposed test techniques for calibration purposes and the fabrication of integrated demonstrators for validating our approach experimentally.

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