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Realization of a High Current and Low R_{ON} 600V Current Limiting Device

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Keywords : 4H-SiC, MOSFET, Current Limiting Device, Simulation, I-V Characteristics, Forward Current Density, Saturation.

Abstract. The first experimental results of a 600 V 4H-SiC current limiting device are shown. This device limits the current as the bias voltage increases. The forward conduction is ensured by an N type implanted channel (doping species: nitrogen) on top of a P^+ implanted layer (doping species: aluminum). The prototypes reach a saturation current density of **900 Acm^{-2}**, with a specific on-resistance of **13 mWcm^2.** The 4H-SiC current limiting devices belong to the best set of Accu-MOSFETs devices reported in the literature.

Introduction

Silicon carbide technologies for the manufacturing of power devices seem to be promising in the near future. The first SiC power devices commercially available are Schottky diodes proposed by Infineon technologies (ranging: 300 V / 10 A and 600 V / 4-6 A) and Microsemi. In the field of the SiC switches, the current trends are the Accu-MOSFET and JFET structures which exhibit the best specific on-resistance/breakdown voltage ratio experimentally obtained (Accu-MOSFET: 16 mΩcm^2/1600 V [1] ; JFET: 10 mΩcm^2/600 V [2], 14 mΩcm^2/1800 V [2]). The physical properties of SiC allow to develop new solid state devices for applications not covered by the silicon technologies. In this sense, a silicon carbide current limiting component should be a solid state structure which has to work under high voltage and high temperature conditions when a short-circuit current appears. The function requires to limit a short-circuit overcurrent during a time long enough to allow the opening of the power line by a circuit breaker under reliable conditions. Such a 4H-SiC component corresponding to the End User specified requirements (600 V / 50 A) led to the definition of the device technological parameters assisted by the finite-element simulation software DESSIS ISE® developed by ISE™ TCAD [3]. The electrical static behavior of the first process run, realised at CNM (Barcelona), are discussed and led us to change some technological parameters in order to reduce the specific on-resistance and increase the saturation current density.

Device structure, simulation and technology

The design of the component is based on an Accu-MOSFET device whose structure is presented in Fig. 1. The wafer is composed by a N^{++} substrate layer (ρ =20 mΩ.cm / 430 µm) on which a N type epitaxial layer (4×10^{15} cm^{-3} / 7 µm) was grown (purchased from CREE Research). A single Al implantation is used for the realization of the buried P^+ region and the guard ring protection. Then, a full wafer multiple N implantation is processed to implement the N-channel (the N implantation come over the Al implantation, so the N-channel is a high compensated N-layer). After that, N^{++} implantation for ohmic source contact, SiC etching to reach the P^+ layer, dry oxidation and both side metallization are processed to manufacture the device without passivation layer. In case of positive drain to source voltage bias, the conduction current is carried by the electrons whose path inside the device crosses the entire thickness of the wafer, the 'intercell' region and the channel region successively. Fig. 1 shows the device structure with its guard ring protection.

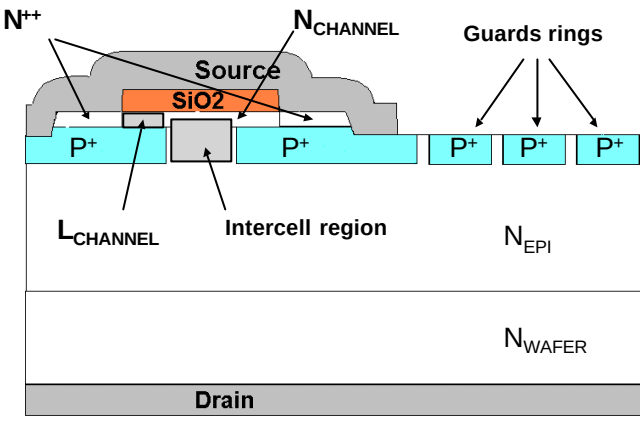

Fig. 1: Vertical cross section of the device and its guard ring peripheral protection (the channel region, $L_{CHANNEL}$, and the 'intercell' region are noted).

For a drain to source voltage V_{DS}>0 V, the drain to source current I_{DS} increases linearly with V_{DS}. When the device reached the saturation mode, the current can not increase any more because the reverse space charge region of the $P^+/N_{CHANNEL}$ junction is wide enough to pinch-off the channel. Consequently, the device is normally-on and the current limiting behavior is unidirectional (for V_{DS}>0 V). Electrical simulations, with DESSIS ISE® [3], were performed [4] to optimize the structure characteristics : low on-resistance (10-20 mΩcm^2) and high saturation current density (500-1000 Acm^{-2}). The technological choices led to a 6 mask levels process using standard process steps commonly used in a Si clean room except for the high temperature post-implantation annealing which is realized in our specific annealing equipment. The device voltage handling capability is 700 V with the specified epitaxial layer and a non optimized guard ring protection. The expected I-V characteristics given by a DESSIS ISE® simulation using implanted doping profiles simulated by a specific software developed by E. Morvan [5] are shown in Fig. 2 (P^+: 350 keV/4×10^{13} cm^{-2} ; $N_{CHANNEL}$: 30-180 keV/1.3×10^{13} cm^{-2}).

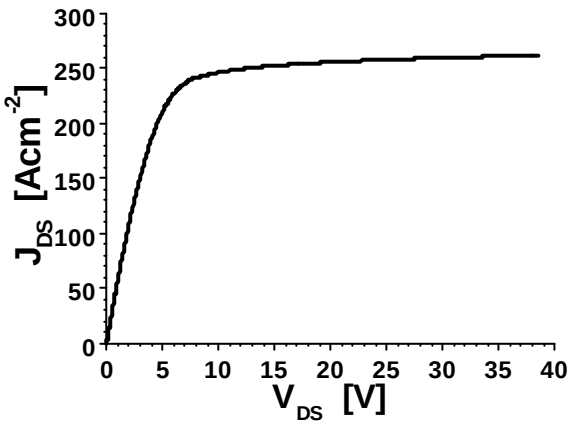

Fig. 2: Device static I-V simulation results obtained by DESSIS ISE® on a limiting device with the following parameters: (P^+: 350 keV/4×10^{13} cm^{-2} ; $N_{CHANNEL}$: 30-180 keV/1.3×10^{13} cm^{-2}).

Experimental results

The prototypes are designed following a multiple hexagonal cells device, with different values of the channel length (4, 5 and 6 µm) and the 'intercell' width (4, 6 and 8 µm) (see Fig. 1). The active area (surface of the source contact) is about 0.05 mm^2 and the conduction perimeter is 2880 µm.

In the first batch prototypes, ohmic contacts are made with nickel and annealed at 850°C. The 'gate' oxide thickness is about 90 nm and the post-implantation annealing process used is 1700°C during 30 min in an inductive furnace. The electrical characteristics were measured using a Keithley K237 (P_{MAX}=10 W that means a 100 mA/100 V range). The best devices show a normally-on behavior with a high specific on-

resistance (R_{ON-SPE}) of 150 mΩcm^2 and a saturation current density of 150 Acm^{-2}. We observe a very soft saturation region as shown in the I-V characteristics of Fig. 3. The specific on-resistances obtained are very high compared to the expected value (10-20 mΩcm^2) (Fig. 2) and the saturation current region is not clearly demonstrated.

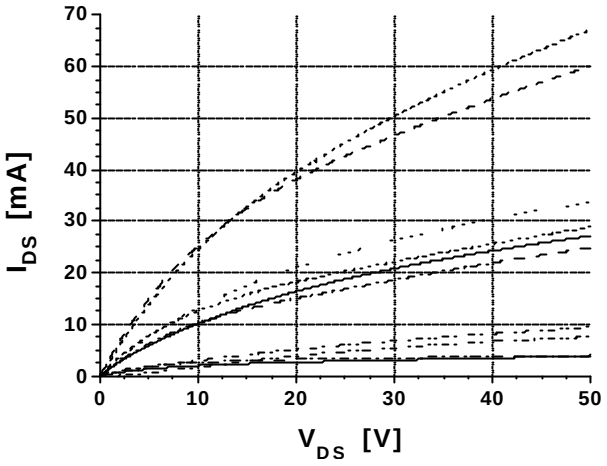

Fig. 3: Sampling of different I-V static characteristics obtained on limiting devices from the first batch (25°C).

SIMS (Secondary Ion Mass Spectroscopy) analysis indicate a channel depth of 0.1 µm with an average doping level of 2D10^{17} cm^{-3}. TLM (Transmission Line Method) measurements combined with the doping profiles (extracted from the SIMS profiles) allow us to estimate a channel electron mobility of 100 cm^{2}V^{-1}s^{-1}. The effective charge density at the SiO_2/4H-SiC interface were extracted from C-V measurements and are found to be negative in the 1.5-2D10^{12} cm^{-2} range. This explains the normally-off behavior of most devices (SiO_2/4H-SiC interface charge density is close to the channel dose, 2D10^{12} cm^{-2}). To improve the device characteristics, some technological changes were used for the second prototypes realization. The static I-V characteristics (measured with a Tektronix 370 curve tracer) of the second run prototypes show a very good behavior. The effects of the channel length and the intercell width are clearly visible and indicate that the intercell width has a low effect on $R_{ON-SPE,}$ but decreasing $L_{CHANNEL}$ lead to clearly decrease R_{ON-SPE}. The best specific on-resistances measured are in the 13-17 mΩ cm^2 range (Fig. 4) and the highest saturation current density is 900 A cm^{-2} (Fig. 5), obtained for the devices designed with a channel length of 4 µm and an intercell width of 8 µm. These results are not so far from the DESSIS ISE® simulations performed with the second run projected technological data. Further analysis will be necessary to extract the channel mobility and the SiO_2/4H-SiC interface charge density. Nevertheless, it seems that a high channel electron mobility (close to the simulation value, 400 cm^{2}V^{-1}s^{-1}) is obtained with a low level of SiO_2/4H-SiC interface charge density, when comparing the simulated I-V characteristic (without SiO_2/4H-SiC interface charge density specification) and the corresponding experimental results of Fig. 5.

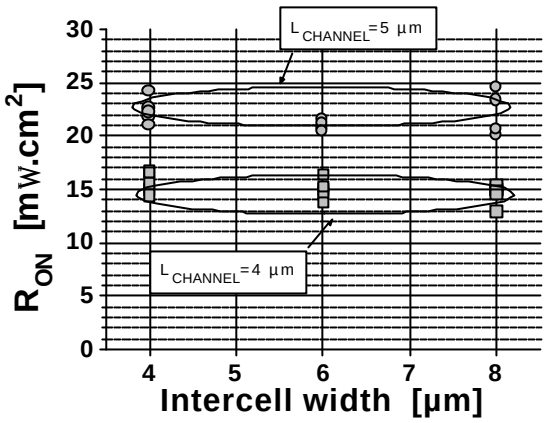

Fig. 4: Experimental Specific on-resistance plotted versus the intercell width.

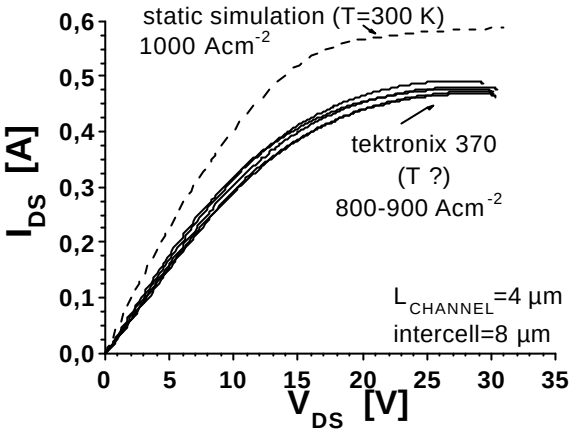

Fig. 5: Simulation/experiment comparison for current limiting devices (channel length: 4 µm / intercell width: 8 µm). For the experimental results using the Tektronix 370 curve tracer, the temperature inside the device, particularly at the end of the channel, is unknown due to self heating (I-V characteristic was limited to 30 V to avoid the device destruction. The 600 V capability should require a pulsed method to avoid self heating and show the real I-V static characteristic).

Conclusion

In this paper we presented the first experimental results of a new normally-on Accu-MOSFET for current limitation applications. The fabricated devices show a very high saturation current density (**900 Acm^{-2}**) and a low specific on-resistance (**13 mW cm^2**) without gate drive, close to the best characteristics reported for a JFET device [2] for the 600 V breakdown voltage range. The fabrication-technology used is based on an implanted channel and only 6 mask levels are necessary.

Acknowledgment

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[3] ISE Integrated System Engineering, DESSIS, Operator's manual
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