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Compatibility of VJFET Technology to MESFET Fabrication and its Interest to System Integration : Fabrication of 6H and 4H-SiC 110V Lateral MESFET.

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Keywords : MESFET, VJFET, Technology compatibility, system integration

Abstract. Integration of Power devices with their control circuitry is a usual challenge in Si and SiC technologies to increase efficiency of power switch and systems. The purpose of this article is to evaluate the integration compatibility of lateral MESFETs within a Vertical power JFET fabrication technology. The interest of this method is to allow control circuitry based on MESFET devices to get both power devices and control circuits on the same die. Several possibilities can be foreseen for the realization of lateral SiC-MESFETs [1], using conductive substrates or semi-insulating wafers. Other possibilities, more compatible with a vertical power device process, are P and N well formation by ion implantation to form the lateral channel. The description of the fabrication process presented below is a part of the fabrication process of a VJFET designed for high voltage current limitation [2]. High energy implantation, RIE etching adjustment and metal contact annealing are the critical steps of the fabrication of this device and will be developed in the process description. Electrical characterization of fabricated MESFET exhibit specific on resistance of 38mΩ.cm² and a transconductance value of 0,4 $mS.mm^{-1}$. These results demonstrate VJFET and MESFET fabrication technology compatibility. Keys points to improve for the next generation of devices will be presented as well.

Introduction

Getting both power devices and their associated control circuitry on same die is interesting in terms of efficiency, reducing chips interconnections number subject to both thermal and mechanical stress leading to component failure. A solution to avoid this is to get both power and control on the same wafer. SOI offers solution and lateral power devices have been done with both power and control on the same chip. Unfortunately, those kind of devices are usually designed for low voltage components. Using vertical devices such as VJFET, Thysristor or IGBT allows fabrication of high voltage devices. Getting both high voltage components and its command let us implement intelligent devices such as self protected IGBT against short circuit, or cascode association one same chip. Several solution can be foreseen to realize such components on the same die : connection by bonding, wafer bonding, stack with vertical connection, local SOI zone formation on a vertical component. The challenge consists in the reduction of the number of fabrication steps combined with high efficiency of the completed device.

1. VJFET and MESFET Fabrication Compatibility.

The *fabrication compatibility* between a VJFET and a lateral MESFET with a *reduced number of mask* is presented below. Figures 1 and 2 presents cross sections of the VJFET and lateral MESFET and their similarities.

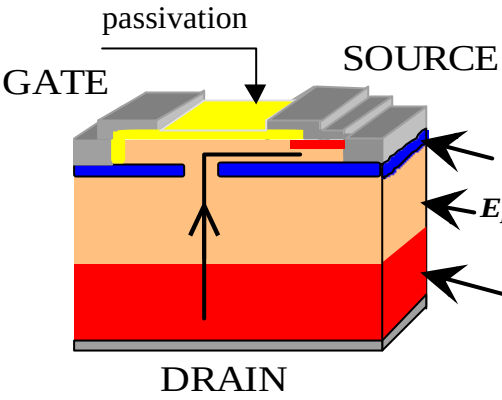

Fig. 1 Cross section of the VJFET.

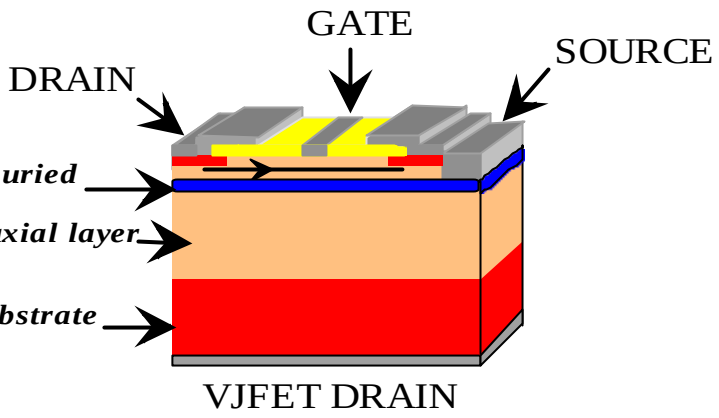

Fig. 2 Cross section of the MESFET.

Those matches enables the potential realization of both components at same time. The p-type buried layer doesn't have the same role in each device. In the case of the VJFET, it allows current limitation with surface channel definition and a lateral control of the current while applying a bias voltage between gate and source. Regarding the MESFET, the function of the p-type buried layer consist of insulation from the wafer and pinch off of the horizontal channel in conjunction with then Schottky gate action.

2. MESFET Operation.

Parameters such as channel doping concentration have been fixed by the design of the VJFET. We have designed the gate of the MESFET considering fabrication capabilities. The source electrode is connected to the p-type buried layer in order to control the gate bias voltage.
Without gate bias applied, the MESFET is normally on. Rising the drain bias will cause reverse bias of the pn junction formed between the p-type buried layer and surface channel resulting in a local extension of space charge and the saturation of the current. An ISE-TCAD simulated result view illustrate the mechanism of saturation of the current (figure 3).

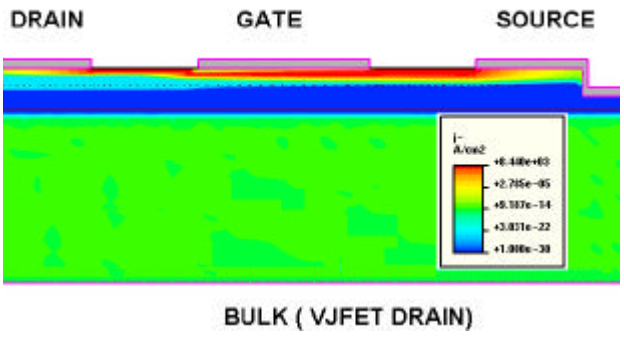

Fig. 3 Mesfet current density at pinch-off (V_{DS} = 50V, V_{GS} = 0V).

While applying a gate bias, a restriction of the lateral channel is induced causing reduction of current as in the classical MESFET. This structure allows the control of channel restriction by both JFET (between drain and p-type buried layer) and MESFET effects.

3. Process Fabrication Description

Both 6H and 4H SiC wafers were used for the device fabrication. N-type epitaxial layers with doping concentration in the range of 5×10^{15} cm^{-3} (15µm) were purchase from Cree INC. A high energy Al implantation (2MeV with a dose of $10^{14}cm^{-2}$ @400ºC) has been performed to form the p-type buried layer. Figure 4 presents simulated profile and SIMS analysis after the thermal annealing step. N^+ areas were then implanted (Dose of $10^{15}cm^{-2}$) for contact zones of the drain and source. Then an n-type box profile was formed at the surface of the wafer by multiple N implantation ($9{,}8 \times 10^{12}$ cm^{-2}) to define the surface channel. RIE etching (1,2 µm), adjusted in relation with simulated profile of Al implantation [3], was performed to contact the p-type buried layer.

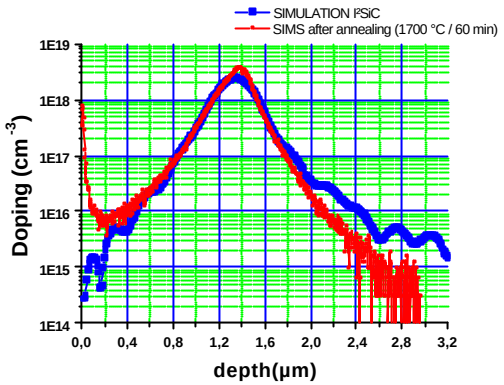

Fig. 4 Simulated Al profile and SIMS analysis results.

Peripheral protection of the MESFET was realized by a field plate whereas the VJFET is protect by both field plate and JTE. The wafers were finally annealed at 1700 °C / 30 min.
Thermal oxidation followed by an oxide deposition was carried out to form the passivation layer. The final step was metal contact formation.

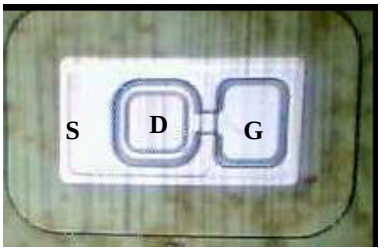

Fig. 5 Top view of fabricated MESFET.

Ni or W layers were deposited and then annealed at the same time for gate and ohmic contacts. Both ohmic and Schottky contacts were simultaneously realized using one mask level for metal patterning. A top picture of the fabricated MESFET is presented in Figure 5.
No additional steps are required to achieve VJFET fabrication due to the similarities with MESFET.

4. Electrical Characterization and Discussion.

The extracted contact resitivity is in the range of $3{,}57 \times 10^{-6}$ Ω.cm² for the Ni 6H-SiC samples (annealing time: 3 min at 900°C) (Figure 6), and $7{,}7 \times 10^{-5}$ Ω.cm² for the 4H-SiC, values in the state of the art [4]. The 4H-SiC MESFET specific on resistance is 38 mΩ.cm² and the transconductance is 0,4 $mS.mm^{-1}$ (higher value : $40mS.mm^{-1}$). This low value is mainly due to high reverse leakage current of the Schottky contact.

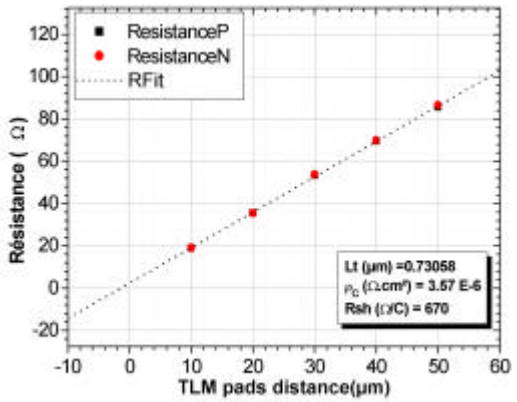

Fig. 6 TLM measurements of 6H-SiC sample.

An on-state current density of 300A/cm² at V_{DS} = 110V has been reached as shown in the Figure 7.
Getting both command and control circuitry on the same chip can cause insulation problems. This is the function of the p-type buried layer. The PN rectifier formed between the p-type buried layer and the epitaxial layer (source/bulk) exhibits a blocking voltage of 950V at 1.10^{-3}A/cm², a very low leakage current density compared to saturation current of MESFET.

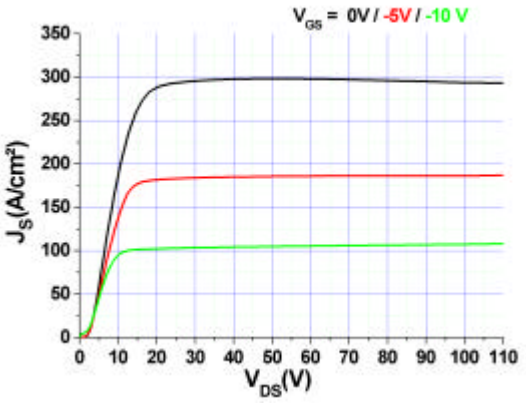

Fig. 7 $I_{DS}(V_{DS})$ versus gate to source applied voltage.

Dynamic resistance as function of gate to source bias has been investigated and remains constant up to V_{GS}= -15V at a value of 50 kΩ/mm and rises up to 170 kΩ/mm with V_{GS}=-20V. This fact is attribute to gate leakage current. In the case of nickel, a metal anneal has been done. The Schottky gate contact was lost and not connected for this measurement (Figure 8). Good ohmic contacts were formed, leading to a rise of current but inducing a degradation of saturation linearity. Nickel reaction with SiC involving channel geometry modification is probably at the origin of this. Using W instead of Ni should avoid this problem.

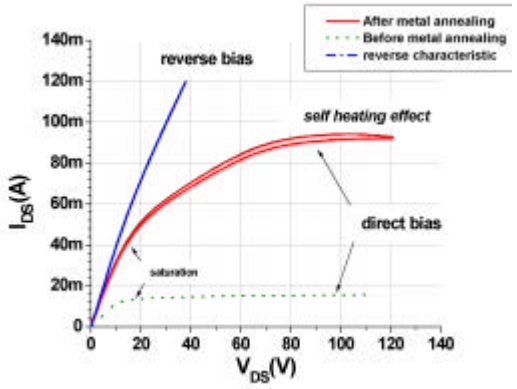

Fig. 8. Metal annealing effect on electrical characteristics.

Conclusion

Full compatibility of fabrication of SiC-VJFETs and lateral SiC-MESFETs has been demonstrated. High power density has been reached (30kW/cm²). State of art ohmic contact values were obtained. Next batch fabrication challenge will consist of both VJFET and MESFET optimization to realize a self controlled current limiter by a cascode-like association of MESFETs and VJFET . Metallization optimization will remain the main point to improve in the next generation of devices. Therefore, two mask levels for metal deposition and patterning should be envisaged with different metal deposition and annealing steps. This compatibility of fabrication should allow us to increase efficiency of power switches and systems as it enables both power devices and control circuits on the same die.

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