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Low damage patterning of $In_{0.53}Ga_{0.47}As$ film for its integration as n-channel in a fin metal oxide semiconductor field effect transistor architecture

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One of the challenges of InGaAs integration as a channel in a fin field effect transistor architecture is the patterning of the III–V fin with nanometer scale definition, vertical sidewalls, and undamaged surfaces. In this work, the authors propose a two-step process to etch anisotropically and with minimal damage thin layers of InGaAs material. The first step of the process aims to modify the InGaAs surface on a well-defined thickness with limited sputtering by implanting light ions generated by a low pressure He/O_2 plasma. The depth of the material modification is well controlled by the ion energy and saturates with process time, giving to this step a self-limited behavior. The second step uses aqueous HF solution to remove the modified oxidized InGaAs layer with infinite selectivity over the nonmodified InGaAs layer. The repetition of cycles of the two-step process was applied to etch the thin film of InGaAs as well as pattern using a SiN hard mask. Blanket experiments show that each cycle of the two-step process allows to remove a fixed and reproducible InGaAs thickness of 5.7 nm, while blanket SiN films are not consumed. After the process, the InGaAs surface roughness is kept intact, but the surface stoichiometry is slightly degraded with Arsenic enrichment because of the wet chemical reactions between the III-As semiconductors and the acids. The results on the pattern show that it is possible to transfer the SiN hard mask into the InGaAs layer using cycles of the two-step process with a reproducible consumed InGaAs thickness at each cycle and low sidewalls surface damage. However, the process leads to tapered InGaAs profile because of the lateral consumption of the SiN hard mask due to preferential sputtering at grazing incidence angle. *Published by the AVS.* https://doi.org/10.1116/1.5051505

I. INTRODUCTION

The transition from planar complementary metal-oxide-semiconductor (CMOS) architecture to 3 dimension (3D) architecture such as fin field effect transistor (FinFET) has been necessary to pursue transistor scaling and overcome high power consumption of logic chip.[1] Innovations in multi-gate devices, such as FinFET nanowire, and vertical FET designs will allow one to continue device scaling at least to the 5 nm technology node.[2] Beyond, new higher mobility channel materials are considered as an alternative to Si in order to meet power and performance requirements to increase performance at reduced supply voltage.[2]

III–V semiconductors, and in particular $In_{0.53}Ga_{0.47}As$, appear highly promising as the n-channel solution for post-Si CMOS due to their high electron injection velocities.[3] FinFET devices with InGaAs channel have been realized and demonstrated with promising performances.[4,5] One of the challenges of InGaAs integration as a channel in a FinFET architecture is the fabrication of the III–V fin.[6,7] It requires the development of the plasma etching process allowing nanometer scale fin definition, with vertical sidewalls and undamaged surfaces (top and sidewalls). Indeed, vertical-sidewall FinFETs have demonstrated better performance at low and moderately doped fins while extremely doped FinFETs are more performant when the fin sidewalls are tapered.[6] Furthermore, plasma induced damage such as sidewall roughness[8] or modification of the surface stoichiometry[6] greatly degrades the MOS interface causing an important decline in the device reliability and electrical performance. These different aspects should be taken into account when carrying out advanced FinFETs.

Today, conventional plasma technologies show intrinsic limitations to etch material with a subnanometer accuracy and without introducing surface damage.[9] On the other hand, atomic layer etching (ALE) emerges as an attractive technique to etch materials with minimal damage while maintaining stoichiometry and providing smooth surfaces.[10]

The basic ALE concept uses sequential reaction steps that are self-limiting.[11] Typically, it starts with a modification step to form a reactive layer, followed by a removal step to takeoff only this modified layer. This concept has already been proposed to etch III–V semiconductors, and a variety of self-limiting mechanisms have been investigated.[12–17] The majority are on directional ALE using alternating chlorination modification step followed by modified layer removal with particle bombardment.[12–14] Other studies on III–V materials involved isotropic ALE, originally referred to as "digital etching."[15–17] The reactive layer is formed by oxidizing the substrate by a diffusion limited process (rinse in H_2O_2). This is followed by the removal of the oxidized layer by submerging the wafer into a wet acid bath (e.g., HCl solution).

Posseme *et al.*[18] proposed a new approach based on a two-step process to etch anisotropically thin layers without introducing damage and applied it to nitride spacer etching.

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In a first step, the thin film material is modified on a defined thickness by light ions implantation (He^+ or H^+) produced in a low pressure plasma reactor. Then, the modified material is removed using appropriate wet etching with a high selectivity with respect to the nonmodified material. This process is not the ALE process since it does not aim to remove one atomic layer of material, but it could be considered as quasi-ALE process in the sense that the process involves two self-limiting steps.

In this article, we evaluate the concept proposed by Posseme *et al.* to pattern InGaAs fin with vertical sidewalls and minimal damage. The two-step process to be developed is illustrated in Fig. 1.

The first step uses light ions implantation performed in an inductively coupled plasma (ICP) reactor to modify InGaAs on a well-defined thickness. During this step, the modified layer thickness must be well controlled and the materials sputtering limited. The second step uses aqueous wet etching to remove the modified InGaAs layer with infinite selectivity over the nonmodified InGaAs layer as well as over the hard mask (both modified and nonmodified). Each cycle removes a fixed and reproducible thickness of InGaAs, and repetition of the cycle is used to obtain a desired etch depth.

In the first experimental part of this article (Sec. III A), preliminary studies are performed on blanket films and are dedicated to the determination of the best suited plasma chemistry for the implantation step, as well as the more suitable wet solution to remove the modified layer. In a second part (Sec. III B), the selected conditions for the two-step process are optimized to ensure a well controlled modified InGaAs thickness with minimal InGaAs and hard mask sputtering during the implantation step, and selective removal of the modified InGaAs over bulk InGaAs and hard mask during the wet step. Finally, in a third and fourth part, the cycle composed of the optimized two-step process is repeated to etch the InGaAs film (Sec. III C), as well as to pattern InGaAs fin with a SiN hard mask (Sec. III D). Particular attention is paid on the damage (roughness and loss of stoichiometry) generated on the InGaAs surface (flat surface and pattern sidewalls) after the sequence of cycles of the two-step process.

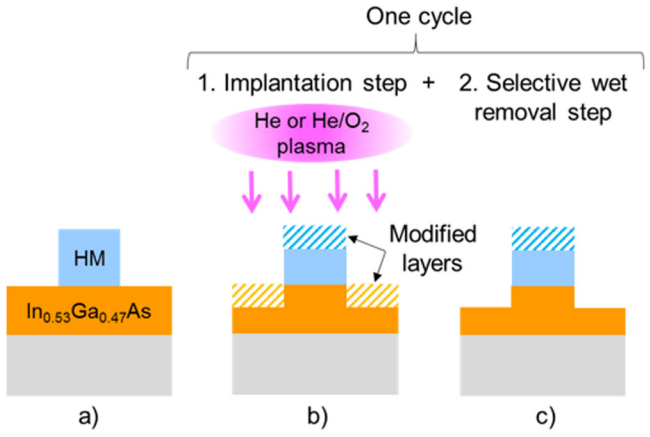

FIG. 1. Description of InGaAs fin patterning with hard mask (HM) using a two-step process: (a) stack before process; (b) first step: material modification by ion implantation achieved with He or He/O_2 plasmas; (c) second step: selective wet removal of modified InGaAs layer over all other materials in presence. The cycle is repeated until etching the desired thickness.

II. EXPERIMENTAL SETUP

A. Substrates

The materials under investigation are 30 nm thick undoped $In_{0.53}Ga_{0.47}As$ films grown on a 4 in. InP wafer by metal organic chemical vapor deposition and 40 nm thick SiN films deposited on Si wafers by plasma enhanced chemical vapor deposition that will be used as the hard mask material.

For the pattern experiments, a 80 nm thick SiN film is deposited on the InGaAs film. A trilayer masking strategy has been adopted to open the 80 nm thick SiN hard mask. It consists in spinning a 90 nm thick spin on carbon (SOC) film, then a 30 nm Si antirelective coating (Si-ARC), and then the 90 nm thick ebeam resist film on the SiN deposit. Ebeam lithography is used to define the 50 nm-wide isolated lines. The Si-ARC layer is first open using a $Ar/CHF_3/CF_4$ plasma, then the Si-ARC is used to open the SOC layer in HBr/O_2 plasma. Finally, the SiN hard mask is open with a CF_4 plasma and the SOC is stripped with O_2 plasma. All plasma processes are achieved in the ICP reactor described in Sec. II B; the plasma conditions could be found in Ref. 19.

For the implantation experiment, 1 cm^2 of blanket or patterned sample is taken from the substrate and glued with a thermal paste on a 300 mm diameter Si carrier wafer on which a 20 nm thick Al_2O_3 film has been deposited by atomic layer deposition.

B. Plasma reactor

The plasma implantation is performed in a 300-mm ICP etch tool from applied materials (Centura® AdvantEdge™ MESA™). The plasma is inductively excited via two radio-frequency (rf) coils to improve the ion flux uniformity with a power supply operating up to 3 kW at 13.56 MHz. The wafer can be rf-biased using a second power supply (capacitively coupled to the electrostatic chuck) operating up to 1.5 kW. The temperature of the wafer is kept at 60 °C by means of a helium backside temperature regulation at 12 Torr between the electrostatic chuck and the 300 mm wafer. The reactor chamber walls are coated with Y_2O_3 material and are kept at 65 °C. He or He/O_2 plasma have been used to perform the implantation step. In all the experiments, the reactor chamber pressure and the source power are fixed at 10 mT and 800 W, respectively.

C. Characterization techniques

1. Ellipsometry

The thicknesses of SiN and InGaAs films before and after implantation and wet removal are obtained by ellipsometry. These measurements were carried out with a phase modulated ellipsometer using an M-2000 model from J. A. Woollam. The light source consists of two lamps, one in

deuterium and the other in Tungsten Halogen Quartz allowing acquisition over a range of 700 wavelengths between 193 and 1690 nm. In this study, acquisitions were carried out over the entire wavelength range (193–1690 nm) with an increment of about 2.1 nm and an integration time of 50 ms. The spectra obtained are processed with WVASE32 software by J. A. Woollam that proposes dispersion laws for the two materials investigated here.

2. Electronic microscopies

Transmission electron microscopy (TEM) was performed to observe the depth of the modification induced in the InGaAs film after implantation and the thickness of removed InGaAs by the wet etching. The observations are achieved in a TEM TECNAI with an incident beam energy of 200 keV. Prior to TEM observations; a dual focused ion beam-scanning electron microscope (FIB-SEM, FEI Helios 450S) is used to prepare the 100 nm thick thin lamella for the TEM characterizations.

The InGaAs profiles after patterning using the two-step process are characterized using scanning electron microscopy (SEM) cross-sectional observations performed in a Hitachi 5000 equipment.

3. Atomic force microscopy

Atomic force microscopy (AFM) was used to estimate the surface roughness of the InGaAs films and the pattern sidewalls roughness [line edge roughness (LER)] before and after the two-step process. The AFM experiments were carried out in tapping mode with conical tips (AC160TS from Olympus) having a radius of curvature of 10 nm in an EnviroScope from Veeco instruments. For the surface roughness, an area of $5 \times 5\,\mu m^2$ is scanned with a resolution of 1024×1024 data points. For the sidewalls roughness, a home-made setup was used where the sample is tilted so that the AFM tip can probe directly the pattern sidewalls. All the details about this technique can be found in Ref. 20.

4. X-ray photoelectron spectrometry

The InGaAs surfaces exposed to the implantation and wet steps are chemically characterized by angle resolved x-ray photoelectron spectrometry (ARXPS). The XPS chamber is directly connected via a vacuum transfer chamber to the MESA plasma reactor allowing quasi *in situ* characterization of the surface after implantation. The ARXPS system is equipped with a high resolution monochromatic Al Kα x-ray source (1486.6 eV photons) and with the Thermo Electron Theta 300 x-ray spectrometer that allows to collect photoelectrons with a wide acceptance angle of 60°, more precisely photoelectrons emitted from the surface with angles ranging from 20° to 80°.[21] This allows to detect electrons coming from different depths of the surface, and thus to get some information on the element distribution within the probed surface (about the first 10 nm). The XPS spectra are recorded in the angular mode using eight angles regularly spaced between 20° and 80° referred to the normal of the wafer with an acceptance angle of ±3.25° at a constant dwelling time of 500 ms and pass energy of 100 eV. In this study, we have used the XPS spectra collected at an angle of 23.25° ± 3.25° and 76.75° ± 3.25° corresponding to photoelectrons escaping from the deep surface (about 10 nm, referred here as "bulk" signal) and the near surface (about 1–2 nm, referred here as "surface" signal). The concentrations of As, In, Ga, Si, C, and O atoms are extracted from the As3d, $In3d_{5/2}$, Ga3p, Si2p, C1s, and O1s core level energy regions, respectively. Using a numerical fitting procedure based on a Levenberg–Marquardt algorithm, spectral deconvolution is performed to extract the peak contributions in the acquired energy regions. Individual line shapes are simulated with the combination of Lorentzian and Gaussian functions. The background subtraction has been performed by using a Shirley function calculated from a numerical iterative method. After correction of the lens transmission factor, each element concentration is obtained by dividing calculated peak areas by the corresponding Scofield cross section ($As3d_{5/2}$: 1.08, In $3d_{5/2}$: 13.32, $Ga3p_{3/2}$: 2.11, Si2p: 0.817, C1s: 1.0, O1s: 2.93). The sum of the concentrations of different elements present on the analyzed surfaces is equal to 100%. The element energies are shifted using the C1s peak at 285 eV as a reference. The $In3d_{5/2}$ spectrum of the as-grown InGaAs layer can be fitted with two peaks at 444.6 and 445.4 eV corresponding to In—As and In—O (native oxide) bonds, respectively. The As3d and Ga3p spectra are fitted with spin-orbits splitting of 0.69 and 3.5 eV, respectively. The As3d spectrum of the as-grown InGaAs layer is composed of three doublets, whose $As3d_{5/2}$ peaks are located at 41.1, 44.3, and 45.4 eV corresponding to As—(In or Ga) bonds, As—O bonds in As_2O_3 environment, and As—O bond in As_2O_5 environment, respectively. The Ga3p spectrum of the as-deposited InGaAs is composed of two doublets, whose $Ga3p_{3/2}$ peaks are located at 104.8 eV and 106.1 eV corresponding to Ga—As bonds and Ga—O bonds in Ga_2O_3 environment, respectively. The peak positions are in agreement with what can be found in the literature.[22,23]

D. Simulation

Stopping and range of ions in matter (SRIM) software by J.F. Ziegler, available on the web,[24] was used to simulate the ion penetration depth into the InGaAs film during the implantation as well as the sputtering yields of the As, Ga, and In. InGaAs was defined with a chemical composition of 26.5% indium, 23.5% gallium, and 50% arsenic and a density of 5.48 g/cm^3. The simulations were runned using the "surface sputtering/monolayer collision steps" type of SRIM calculations.

III. EXPERIMENTAL RESULTS

A. Preliminary investigations

Figure 2 shows a cross-section TEM image of the InGaAs film exposed to He implantation with the following plasma conditions: He 100 sccm, source power 800 W, bias power 125 W, pressure 10 mTorr, and time 60 s. In these conditions, the ion energy is about 140 eV. A 6 nm thick damaged layer

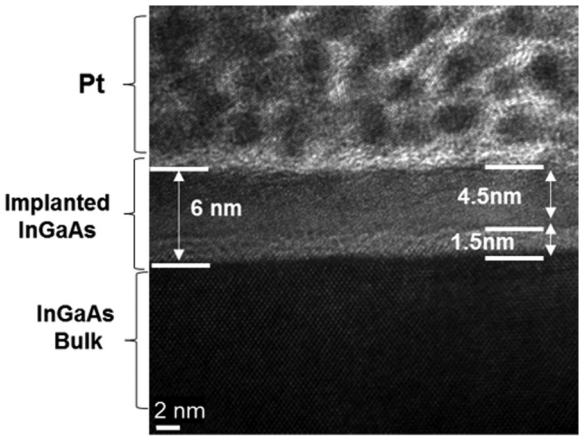

FIG. 2. Cross-section TEM image of the InGaAs film after He implantation (He 100 sccm, source power 800 W, bias power 125 W, pressure 10 mTorr, time 60 s).

is clearly visible above the undamaged crystalline InGaAs substrate, conveying that He implantation has generated an amorphous InGaAs layer composed of lighter elements, as indicated by the contrast difference visible in the TEM image. It is also noticed that the amorphous layer seems to be composed of two distinct regions, one 4.5 nm deep near the surface and the other 1.5 nm above the unmodified InGaAs. The interface between the modified and unmodified layers appears suitably flat and the underlying InGaAs has also not been physically damaged and has retained its perfect crystallinity. Under the implantation conditions used here, the sputtering of the InGaAs layer is of 0.5 nm and no SiN consumption is measured.

The atomic chemical composition of the InGaAs surface before and after He implantation is obtained by ARXPS analyses (cf. Fig. 3). Before implantation, InGaAs is slightly oxidized due to the presence of the native oxide and the surface is contaminated with carbon. After implantation, the InGaAs surface is strongly oxidized on almost all the probed depth (only few traces of nonoxidized III–V elements are detected at 23°) [cf. Fig. 3(b)]. Indium is found on its oxidized form on the whole probed surface. At grazing angle, 65% of Ga and 80% of As are oxidized. The surface is enriched in indium and depleted with Ga and As. This can be explained by the preferential sputtering of Ga and As compared to In by He ions. SRIM simulations were runned and showed that the sputtering yields of In, Ga, and As by He ions with a 140 eV energy are of 0.0019, 0.0025, and 0.008 atoms/ions, respectively. The surface also contains non-negligible amounts of contaminants such as carbon, fluorine, and silicone. As XPS analyses are achieved in a quasi *in situ* way, all the contaminants including oxygen present on the InGaAs surface come from reactor chamber wall contamination. Indeed, the MESA reactor is dedicated to silicon based materials etching and fluorine-based plasma cleaning processes are systematically used after silicon etching to clean Si residues deposited on the reactor wall. The oxygen can come from the Y_2O_3 reactor wall, as well as the Al_2O_3 carrier wafer, although Al was not detected in the layer.

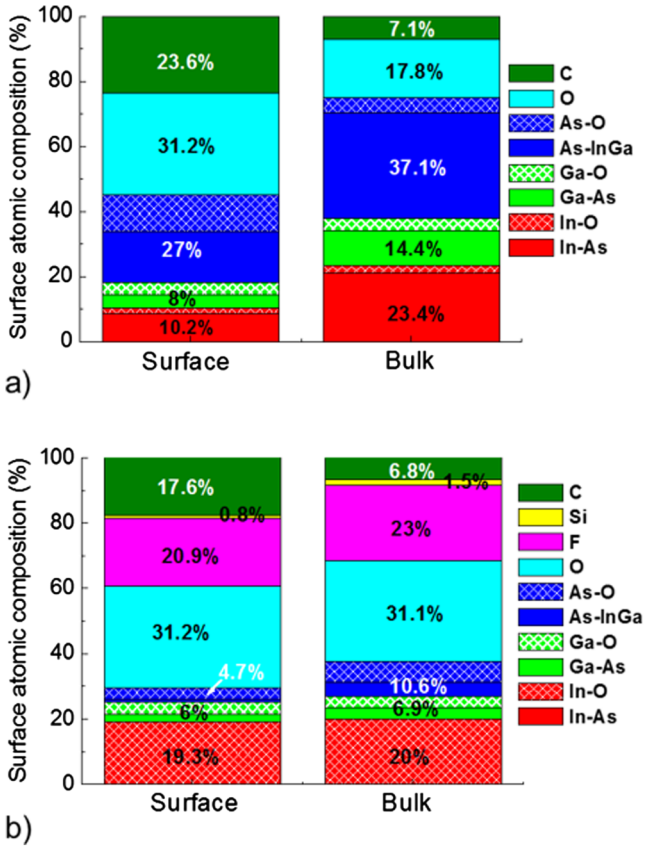

FIG. 3. Atomic composition of the InGaAs surface at grazing angle 76.75° (surface) and near normal angle 23.25° (bulk) (a) before and (b) after He implantation. The percentage indicated on the graph represents the relative chemical quantification of one element whatever its chemical environment.

Moreover, the ARXPS analyses reveal that these contaminants, except carbon, are not just located at the very near surface but are implanted in the bulk, since the relative contributions of these elements at near normal angle are slightly higher than at grazing angle. This is somewhat not surprising. Indeed, helium has a very high ionization potential of 24.59 eV compared to the ones of Si (8.15 eV), C (11.26 eV), O (13.62 eV), and F (17.42 eV).[25] This means that if these contaminants are present in the gas phase, they will be more likely to be ionized compared to helium and will also be implanted into the InGaAs surface. As described by the theory of the stopping and range of ions in matter, the depth at which each element will be implanted will mainly depend on their atomic mass; the lighter the atom the deeper it will penetrate.[26] SRIM simulations were runned to get the penetration depth profile of He, Si, and O ions with an energy of 140 eV into the InGaAs film (cf. Fig. 4). The mean depth of He ion distribution, also called projected ion range, is of 3.9 nm, while it is only of 1.5 and 1.2 nm for O and Si, respectively. The standard deviation of the ion distribution, also called straggling, is of 2.2, 0.9, and 0.7 nm for He, O, and Si, respectively. The difference in the implantation profile according to the ion mass well explains why in TEM image of Fig. 2, there are two distinct regions in the modified InGaAs layer. The upper 4.5 nm thick region corresponds to the range at which O, Si, and F can be implanted, and

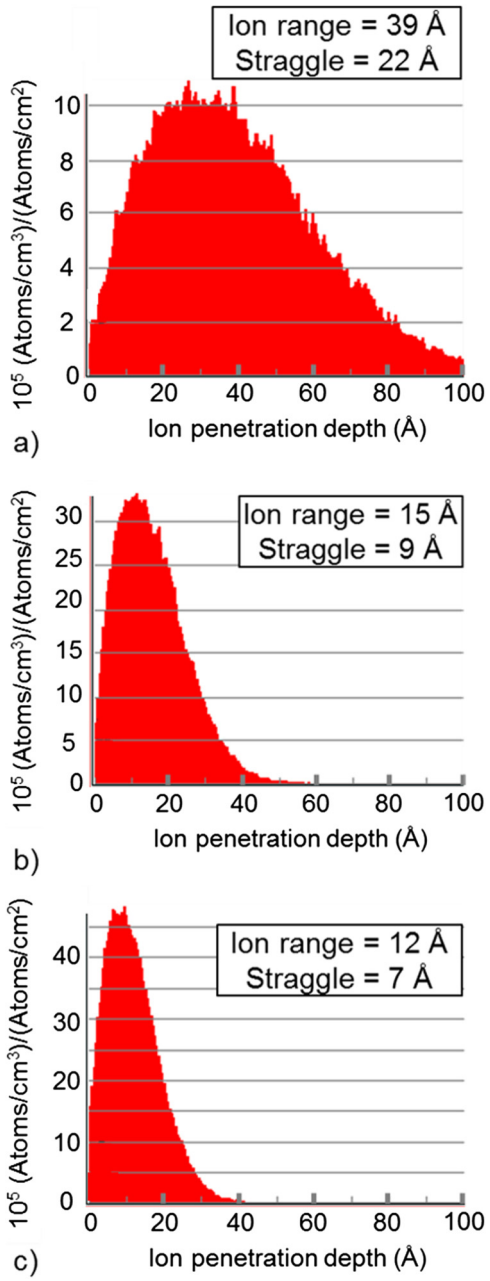

FIG. 4. Penetration depth profile of ions with 140 eV energy into $In_{0.53}Ga_{0.47}As$ simulated by SRIM (a) He^+, (b) O^+, (c) Si^+.

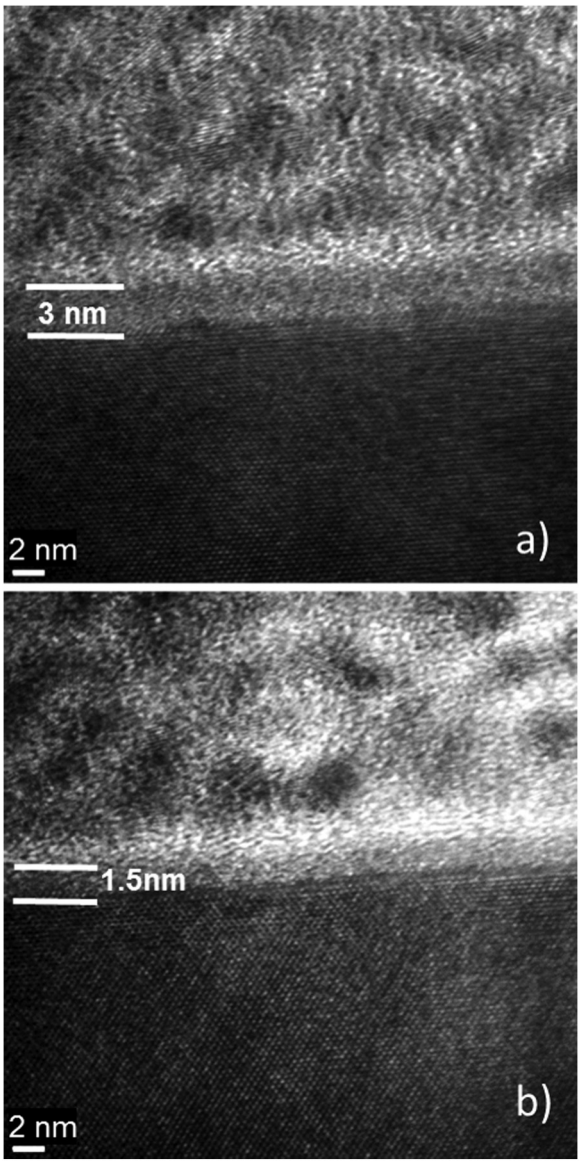

FIG. 5. Cross-section TEM analyses of the InGaAs layer after He implantation and subsequent wet bath using (a) 4% HCl during 3 min and (b) 1% HF during 1 min.

InGaAs is strongly oxidized in this region. On the other hand, only helium ions could reach the 1.5 nm thick underneath region (that appears brighter on the TEM image). The 6 nm thick total modified thickness observed on the TEM image is also consistent with the He ion projected range of 3.9 ± 2.2 nm.

Acidified solutions are effective for removing oxides formed on the InGaAs surface without consuming the bulk material.[27,28] In this study, HCl and HF wet solutions were tested to remove the InGaAs modified layer. Whatever the wet duration or the dilution tested, similar results were obtained and are illustrated in the TEM images of Fig. 5. After HCl wet, only 3 nm of the InGaAs modified layer is removed against 4.5 nm with HF wet (cf. Fig. 5).

ARXPS analyses carried out after He implantation followed by HCl and HF wet are shown in Fig. 6.

By comparing the XPS results after wet (cf. Fig. 6) to those obtained after He implantation [i.e., before wet, cf. Fig. 3(b)], it is observed that both HCl and HF can remove, at least partially, the III–V oxidized layer formed during the implantation, since III–V elements under their metallic form are now detected after wet at grazing angle. As the XPS analyses after wet are achieved after air exposure, it is hard to conclude if the oxidized III–V elements present at the InGaAs surface after wet are coming from the reoxidation of the InGaAs surface during the air exposure or if they come from the InGaAs layer modified by the implantation that has not been removed by the wet step.

After HCl, a significant amount of Si (~8%) is retrieved at the surface against only 3% in the HF case. The Si quantification is extracted from the Si2p core level XPS spectrum

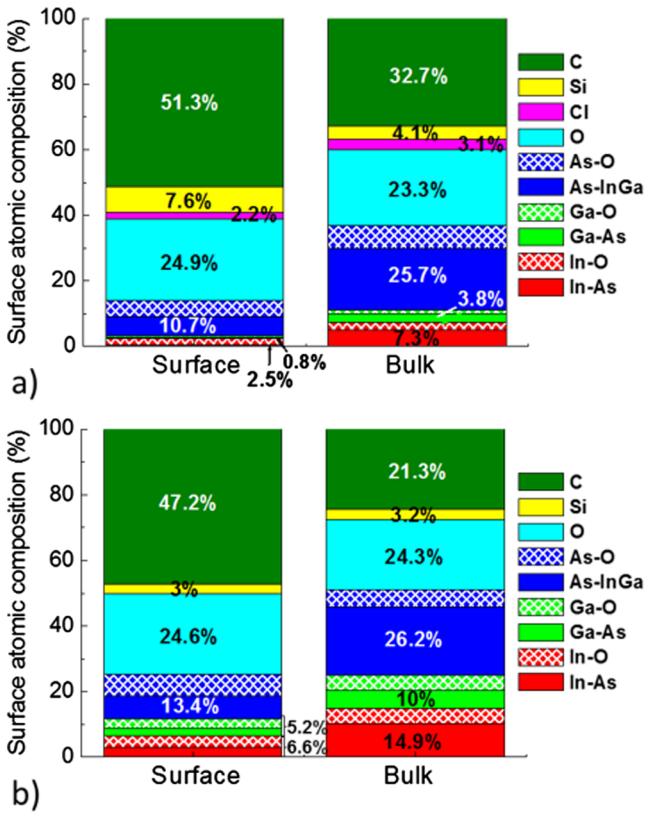

FIG. 6. Atomic composition of the InGaAs layer at grazing angle 76.75° (surface) and near normal angle 23.25° (bulk) after He implantation followed by (a) 4% HCl dip during 3 min and (b) 1% HF dip during 1 min. The percentage indicated on the graph represents the relative chemical quantification of one element whatever its chemical environment.

that presents one peak at 102.3 eV, revealing that Si is oxidized (SiOx). SiOx compounds can be removed with HF but not with HCl.

Thus, in the HCl wet case, the silicon that was implanted in the InGaAs layer during the modification step blocks the action of the HCl chemistry. It creates a passivation layer that prevents from removing the whole oxidized InGaAs layer.

In the HF case, the presence of implanted SiOx is not an issue and the upper oxidized 4.5 nm thick modified layer is completely removed. On the other side, the underneath 1.5 nm thick less oxidized layer is left intact. XPS analyses also reveal the presence of Si at the InGaAs surface after HF wet. It corresponds to the few Si atoms implanted in the He rich InGaAs region. We do not think that in this case, it is responsible for the etching stop but rather the low InGaAs oxidation state.

From these preliminary set of experiments, we can draw the following conclusions. The wet removal of InGaAs after He implantation is efficient only if InGaAs is oxidized during the treatment. An amorphization of the InGaAs surface without oxidation is not enough to allow efficient wet removal (the 1.5 nm thick layer above the unmodified InGaAs is not removed by HF wet). That is why the 6 nm thick modified InGaAs layer after implantation cannot be completely removed by HF wet. Si contamination from the reactor chamber leads to Si implantation into InGaAs during the He implantation step. Although several reactor wall cleaning and conditioning strategies were tested, we could not get rid of the Si contamination. The detrimental consequence is that its presence blocks HCl wet removal action. HF wet is thus preferred. However, the HF wet conditions must be carefully chosen in order not to consume the SiN hard mask. Based on these findings, we choose to develop He/O_2 plasma chemistry to perform the implantation step in order to have a better control on the implanted oxygen, and we investigate the best HF wet conditions compatible with our integration.

B. Optimization of the two-step process

In this subsection, we first investigate the optimal He/O_2 plasma conditions to modify InGaAs with minimal sputtering. Then, we optimize the HF bath conditions to allow infinite selective removal over the SiN layer.

A previous study[29] dealing with He implantation into Si and SiN layers showed that the ion dose (ion flux * process time) and energy were the main parameters controlling both the thickness and modification rate of the modified layer generated by He implantation. Figure 7 shows the modified thickness as a function of the processing time for three different ion energies (75, 140, and 205 eV) obtained by varying the bias power at 60, 125, and 200 W, respectively, the other plasma parameters being fixed: 100 sccm He/5 sccm O_2, source 800 W, and pressure 10 mT.

It appears that the thickness of the modified layer is mainly driven by the ion energy. The higher the energy is, the thicker the modified layer is. For each ion energy, the evolution of the modified thickness with the implantation time takes place in two stages. It first increases rapidly and then reaches a saturation value indicated by the dotted lines in Fig. 7(a). The steady state is defined as the moment when the modified thickness reaches this saturation value. This behavior is due to the self-limiting nature of the implantation which lies in the fact that from the moment when the stationary state is reached, the absorption of atoms by the material is constant. Indeed, molecular dynamics results dealing with He implantation into silicon and SiN showed that in the stationary state, the number of helium atoms ejected by the bombardment became equal to the number of helium atoms penetrating into the material.[29] A last point to raise on Fig. 7(a) is that the stationary state is reached all the more quickly that the energy of bombardment is high and this, in an almost linear way: when the energy of the ions is doubled, the stationary state is reached with a time two times shorter. This trend is also well explained in Ref. 29. When helium ions are implanted in a material, the probability that they are reflected on its surface is inversely proportional to their energy. Thus, the lower the bombardment energy, the lower the proportion of ions transferred into the material, which obviously decreases the efficiency and rate of surface modification, thus delaying the onset of the stationary state. The modified layer thickness at the stationary state is 4.5, 5.9, and 6.7 nm at 75, 140, and 205 eV, respectively. In

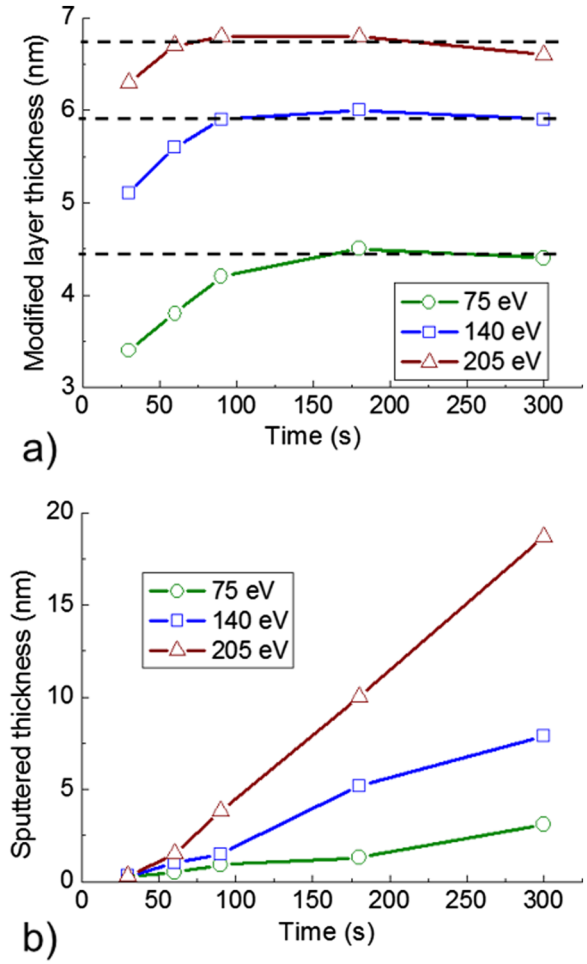

FIG. 7. (a) Thickness of the modified InGaAs layer and (b) sputtered InGaAs thickness generated during He/O_2 implantation as a function of processing time and ion energy. Plasma conditions: 100 sccm He/5 sccm O_2, source 800 W/pressure 10 mT. Bias power is varied at 60, 125, and 200 W corresponding to 75, 140, and 205 eV ion energy.

Fig. 7(b) is also plotted the InGaAs sputtered thickness as a function of implantation time and ion energy. It logically shows that this thickness increases with time and ion energy. By limiting the duration of implantation to the time required to reach the stationary state, 180 s at 75 eV, 90 s at 140 eV, and 60 s at 205 eV, the sputtered thickness of InGaAs is minimized and is, respectively, of 1.3, 1.1, and 1.5 nm. The implantation condition using 140 eV ion energy (125 W bias) during 90 s seems a good compromise between surface modification (5.9 nm) with minimal sputtering (1.1 nm). In these implantation conditions, no SiN is consumed by sputtering.

The TEM and XPS analyses performed on the InGaAs surface exposed to 90 s He/O_2 implantation using 125 W bias (not shown here) are very similar to the ones obtained on InGaAs after 60 s He implantation using 125 W bias shown in Figs. 2 and 3. A 6 nm thick modified layer also composed of an upper 4.5 nm thick strongly oxidized layer on a amorphized and less oxidized 1.5 nm thick layer is observed. As already explained for the He implantation where contaminants such as Si, O, and F are also implanted (cf. Sec. III A), the upper oxidized modified layer thickness corresponds to the range at which O can be implanted at a given ion energy, while the total modified thickness corresponds to the range at which He can be implanted at the same ion energy (cf. Fig. 4). Since He is lighter, it is implanted deeper. By increasing the ion energy (the bias power), the thicknesses of both the upper oxidized layer and the total modified layer will increase, provided that sputtering is limited.

The XPS analyses also detect Si contamination with He/O_2 implantation but in a less extend than with He implantation (0.5% instead of 1.5%). The surface is enriched in indium and depleted with Ga and As. Indium is found in its oxidized form on all the probe surface. At grazing angle, Ga and As are slightly more oxidized (77% of Ga and 86% of As) than with He implantation (65% of Ga and 80% of As). AFM measurements performed before and after He/O_2 implantation with the selected conditions (125 W bias-60 s) [cf. Figs. 8(a) and 8(b)] show that the surface roughness is not much impacted by the implantation step, the peak-to-peak roughness R_{max} being even smaller conveying a preferential sputtering of the hills of the surface. Generally, it was noticed that the He/O_2 implantation step, whatever the ion energy used, does not generate surface roughness as long as the InGaAs sputtering is limited.

HF wet has been used to remove the InGaAs modified layer, since we have seen in Sec. III A that HCl wet was not efficient enough to remove the Si-containing modified InGaAs layer. The drawback of HF wet compared to HCl is that it is likely to consume the modified (the top surface) and

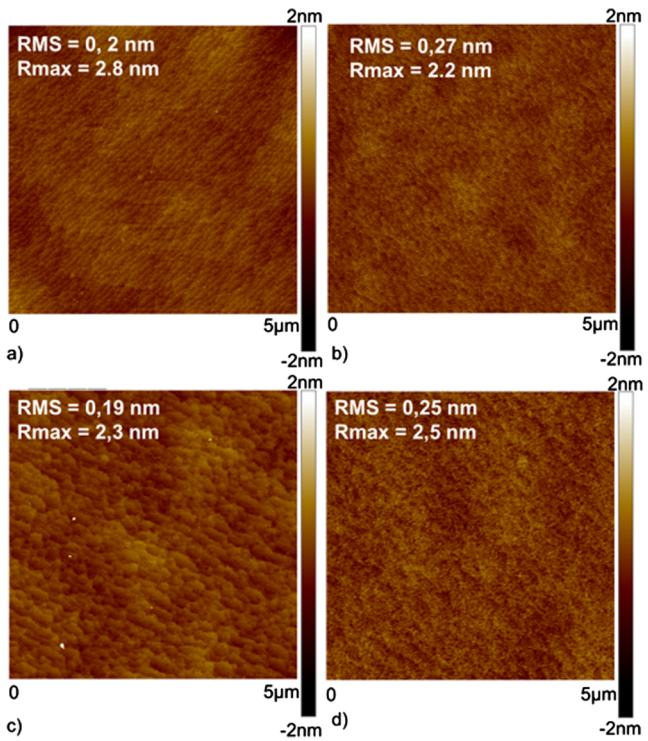

FIG. 8. 5 * 5 μm AFM images of (a) as-grown InGaAs, and InGaAs after (b) He/O_2 implantation (100 sccm He/5 sccm O_2/source 800 W/pressure 10 mT/bias power 125 W/90 s), (c) one cycle of the two-step process (implantation + HF wet), (d) three cycles of the two-step process (implantation + F wet). RMS and R_{max} stand for root mean square roughness and peak-to-peak roughness, respectively.

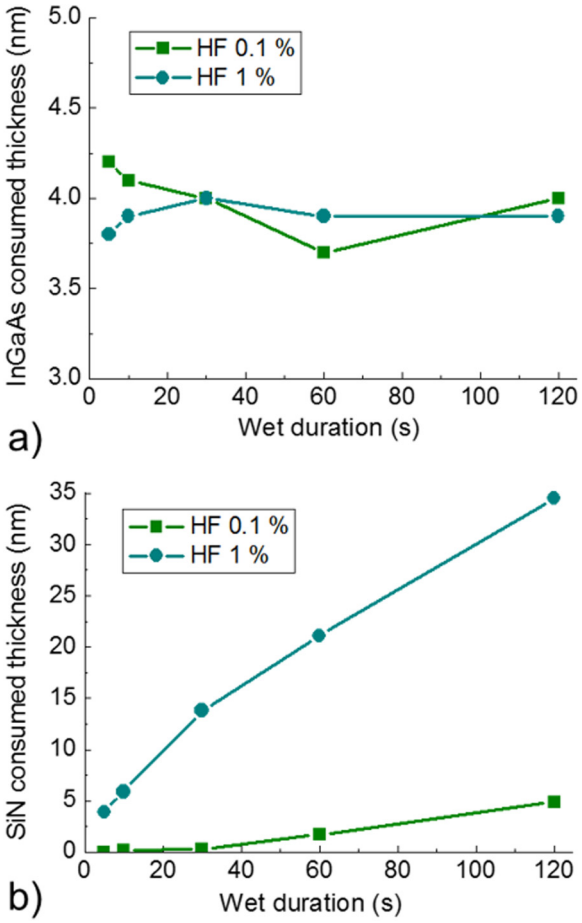

FIG. 9. Consumed thickness during a HF wet according to the HF dilution and wet duration of (a) InGaAs and (b) SiN films priory exposed to He/O_2 implantation (100 sccm He/5 sccm O_2/source 800 W/pressure 10 mT/bias power 125 W/90 s).

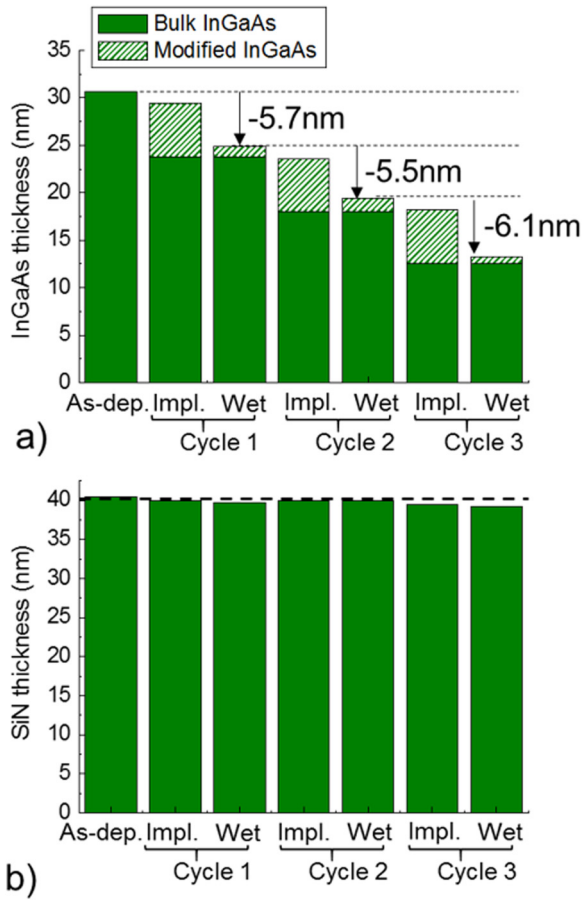

FIG. 10. Evolution of the InGaAs (a) and SiN (b) film thickness after each step [implantation (Impl.) and HF wet (Wet)] composing an etch cycle. The films have been exposed to three subsequent cycles. The implantation conditions are 100 sccm He/5 sccm O_2/source 800 W/pressure 10 mT/bias power 125 W/90 s, and the wet uses 0.1% HF during 5 s.

unmodified (the sidewalls) surface of the SiN hard mask. SiN and InGaAs films are exposed to the optimal implantation conditions selected previously (100 sccm He/5 sccm O_2/source 800 W/pressure 10 mT/bias power 125 W/90 s) and then dipped into either 0.1% or 1% HF bath over times ranging from 5 s to 2 min. Ellipsometry measurements are performed before and after the wet step. The InGaAs and SiN consumed thicknesses during the HF wet as a function of time and HF dilution are shown in Fig. 9.

Whatever the HF dilution and bath duration, about 4 nm of InGaAs is removed during the wet, thickness that corresponds to the oxidized part of InGaAs during the implantation. As for the He implantation case, the 6 nm thick modified InGaAs layer is not completely removed and only the upper more oxidized layer is consumed by the HF wet. On the other hand, the consumption of the implanted SiN [Fig. 9(b)] evolves linearly with time and is highly dependent on the HF concentration. Low HF dilution and low wet duration are favorable to good etch selectivity of InGaAs over implanted SiN (as well as nonimplanted SiN, not shown here). An infinite selectivity can even be obtained with a solution of 0.1% HF limited to 5 s; the SiN is not consumed under these conditions while 4 nm of the modified InGaAs layer is removed.

C. InGaAs film etching with cycles of the two-step process

InGaAs and SiN blanket samples are patched on a Al_2O_3 carrier wafer and exposed to three cycles of the two-step process. Each cycle comprises an He/O_2 implantation step at

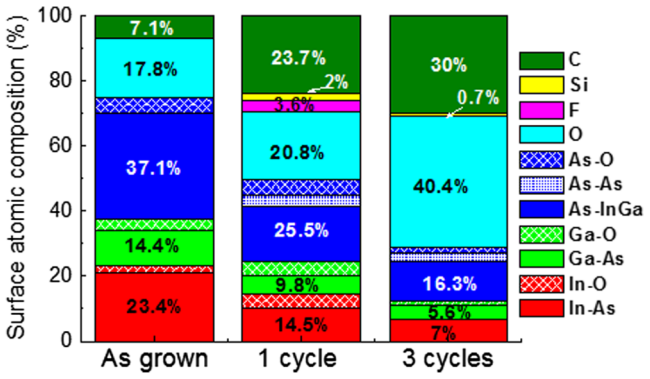

FIG. 11. Surface atomic composition of as-grown InGaAs, and InGaAs exposed to one and three cycles of the two-step process obtained by ARXPS at a collection angle of 23.6° (bulk). The percentage indicated on the graph represents the relative chemical quantification of one element whatever its chemical environment.

TABLE I. InGaAs stoichiometry before and after one or three cycles of the two-step process determined by XPS analyses using a collection angle of 23.6° (bulk).

	(In + Ga)/Ga	(In + Ga)/As
As received	0.62	1.02
One cycle	0.6	0.95
Three cycles	0.54	0.73

140 eV ion energy during 90 s followed by a 0.1% HF wet during 5 s. Figure 10 shows the evolution of InGaAs and SiN thicknesses at each step (implantation and wet) of the three cycles. The steps are reproducible from one cycle to another. During each implantation step, 1.2 nm thick InGaAs layer is sputtered and the InGaAs surface is modified on the 5.6 first nm. During the HF wet step, about 75% of the modified layer is removed, namely, 4.5 nm. At each cycle, 5.7 nm of InGaAs (1.2 nm sputtered + 4.5 nm removed by wet) is thus reproducibly consumed. On the other hand, only 1.1 nm of SiN is consumed after the three cycles.

AFM analyses performed on InGaAs films after one and three cycles of the two-step processes are shown in Figs. 8(c) and 8(d). After one or three cycles, the InGaAs surface roughness is very similar to the one after the first He/O_2 implantation [cf. Figs. 8(b) and 8(c)]. The sequence of cycles of the two-step process does not degrade the InGaAs surface roughness. Figure 11 compares the surface composition of as-grown InGaAs and InGaAs exposed to one and three cycles of the two-step process obtained by XPS at a collection angle of 23.6°. Due to air exposure, the surface is contaminated by carbon and oxygen. The high oxygen content obtained after three cycles is mainly due to the presence of C—O and C═O bonds on the surface. After one and three cycles, there are still some traces of silicon detected on the InGaAs surface coming from the implantation step. However, its concentration seems to decrease with the sequence of cycles. The InGaAs surface is slightly oxidized certainly due to air exposure. After three cycles, the surface is much less oxidized than after one cycle. It is hard to conclude if this is due to the queue time between the wet step and the XPS analysis that might have been different or if the sequence of cycle helps in passivating the surface and prevents from its oxidation. From these analyses, InGaAs surface stoichiometry can be obtained by calculating two ratios: the In/(Ga + In) ratio that compares the III elements proportion in the crystal (theoretically 0.53) and the (In + Ga)/As ratio that compares the proportion of III elements to the one of V element (theoretically 1). Table I shows these ratios for the pristine material and after one and three cycles of the two-step process. It shows that the sequence of cycles causes a slight indium depletion of the surface [decrease of 13% of the In/(Ga + In) ratio] and a strong enrichment in arsenic [increase of 28% of the (In + Ga)/As ratio]. The deconvolution of the XPS As3d core level spectrum after the two-step process shows the presence of a new As environment with a $As3d_{5/2}$ peak at 41.8 eV [+0.7 eV above the As—(In or Ga) bond] identified as As—As bonds.[23,30] As indium is the element that is more oxidized after the implantation step [cf. Fig. 3(b)], and that the wet step aims to remove III–V oxides selectively over III–V elements, it is logical to retrieve a surface slightly depleted in indium. The generation of

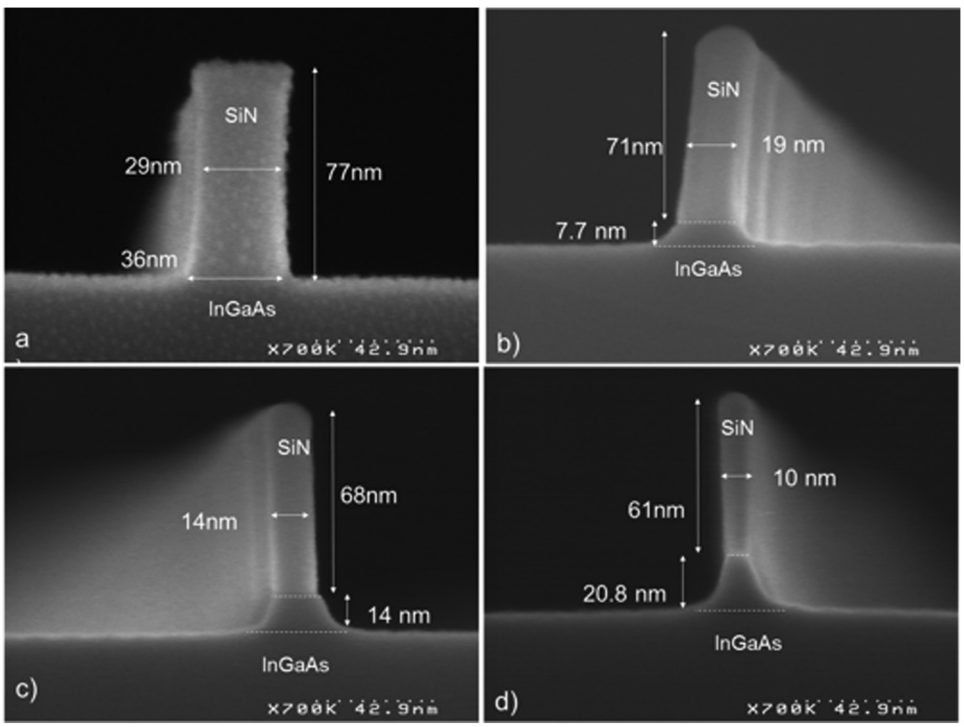

FIG. 12. SEM cross-section images of InGaAs patterned with the digital etching process using He/O_2 implantation (100 sccm He/5 sccm O_2/source 800 W/pressure 10 mT/bias power 125 W/90 s) followed by 0.1% HF wet during 5 s (a) before etching, (b) after one cycle, (c) two cycles, and (d) three cycles.

elemental As after wet etching using acidified solution is consistent with previous reports and the wet mechanisms involved between III-As and acidified solutions.[27,31]

D. InGaAs pattern etching with cycles of the two-step process

The two-step process was then applied to the patterning of the InGaAs film using an SiN hard mask. Figure 12 shows the pattern profile evolution before etching and after one, two, and three cycles of the process. From Fig. 12, it is observed that the vertical InGaAs thickness consumed at each cycle is reproducible and of about 7 nm, slightly higher from what was expected from the blanket experiments of Sec. III C where 5.7 nm of InGaAs was removed at each cycle. On the other side, the behavior of the SiN hard mask is completely different from what was measured on blanket films. The SiN hard mask is consumed at each cycle vertically and laterally in a nonreproducible way. The lateral consumption of the SiN hard mask has some drastic consequences on the InGaAs profile and it is likely responsible for the slope profile of the InGaAs patterns. The lateral and vertical consumptions of the SiN hard mask are due to sputtering effects occurring on a 3D pattern during the implantation step. Indeed, it is known that the sputtering is dependent on the ion incidence angle.[32] In general, it increases with ion incidence angle and reaches its maximal yield for incidence angle comprised between 50° and 80°. SRIM simulations were runned to simulate the angular dependence of the sputtering yield of the Si_3N_4 film (density 2.2 g/cm^3) by 140 eV He ions. They reveal that the maximal sputtering yield occurs at ion incident angle of 70° and is about 50% higher than the one at normal incidence. It is seen in Fig. 12 that the SiN hard mask profile is square before etching and turns into facetted at the top after one cycle, highlighting an enhanced consumption of the SiN at the top corner where the ion incidence angle is higher than the normal. As the pattern critical dimensions are initially small of about 30 nm, the facets formed at the corners join together and the top SiN pattern surface is not flat anymore and will not be sputtered similarly as a blanket wafer. We suspect that for larger pattern dimensions (100 nm), the impact of the faceting would have been less important and the top pattern surface would have remained flat and not consumed by the implantation. Similarly, the lateral consumption of the SiN hard mask is due to sputtering of ion bombarding the sidewalls at grazing incidence. This effect might be enhanced by some charging effects that deflect the ions on the SiN sidewalls. Indeed, it is noticed that the SiN bottom dimension is laterally more consumed than the SiN middle dimension.

AFM was used to characterize the line edge roughness of the SiN hard mask before process and the InGaAs LER after three cycles of the two-step process and SiN hard mask removal. Figure 13 shows the LER measured all along the pattern height as well as an estimated average LER (LER_{av})

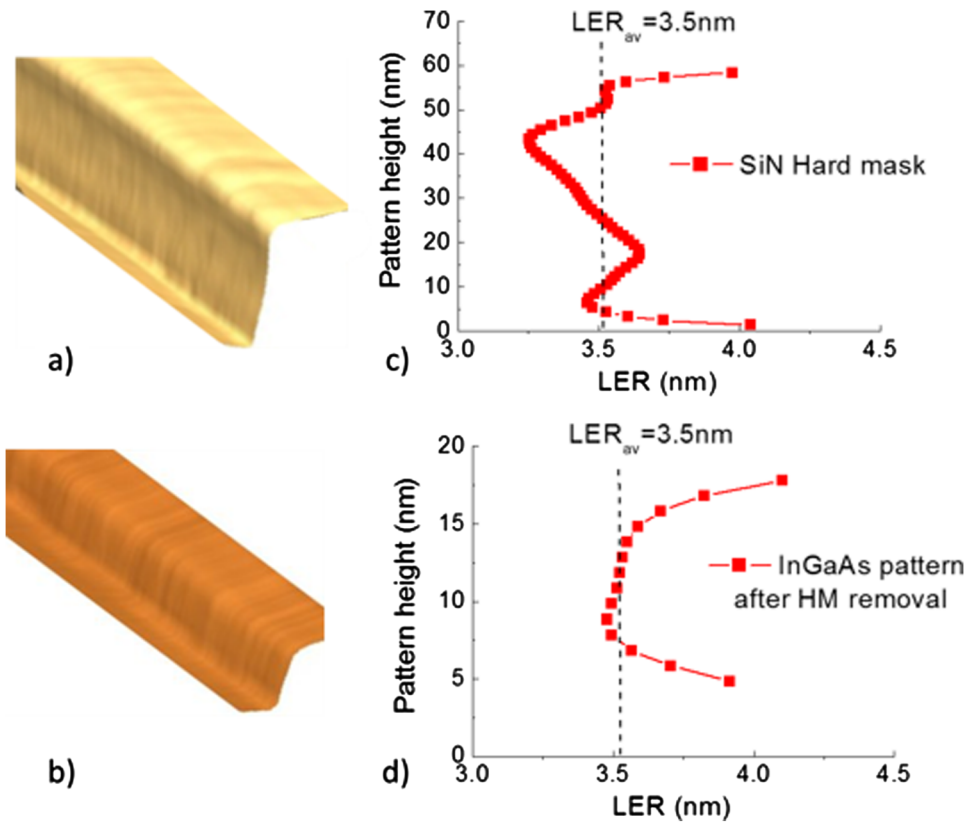

FIG. 13. AFM images of the half-reconstructed pattern profile [(a) and (b)] and estimation of the LER all along the pattern height [(c) and (d)] for [(a) and (c)] SiN hard mask before process and [(b) and (d)] InGaAs pattern after three cycles of the two-step process and SiN hard mask removal with 1% HF during 30 s.

of the sidewalls. It should be noted that the LER increase at top and bottom of the pattern is due to measurement artefacts.[20]

The SiN LER before the process is of 3.5 nm and is identically transferred into the InGaAs layer during the sequence of cycles of the two-step process. It is generally admitted that during plasma etching, the hard mask LER is transferred into the underlayers.[19] In our case, this is a little surprising to retrieve this trend since the SiN hard mask sidewalls are sputtered during the sequence of cycles, which could have modified its sidewalls roughness. Anyway, it seems that the sequence of cycles of the two-step process does not introduce sidewalls roughness, as it was the case for the flat surface. Nanoauger analyses were also performed to get some information on the chemical composition and stoichiometry of the InGaAs sidewalls after three cycles of the two-step process. In the setup configuration, the sample is tilted by 50° from horizontal so that the 30 nm-diameter electron beam can be spotted precisely on the pattern sidewalls. The analyses (not shown here) showed that the sidewalls are enriched in arsenic as like flat surface but that the In/Ga ratio is not impacted. This is again consistent with the arsenic-dominated chemistry in the chemical reactions between the III-As semiconductors and the acids.[27,31]

IV. SUMMARY AND CONCLUSIONS

Conventional plasma processes show intrinsic limitations to control the etching of very thin layers with nanometric precision without introducing damage. In this work, we propose an approach allowing to perform quasiatomic layer etching of thin layers by cycling two self-limited steps. This approach was applied to the etching of InGaAs material with the view to integrate it as a nMOS channel in a FinFET architecture but could be applied to other materials.

The first step uses light ions implantation using He/O_2 plasma performed in an ICP reactor. This step allows to modify InGaAs on a well-defined thickness with limited sputtering. The depth of material modification is well controlled by the ion energy and saturates with process time, giving to this step a self-limited behavior. The implantation conditions selected (100 sccm He/5 sccm O_2/source 800 W/pressure 10 mT/bias power 125 W/90 s) allows to modify the first 6 nm of the InGaAs surface. The modification of the InGaAs layer mainly consists in an oxidation of the III–V elements and especially indium. The modification is not homogeneous and is dependent on the ion penetration profile into InGaAs. Lighter ions such as He will penetrate deeper than heavier O ions. This will result in an upper highly oxidized layer on a lower oxidized layer. In our study, Si coming from the reactor chamber was systematically implanted into the InGaAs layer, whatever the plasma condition or reactor wall conditioning used. The second step uses aqueous wet etching to remove the modified InGaAs layer with infinite selectivity over the nonmodified InGaAs layer as well as over the hard mask (both modified and nonmodified). Acidified solutions such as HCl or HF were tested since they are very effective for removing oxides formed on the InGaAs surface without consuming the bulk material. In our study, HCl was found unefficient to remove the modified InGaAs layer because of the presence of Si contamination. 0.1% HF wet solution was used to remove the modified InGaAs layer selectively over the bulk InGaAs and the SiN materials (pristine and implanted). The HF wet step is self-limited and removes the same modified thickness whatever the HF dilution and process time used. However, it only removes the upper oxidized layer and is not efficient to remove the underneath layer amorphized by the He implantation. The repetition of cycles of the two-step process was applied to etch the thin film of InGaAs as well as pattern using a SiN hard mask. Blanket experiments show that each cycle of the two-step process allows to remove a fixed and reproducible InGaAs thickness of 5.7 nm. The two-step process keeps intact the surface roughness. After such a process, the surface is slightly depleted in indium (−13%) and enriched in arsenic (+28%). If the two-step process is to be used to etch partially an InGaAs film, solutions to retrieve stoichiometric InGaAs surface should be implemented. For instance, NH_4OH solution was proposed by Kang *et al.*[33] to dissolve elemental As present on GaAs and could be efficient on InGaAs. In this study, the ion energy of the implantation step was set to remove several nanometers of the InGaAs film. However, by operating at lower ion energy, the two-step process offers the capability to etch very thin layers of InGaAs (<2 nm) selectively over the underlayer with one or two cycles, which is not so easy to achieve with the conventional plasma process.

The results on pattern were less conclusive. It was possible to transfer the SiN hard mask into the InGaAs layer using cycles of the two-step process. A reproducible thickness of InGaAs was removed at each cycle. The two-step process induced limited damage on the InGaAs sidewalls. It does not generate sidewalls roughness and does not degrade the In/Ga stoichiometry but leads to As enriched sidewalls surface. However, the process leads to tapered InGaAs profile because of the lateral consumption of the SiN hard mask that we did not anticipate. Although the blanket film of SiN is almost not consumed by the two-step process, etching mechanisms differ in 3D. The preferential sputtering of non-normal SiN surfaces (top corner and sidewalls), combined to charging effect deflecting ions on the SiN sidewalls, led to the lateral consumption of the SiN hard mask. To use such a process to transfer patterns anisotropically into thin layers of InGaAs, the masking strategy should be optimized. Metallic hard masks such as TiN could be an option since they are less sensitive to faceting and charging effect than SiN. However, their use would introduce a new issue since they need to be removed after the etch to pursue the integration. This requires the development of a selective removal step of the TiN hard mask over InGaAs without damaging InGaAs.

Finally, the two-step process proposed here is not industrializable, since alternating cycles in two independent equipments (plasma reactor and wet chamber) are not cost efficient in terms of throughput. But the idea behind this study was first to demonstrate the viability of the two-step process with a second step using wet solutions that are

known to provide high selectivity of oxidized InGaAs over bulk InGaAs, and then to develop dry plasma solutions for the III–V oxide removal selectively over bulk III–V that could be performed in the same plasma reactor or platform that the one used for the implantation. Indeed, some research efforts are dedicated today to replace wet cleaning steps by dry plasma solutions using remote plasma source reactor.[34] Some suppliers are even working on the development of reactors equipped with both a capacitive coupled plasma source and a remote plasma source which would make the two-step process industrializable.

ACKNOWLEDGMENTS

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