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Abstract— *This paper focuses on the study of a 5 kV Asymmetrical 4H-SiC thyristor and on its Junction edge termination protection. Based on a numerical semiconductor simulator, doping level and thickness of the different layers that constitute the device will be proposed. Several techniques of periphery protection such as Mesa structure, Junction Termination Extension (JTE) and Epitaxial Guard Rings (EGR$_s$) have been studied. Furthermore we report on the simulation of the finite element thyristor inserted in a circuit for an Electromagnetic Launching (EML) application.*

Index Terms—**SiC, Numerical Simulation, Thyristor, Junction Edge Termination, Mesa, JTE, EGR$_s$, Power Pulse.**

I. INTRODUCTION

THE feasibility of using silicon power thyristor for electric gun application has been established [1]. But a series array of a large number of devices is needed to achieve the required performance. The resulting size and weight of the pulser is non-optimal. The material properties of silicon carbide (SiC) indicate the potentiality of reducing the size and the power losses of the power devices [2]. SiC has a bandgap three times wider than that of silicon, high critical electric field of 2-4.10^6 V/cm, high thermal conductivity of 4.9 w/cm.K and high electron saturation velocity of 2.10^7 cm/s. This paper investigates the design and the performance of a 5 kV Asymmetrical 4H-SiC thyristor as main switch in EML applications where high power pulses are needed.

Based on the simulation result, the evaluation of a 4H-SiC thyristor is carried out with regard to the electrothermal effect. A two dimensional (2D) finite element simulation package ISE is used [3]. The numerical simulator solves coupled, non-linear partial differential semiconductor equations and predicts the electrical characteristics that are associated with specified physical structure and bias conditions.

The study of the peripheral protection, that is an important issue in the design of SiC power devices is considered and the optimal breakdown voltage for each technique (Mesa, JTE and EGR$_s$) will be presented to terminate this static study.

In the dynamic simulation we investigate the thyristor in a circuit to estimate the switching performance and to predict the minimum area for a 20 kA current pulse.

II. SIMULATION PARAMETERS AND MODELS

A. Models used for the simulation

The physical models installed in the simulator are used with the material parameters tuned for 4H-SiC. The most important physical models used are for bandgap, mobility, SRH recombination, impact ionization.

1) Bandgap Energy : The variation of the intrinsic SiC bandgap with temperature is expressed by :

$$E_g(T) = E_g(0) - \frac{\alpha . T^2}{(T + \beta)} \qquad (1)$$

Where T is the lattice temperature, and $E_g(0)$ is the bandgap at 0 K (Eg(0)= 3.26 eV). The values of

the parameters α and β are respectively $33x10^{-5}$ $eV.K^{-1}$ and 0 K.

2) Carrier mobility : The electron mobility μ_n and hole mobility μ_p are modeled by the Caughey-Thomas's equation :

$$\mu_n = \frac{700}{1+\left(\frac{N_A+N_D}{1.94x10^{17}}\right)^{0.61}}\left(\frac{T}{300}\right)^{-2.15} \quad (2)$$

$$\mu_p = 15.9 + \frac{170}{1+\left(\frac{N_A+N_D}{1.76x10^{19}}\right)^{0.34}}\left(\frac{T}{300}\right)^{-2.15} \quad (3)$$

Where N_A and N_D are local impurity concentrations. The $\mu_p$max and $\mu_n$max are fitted from the literature data [6].

3) Generation and recombination : The Shockley-Read-Hall (SRH) recombination-generation rate R_{SRH} is used. The lifetime of electrons and holes τ_n and τ_p are modeled as doping level dependent

$$\tau_{n,p} = \frac{\tau_{n0,p0}}{1+\frac{(N_A+N_D)}{10^{16}}} \quad (4)$$

In the simulation, $\tau_{n0} = \tau_{p0} = 10^{-7}$ s is assumed.

3) Impact ionization : The generation rate of electron-hole pairs due to impact ionization is modeled by :

$$\alpha = \gamma a e^{-\frac{\gamma b}{|E|}} \quad \text{with } \gamma = \frac{\tanh\left(\frac{1000\pi}{kT_0}\right)}{\tanh\left(\frac{1000\pi}{kT}\right)} \quad (5)$$

The impact ionization coefficients a and b used are given by Konstantinov [4].

III. Simulation Results

A. Ideal breakdown voltage for a PT structure

The thyristor structure envisaged is asymmetrical with the aim to improve the voltage-blocking characteristics [5]. The maximum blocked voltage in a thyristor is fixed by the thickness and the doping level of its drift layer that corresponds to a punchthrough (PT) structure. The preliminary work was to determine the parameters of a PT structure that allows to obtain a breakdown voltage superior to 5 kV. We present in Fig. 1 the ideal breakdown voltage for a PT structure (N^+P^-P) as a function of doping and blocking layer thickness for 4H-SiC determined by simulation.

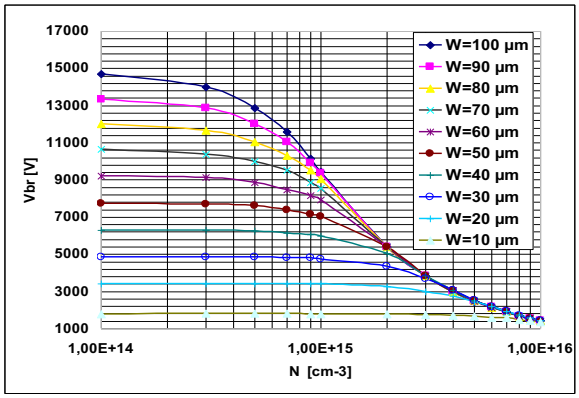


Fig. 1: Ideal breakdown voltage for a PT structure as a function of doping and blocking layer thickness.

In order to facilitate the calculation convergence the simulations are done at 600 K. The breakdown voltage is determined with the ionization integral criterion. The graph (Fig. 1) shows that a blocking voltage greater than 5 kV may be obtained with a doping of 10^{15} cm^{-3} and a thickness of only 35 µm. To obtain a similar results with the silicon it needs more than 100 µm with a doping inferior to 3.10^{13} cm^{-3}.

B. The 5 kV asymmetrical thyristor

Fig. 2 shows a cross-sectional view of the structure used in the simulator and that corresponds to a half cell of an asymmetrical thyristor. Fig. 2 also shows the different technological parameters determined by simulation. Four epitaxial layers are defined on an N^+ 4H-SiC substrate ($1,4.10^{19}$ cm^{-3}-365 µm). The buffer P^+-layer (5.10^{17} cm^{-3}-1 µm) forms a punchthrough structure which blocks the spreading of the depletion layer under forward bias, thus making the device asymmetrical and improving the blocking voltage. The P-type drift layer (10^{15} cm^{-3}-35 µm) is fixed according to the result determined in the study of the 5 kV ideal breakdown voltage (Fig. 1). Control gate was formed on the third N-type base layer (10^{17} cm^{-3}-2 µm) and it is designed to prevent punchthrough under forward blocking. The anode is the topmost

P^+ layer (10^{19} cm^{-3}-1 µm), its high doping level facilitates the hole injection efficiency.

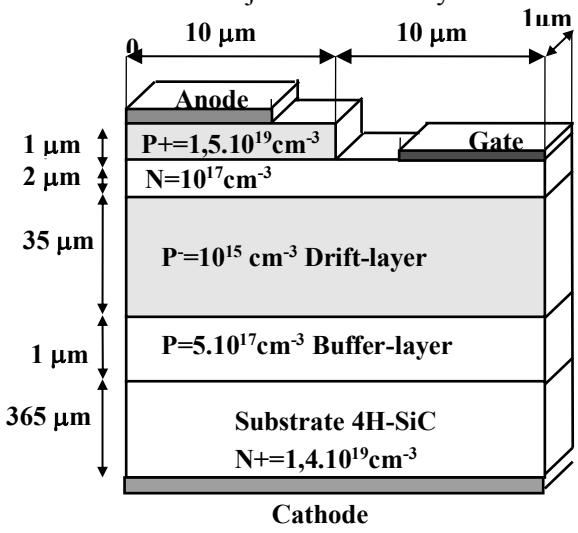
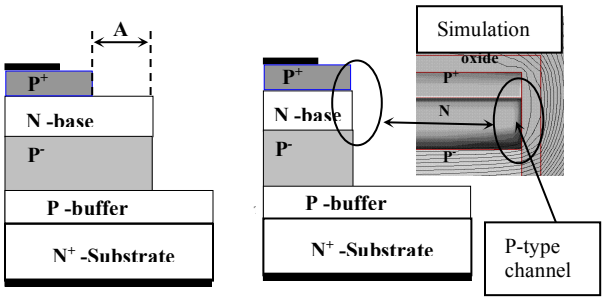


Fig. 2 : Schematic cross-section of the asymmetrical 5 kV thyristor half cell.

Without considering the problems linked to the periphery, the simulation of the structure (Fig. 2) gives a theoretical forward blocking voltage of 5700 V. We obtain a voltage drop V_F = 6 V for 1800 A/cm^{-2} at 600 K. The maximal voltage in this case is limited by avalanche multiplication.

C. Junction Edge Termination Protection

We study here different protection techniques and discuss about their results. We have first considered the Mesa protection shown in Fig. 3. The best configuration corresponds to a vertical etch that reaches the P-type buffer (Fig. 3-a) and for which the maximal voltage is 5600 V. The principal precaution for this technique is to avoid to realize the etch in the extension of the anode etch as it is shown in Fig. 3-b.



a) Mesa with A= 13 µm b) Mesa with A = 0 µm

Fig. 3 : Description of the Mesa

Because this last case allows the creation of P-type channel due to the curving of the equipotential at the edge termination and decrease the blocking voltage down to 1500 V. To circumvent this phenomenon a minimal distance "A = 13 µm" must be set between the anode mesa and edge termination mesa.

The JTE can be an other possibility for terminating the device. It can be realized by forming an N-type region in the p-type drift layer using ion-implantation of nitrogen. First, the study is done without the topmost P^+ layer and the N^+-substrate in order to diminish the simulation time. Then the optimized configuration is applied to the thyristor structure.

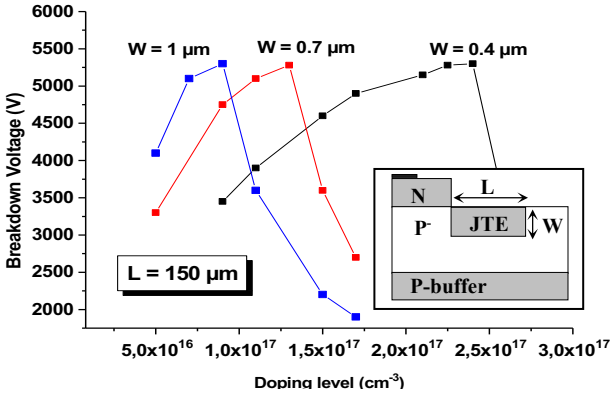


Fig. 4: Breakdown voltage versus doping level for a depth of the JTE "W" equals to 0.4 ,0.7 and 1 µm

Fig. 4 shows the breakdown voltage corresponding to the N-base/P-base/P-buffer structure for three depths of the JTE with a lateral extension L = 150 µm. The optimal result for each depth is 5300 V which corresponds to a dose of 9.10^{12} cm^{-2} of nitrogen. If we apply the optimized case for a depth of 0.4 µm for the thyristor structure, the corresponding blocking voltage is 5500 V.

The last protection studied is called Epitaxial Guard Rings (EGR_s). It consists to etch the N-base to create guard rings. The blocking voltage is sensitive mainly to the ring spacing and the etch depth. The technology we plane to use impose a minimum etch width of 2 µm. The best results is obtained with 5 rings, the space between the ring is 2 µm , the ring width is 12 µm and the etch depth is 2.1 µm. Fig. 5 shows the distribution of the

potential through the EGR_s for the optimized case that gives a blocking voltage of 4100 V.

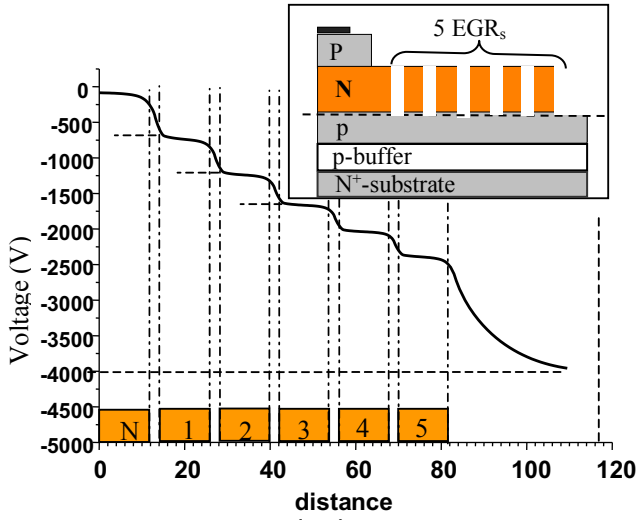


Fig.5 Distribution of the potential through the EGR_s for the optimized structure

D. EML application

The thyristor previously designed is aimed to be used in an EML application. To predict its dynamic behavior we have inserted the finite element thyristor in a circuit (Fig. 6) for an EML application where the other components are SPICE's model defined. The typical current for this application is shaped by the inductance L = 30 µH , the resistance R = 10 mΩ and the capacitance C = 865 µF. Diodes are used as a crowbar switch. The schedule of condition imposed a current pulse superior to 20 kA. The charging voltage of the capacitor is 5 kV. When the thyristor is switched on the current pulse in the load (L and R in series) starts (Fig. 6).

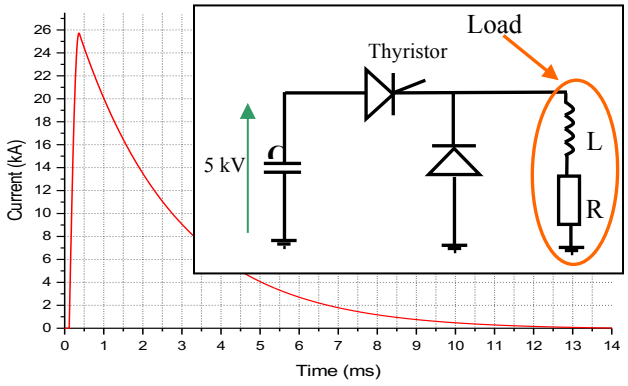


Fig. 6: Application circuit and pulse current

The junction to ambient thermal resistance in the anode and in the cathode are set to 0.05 K/W. According to the electrothermal simulations, the current rate (di/dt) is 160 A/µs, the maximum switching current is 25.68 kA and the thyristor voltage drop (V_F) is only 7.6 V for an active area of 10 cm^2. The comparison with a series silicon thyristor for an identical current density (2500 A/cm^2) and for a similar blocking voltage gives a voltage drop around 20 V with an active area of 20 cm^2.The self heating here induces an increase of the temperature of only 25 K. We have then decreased the active area to 1.5 cm^2 and noticed that the maximum current is reduced to 25.5 kA with V_F = 35 V. The 1.5 cm^2 area contributes to increase the maximum temperature in the device up to 700 K which is supported by SiC.

CONCLUSION

We have investigated the design of a 4H-SiC asymmetrical thyristor and proposed its technological parameters for a 5 kV application. The studies of periphery protection have shown that the Mesa and JTE allow to reach ~98 % of the ideal blocking voltage and the EGR_s only ~72 %. The evolution of the temperature with the area structure can allow to predict interest of SiC for using smaller area device operation.

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REFERENCES

[1] E. Spahn et al., "The use of thyristors as main switches in EML application," IEEE Trans. on Magnetics, Vol. 29, no. 1, pp. 1060-1065, Jan. 1993

[2] B. J. Baliga, "Trends in power semiconductor devices," IEEE Trans. Electron Devices, Vol. 43, pp.1717-1731, Oct. 1996.

[3] ISE Integrated Systems Engineering AG, Zurich/CH (1998)

[4] A. O. Konstantinov, "Ionization rates and critical field in 4H-SiC", Appl. Phys. Lett. Vol.71, no.1, pp. 90-92, Jul. 1997.

[5] Agarwal AK et al., "700 V asymmetrical 4H-SiC gate turn-off thyristors (GTOs)". IEEE Elect. Dev. Lett. Vol. 18, no 11, pp. 518-520, Nov. 1997.

[6] F. Nallet, "Conception, réalisation et caractérisation d'un composant limiteur de courant en carbure de silicium", Thesis INSA de Lyon, 2001