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4H-SiC bipolar power diodes realized by ion implantation

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Abstract—*Physico-chemical and electrical investigations were carried out in 4H-SiC p-type layers created by Aluminum ion implantation at room temperature and high temperature post-implantation annealing. Crystal recovery and dopant preservation after annealing are proved by RBS/C and respectively SIMS measurements. Dopant activation is evaluated by sheet resistance measurements. These results were applied for high voltage bipolar diodes with JTE protection realization.*

Index Terms: **- SiC, ion implantation, SIMS, recrystallization, electrical activation, high voltage diode, JTE**

I. Introduction

SILICON carbide (SiC) is regarded with many attention for high-power, high-temperature and high-speed electronic applications.

P^+-N junctions used in bipolar power device structures must be realized by ion implantation, which is the only available method to locally dope SiC due to very low diffusion coefficients of dopants. This technique is also needed for ohmic contact formation, a high doping concentration being necessary for reducing contact resistance. Aluminum (Al) and Boron (B) are the principal p-type dopants used, both residing in silicon sites for an acceptor behavior. Al dopant is preferred due to its energy level in the SiC band gap nearer to the valence band, around 0.2 eV for Al and 0.3 eV for B. Nevertheless the high ionization energy of dopants imposes to raise the implanted dose, and therefore amorphous layers are formed in the case of ion implantations realized at room temperature. High temperature ion implantations are realized to avoid amorphous layer generation, typically in the 300-600°C range, this method being noticed by its heavier implementation. To obtain well-activated p-type SiC regions in a well-preserved crystalline state, high temperature post-implantation annealing, generally around 1700°C, in particular conditions is needed. In this paper we present a study of Al room temperature (RT) ion implanted and high temperature annealed samples leading to viable physico-chemical and electrical properties of the p-type layers formed. These results were applied to realize power bipolar diodes with junction termination extension.

An interdependent work was carried out between device structure design conception, electrical behavior simulation, their fabrication and experimental results.

II. P-TYPE SIC LAYER CREATION BY ION IMPLANTATION

A. Experimental

Aluminum implantations were performed at room temperature in n-type 4H-SiC epitaxial layers purchased from Cree Research (epitaxial doping $1x10^{16}cm^{-3}$) with energies ranging from 25 up to 300 keV (Table 1). A total dose of $1.75x10^{15}cm^{-2}$ was implanted in disoriented samples to avoid channeling effects along crystal axes. Samples were cut out in 5x5 mm^2 surface.

Energy (keV)	Fluence (cm^{-2})
300	$8x10^{14}$
190	$3.9x10^{14}$
115	$2.8x10^{14}$
60	$1.9x10^{14}$
25	$9x10^{13}$

Table1. Ion implantation energies and fluences of Al in 4H-SiC

All these samples were annealed in a SiC dedicated J.I.P.ELEC™ rf-induction heating furnace [1] at the center of the susceptor as shown in Fig.1. An inert argon atmosphere with a silicon

carbide partial pressure was used. Before to reach a constant temperature plateau in the 1700-1800°C interval during 30 mn, a preliminary heating rate of 40°C/s was utilized. The decreasing of the temperature at the end of the annealing is governed by thermal inertia.

SiC annealing in a rf-induction furnace presents important advantages such as very high heating rate. This allows the recrystallization of amorphized layers. Especially 4H and 6H-SiC samples need a very high heating ramp to preserve the polytype from cubic inclusions, which may be generated during the solid phase epitaxy at too low temperature [2,3].

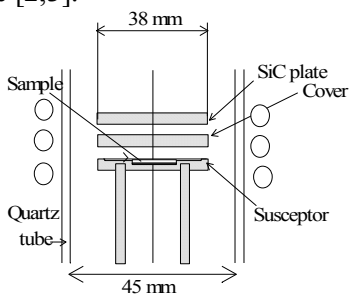

Fig. 1. SiC dedicated J.I.P.ELEC^{TM} rf-induction heating furnace

An inhomogeneous temperature of the heated wafer support (susceptor) is a drawback of the induction technique. Lateral and vertical thermal variations can induce SiC etching if appropriate environments and configurations rich in silicon and carbon are not provided. Si is known to volatilize towards 1300°C [4] under one atmosphere pressure, and without a Si supersaturating vapor the carbonization of the surface is unavoidable.

Dopant distributions for as-implanted samples and after annealing have been investigated by Secondary Ion Mass Spectroscopy (SIMS) measurements, and have been compared to I^{2}SiC Monte Carlo simulations of Al implantations in 4H-SiC. I^{2}SiC simulator [5,6] takes into account the hexagonal polytype silicon carbide structure. It was also utilized to find the optimal sample orientation during the ion implantation to avoid dopant channeling along 4H-SiC axes.

Rutherford Backscattering Spectrometry in the Channeling mode (RBS/C) has alloyed to analyze damages induced in materials by ion implantation and recrystallization following high temperature annealing. Electrical activation of dopants, i.e. incorporation of Al in substitutional Si lattice sites, has been evaluated by sheet resistance measurements with a four point probe technique.

B. Results and Discussion

1) SIMS analyses

In Fig.2 are presented SIMS Al profiles realized in as-implanted and 1700°C during 30 min post-implantation annealed samples. SIMS profiles of both as-implanted and annealed samples agree with the I^{2}SiC simulations even in the channeled part.

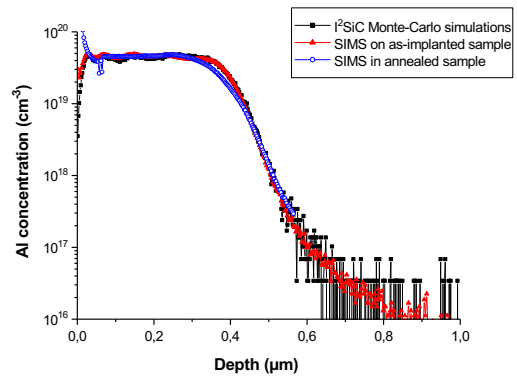

Fig. 2. SIMS analyses in as-implanted and annealed samples compared to I^{2}SiC Monte-Carlo simulation.

No dopant loosing occurs after high temperature annealing by SiC etching or Al exodiffusion and no layer deposited on implanted surface have been detected in the species density and thickness ranges available by SIMS.

2) RBS/C measurements

RBS/C spectra were carried out on 4H-SiC samples before and after annealing to evaluate residual damage and SiC recrystallization.

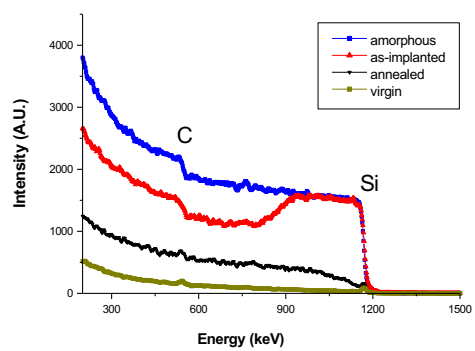

Fig. 3. RBS/C analyses on as-implanted and 1700°C during 30 mn annealed samples

They have been compared (Fig. 3) to an intentionally disoriented analyzed sample (amorphous) and a not implanted one (virgin).

The as-implanted sample spectra reaches the amorphous one up to the surface, this confirms the presence of an amorphous layer, the implant dose being superior to the threshold of an amorphous layer formation [2]. For the as implanted sample a 0.31 µm amorphous layer is found, the energy conversion to depth in RBS/C spectra was made using equation 1, a constant SiC density value (3.21 g/cm^{-3}) was considered.

$$a = \frac{E_R(0) - E_R(a)}{k\left(\frac{dE}{dx}\right)_{in} + \frac{1}{\cos(\pi - \theta)}\left(\frac{dE}{dx}\right)_{out}} \qquad (1)$$

with:

$E_R(0)$ - He ion energy scattered by silicon atoms in surface

$E_R(a)$ - He ion energy scattered by silicon atoms at a depth *a*

$\left(\frac{dE}{dx}\right)_{in}$ - the stopping power during its penetration in the SiC target

$\left(\frac{dE}{dx}\right)_{out}$ - the stopping power in the target after the collision

k - kinematic factor, representing the ratio of He ions energy after scattering on Si atoms and He incident energy (equation 2)

θ - scattering angle

After high temperature annealing of Al implanted samples, the RBS/C spectrum shows a strongly reduced crystalline defect density and no amorphization zone. The backscattering yield after 1700°C during 30 mn annealing is 6.3% for the RT Al implanted sample which is 4,6% more compared with the virgin, non-implanted sample. Nevertheless that represents a good sample crystallinity after annealing for an amorphized room temperature implanted sample.

3) Electrical activation

Sheet resistance measured on Al implanted and high temperature annealed samples by a RT four point probe technique indicate an appreciable electrical dopant activation for room temperature implanted samples.

For 1750°C during 30 mn annealed samples a 10 kΩ/□ sheet resistance is found, which corresponds to a 70 % electrical dopant activation. An ionization energy of 0.18 eV for Al dopant in 4H-SiC and a mobility of 30 cm^{2}V^{-1}s^{-1} for hole carriers have been assumed for calculation.

III. Bipolar diodes with junction termination extension design and realization

1) Device structure design

Commercial MEDICI™ software from Avant! Corporation was used to simulate bipolar diodes with junction termination extension (JTE). On the basis of the 4H-SiC wafer characteristics to be used for device fabrication, (1.375'' CREE wafer diameter with a 40 µm thick n-type epitaxial layer doped at 1.1x10^{15}cm^{-3} and grown on a n-type substrate), geometrical parameters and p-type doping concentrations of the JTE were optimized in order to obtain maximal breakdown voltage.

For the p$^+$-emitter and JTE protection doping (Fig.4), which are carried out by Al$^+$ implantation during device fabrication, I^{2}SiC simulation doping profiles were directly introduced into MEDICI program. Doping profile shape, and especially the channeling part, plays a significant role in the reverse bias behavior.

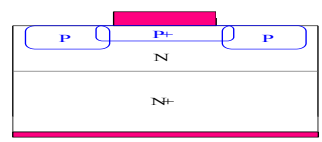

Fig. 4. Schematic cross-section of a bipolar JTE structure

Simulated breakdown voltages versus JTE doping are plotted in Fig.5. A firstly linear increase of the breakdown voltage is followed by an abrupt fall after passing by a maximum.

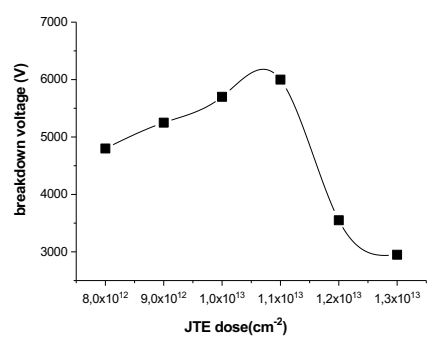

Fig. 5. Breakdown voltage versus JTE dose variation

An equilibrate electric field repartition have been tried to found between p$^+$ emitter extremity and the JTE protection one, at the breakdown occurrence. Thus a dose of 1x10^{13} cm^{-2} was chosen for the JTE doping in 4H-SiC bipolar diodes realized.

JTE bipolar diodes with different areas (Fig.6) were realized on 4H-SiC wafer. The same ion implantation parameters (Table 1) were utilized for the p^+ emitter. A 1700°C during 30 mn post-implantation annealing was carried out.

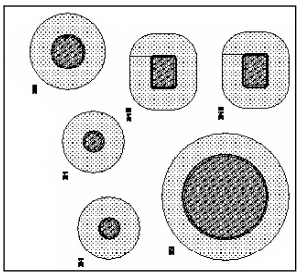

Fig.6. Top mask view of bipolar JTE diodes with emitter area varying from 4.9×10^{-2} mm^2 to 7.9×10^{-1} mm^2.

2) Experimental results

Current density vs. Voltage (J-V) measurements were realized at room temperature. In Fig.7 the results obtained on a single 5x5 mm^2 field are presented.

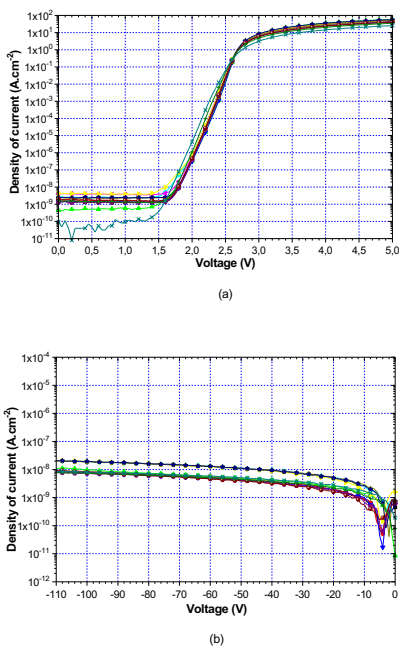

Fig. 7. J-V characteristics on a single 5x5mm^2 field. (a) forward bias (b) reverse bias

A good homogeneity was observed in the electrical characteristics over the whole processed wafer (80 % of 250 µm-diameter diodes presented J(V) curves as shown on Fig.7). That denotes the good contribution of ion implantation and post-implantation annealing preliminary study. However the yield remains depending on the device size (65 % of the 1 mm-diameter diodes exhibited excess-current below the conduction threshold voltage and under reverse bias), as a consequence of the crystal quality. 60 A cm^{-2} current density is found at a forward bias of 5 V and less than 10^{-7} A cm^{-2} under 110 V reverse bias.

These diodes have shown maximum blocking voltage capabilities, higher than 1.1kV in air ambient and 2.3 kV in an SF_6 rich ambient [7]. SiC passivation remains an important problem to be solved to benefit from the remarkable silicon carbide potentialities for high-power device applications.

CONCLUSION

The bipolar diodes realized in JTE geometry have a good behavior in forward and in reverse bias. P-type layers locally realized by ion implantation and post-implantation annealing is an essential and necessary stage in silicon carbide high-power device realization.

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