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Thibaud Denneulin, David Cooper, Jean-Michel Hartmann, Jean-Luc Rouvière. The addition of strain in uniaxially strained transistors by both SiN contact etch stop layers and recessed SiGe sources and drains. Journal of Applied Physics, 2012, 112 (9), pp.094314. 10.1063/1.4764045 . hal-02145343

HAL Id: hal-02145343

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Journal of Applied Physics

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Cite as: J. Appl. Phys. **112**, 094314 (2012); https://doi.org/10.1063/1.4764045
Submitted: 14 May 2012 . Accepted: 09 October 2012 . Published Online: 06 November 2012

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The addition of strain in uniaxially strained transistors by both SiN contact etch stop layers and recessed SiGe sources and drains

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(Received 14 May 2012; accepted 9 October 2012; published online 6 November 2012)

SiN contact etch stop layers (CESL) and recessed SiGe sources/drains are two uniaxial strain techniques used to boost the charge carriers mobility in p-type metal oxide semiconductor field effect transistors (pMOSFETs). It has already been shown that the electrical performances of the devices can be increased by combining both of these techniques on the same transistor. However, there are few experimental investigations of their additivity from the strain point of view. Here, spatially resolved strain mapping was performed using dark-field electron holography (DFEH) on pMOSFETs transistors strained by SiN CESL and embedded SiGe sources/drains. The influence of both processes on the strain distribution has been investigated independently before the combination was tested. This study was first performed with non-silicided devices. The results indicated that in the channel region, the strain induced by the combination of both processes is equal to the sum of the individual components. Then, the same investigation was performed after Ni-silicidation of the devices. It was found that in spite of a slight reduction of the strain due to the silicidation, the strain additivity is approximately preserved. Finally, it was also shown that DFEH can be a useful technique to characterize the strain field around dislocations. © *2012 American Institute of Physics*. [http://dx.doi.org/10.1063/1.4764045]

I. INTRODUCTION

Strain engineering can be used to improve the performances in microelectronics devices. Different biaxial or uniaxial processes are available to increase the mobility of the charge carriers.[1] Uniaxial processes such as SiN contact etch stop layer (CESL) or SiGe SD (recessed SiGe sources and drains) have received more attention lately and have been adopted since the 90 nm technology node.[2] SiN CESL can be either tensile for n-type metal oxide semiconductor field effect transistors (MOSFETs) or compressive for p-type MOSFETs. SiGe SD induces uniaxial compressive strain but can be replaced by $Si_{1-y}C_y$ for tensile strain.[3] It is usually admitted that uniaxial strain techniques are additive.[4] Several studies indicate that, indeed, performances can be increased by using multiple stressors.[5–7] However, apart from simulations,[8] there have been few investigations of this idea from the point of view of strain. Here, we have used a transmission electron microscopy (TEM) based technique called dark-field electron holography (DFEH) to analyze the distribution of the strain in uniaxially strained pMOSFET-like structures.

Convergent beam electron diffraction (CBED) has long time been considered as the most suitable way to measure strain by TEM.[9] While the sensitivity of CBED is relatively good (2×10^{-4}) (Ref. 10), the interpretation of the patterns is rather complicated and requires comparisons with simulations. Currently, industrials tend to use nanobeam electron diffraction (NBED) because the technique is relatively easy to set up and the data treatment can be fully automated.[11] However, the NBED technique is not so sensitive. The best reported sensitivity is 6×10^{-4} (Ref. 12). Very often it requires a careful statistical interpretation of the data.[13] More importantly, it is still a 1D profiling technique. Acquiring strain maps requires the treatment of very large data sets which can be very time consuming. Dark-field electron holography is an imaging technique that can be used to quantitatively map the strain through the phase of the electrons.[14] The principle is to orientate the sample into a slightly off-zone-axis configuration and to select electron beams diffracted by a given family of planes using an aperture. Then, electrons diffracted by both the region of interest (here, the transistors) and a region of reference (the substrate) are interfered by means of an electron biprism. In Lorentz mode, the sensitivity can be as high as 2×10^{-4} with a spatial resolution of 5 nm and a field of view of about $600 \times 600\,nm^2$ (Ref. 15). The strain in a specific direction can be directly calculated from one hologram using a geometrical phase analysis (GPA) algorithm. Data treatment is very straightforward and takes only a few seconds per hologram using a standard desktop computer.

In this work, the strain induced by a SiN CESL and SiGe SD pMOSFETs was investigated independently. Then, the combination of both processes was tested to check for strain additivity. This study was first performed with non-silicided devices. Then, the same investigation was carried out with Ni-silicided devices.

II. EXPERIMENTAL PROCEDURE

The devices comprised regular arrays of 90 nm long and several cm wide SiO_2/Si_3N_4 dummy gates on (100) wafers with a 500 nm pitch. Five different configurations were examined and are summarized in Table I. In the first case,

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TABLE I. Summary of the different configurations examined. The X symbol indicates that the corresponding process was used.

Configuration number	1	2	3	4	5
Recessed $Si_{0.65}Ge_{0.35}$: B SD		X	X	X	X
Ni(Pt) silicidation				X	X
Compressive SiN CESL	X		X		X

the structures were strained using only a 80 nm thick compressive SiN CESL. In the second case, 50 nm deep *in situ* B doped ($\simeq 2 \times 10^{20}\,cm^{-3}$) $Si_{0.65}Ge_{0.35}$ recessed sources and drains were grown at 650 °C, 20 Torr by reduced pressure chemical vapor deposition (RP-CVD) after HCl etching of Si recesses.[16] The third case combined the two previous cases by depositing the CESL over the recessed SiGe SD. In the fourth and fifth cases, $Si_{0.65}Ge_{0.35}$: B SD were grown again and then silicided. The wafers were covered by a 6 nm thick layer of Ni(Pt) with 5% of Pt and annealed in Ar during 60 s at 300 °C. Silicidation was then carried out at 430 °C during 30 s. SiN CESL was added only in the fifth case.

Samples were prepared for electron holography into $[1\bar{1}0]$ parallel-sided cross-sections using a dual beam (focused ion beam, scanning electron microscope) platform FEI Strata 400. The sample surface was protected using a resist and then a 3 μm thick tungsten layer. The final milling was carried out at 8 kV with a tilt angle of $\pm 2°$ to provide parallel sides for the holography experiments. The final thickness of the specimens was in the 100-200 nm range. Dark-field electron holography was performed on a FEI Titan transmission electron microscope using an operating voltage of 200 kV. The objective lens was switched off and the Lorentz lens was activated for a larger field-of-view. A conventional off-axis setup was adopted using an electron biprism in the image plane of the objective lens. The biprism was biased with a voltage of +180 V corresponding to a fringe spacing of 2 nm. Beams diffracted by a given family of plane were selected using a 10 μm objective aperture in dark-field mode. Information in the [001] and [110] directions was obtained by selecting the (004) and (220) diffraction spots, respectively. Acquisitions were performed for 64 s for signal-to-noise improvement.[15] The reconstruction of the holograms was carried out using a home-made geometrical phase analysis plug-in for Digital Micrograph. More details about the data treatment method are described in Béché *et al.*[17] Here, the spatial resolution is 6.6 nm according to the full width at half maximum (FWHM) of the inverse Fourier transform of the Gaussian mask used for the reconstruction.

Finite element simulations of the SiGe SD sample were carried out for better understanding of the epitaxial strain. Simulations of the thin foil were performed in 3D within the framework of the structural mechanics module of COMSOL Multiphysics. The geometry of the model was built according to TEM observations. The crystalline thickness of the sample was determined by CBED.[18] Only the elastic strain induced by the epitaxial growth was taken into account in the model. The lattice parameter of $Si_{(1-x-y)}Ge_xB_y$ was calculated using the formula,

$$a_{Si_{(1-x-y)}Ge_xB_y} = 5.43105 + 0.1988x + 0.028x^2 - 1.579y \quad (1)$$

(Å).[19,20] The stiffness coefficients of Si and Ge were taken from the literature. For comparison with the experiment, strain maps and profiles were obtained from the model by averaging the strain over the thickness of the thin foil.

In order to study the variation of the germanium distribution after silicidation, scanning TEM high angle annular dark-field imaging (STEM-HAADF) and energy dispersive x-ray spectroscopy (EDS) were also performed. Relative concentration profiles were obtained from EDS spectra using FEI TIA software.

Sections III–VI of this paper give a qualitative description of each configuration. A quantitative comparison is made in Sec. VII.

III. COMPRESSIVE SIN CESL

Figure 1 shows the results corresponding to the devices strained using only a compressive SiN CESL. Figure 1(a) is a Lorentz TEM image of the transistors. Dark-field (220) hologram and the reconstructed ε_{xx} strain map are shown in (b) and (c), respectively. Strain profiles extracted from the map along the arrows drawn in (c) are shown in (d). Similarly, (004) hologram, ε_{zz} strain map, and profiles extracted from the map are shown in (e)–(g). The strain is defined as follows:

$$\varepsilon = \frac{d_{ROI} - d_{Si}}{d_{Si}}, \quad (2)$$

where d_{ROI} is the lattice spacing of the crystal in the region of interest (i.e., the transistor region) and d_{Si} is the lattice spacing of the relaxed silicon substrate. As a convention in this paper, negative strain corresponds to compression while positive values correspond to tensile strain.

As expected, in the in-plane x direction (c) and (d), the silicon crystal is under compression below the gates. The strain map shows that the compressed area is triangular shaped with a base parallel to the channel. The ε_{xx} strain close to the surface is $-0.35 \pm 0.02\%$. In addition, the map shows that between the gates, the silicon is tensile strained with a maximum of 0.2%. Therefore, the CESL modifies completely the lattice plane distances near the surface. Deeper in the substrate (between 100 and 300 nm depth), the sign of the strain changes. This strain amplitude is very small (between $\pm 0.1\%$) but at this depth, it becomes positive under the gates and negative in-between them.

Note concerning the uncertainty of measurement: The precision is usually defined by the standard deviation of the strain calculated in a non-strained region of the substrate.[21] Here the standard deviation is 0.04% for the ε_{xx} strain map and 0.02% for the ε_{zz} strain map which means that the uncertainty is on the third significant digit. However, such a precision is not useful here since strain variations from device to device can be higher than 0.1% (as discussed further, in Sec. VII). Therefore, most of the given values are limited to two significant digits.

In the z, i.e., the [001] direction (f) and (g), large and round shaped strain areas are observed below the gates.

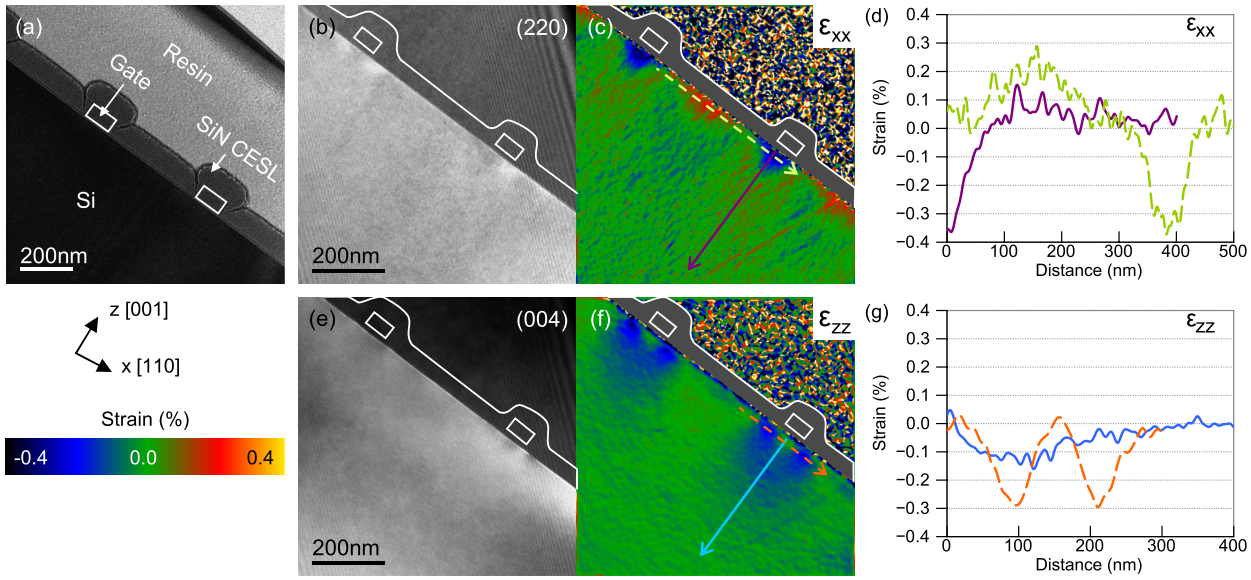

FIG. 1. (a) Lorentz image of dummy gates strained using a compressive SiN CESL. The image was slightly defocused to make the CESL clearer. (b) Dark-field (220) hologram. For indication, the gates have been drawn onto the hologram. (c) ε_{xx} strain map reconstructed from the hologram. (d) Strain profiles extracted from the map according to the arrows. (e) Dark-field (004) hologram, (f) ε_{zz} strain map, and (g) profiles extracted from the map. The profiles were averaged over 6 nm in the perpendicular direction. The profiles along the channel direction (dashed) were placed at 6 nm below the silicon surface.

(004) lattice planes are therefore bent around the gates due to the compression in the perpendicular direction. Just below the surface (a few nm depth), the ε_{zz} strain is positive and then negative with a maximum of -0.1% at 100 nm depth. The (004) lattice planes are therefore pushed deeper in the substrate and piled up which leads to negative strain. This large negative area can be responsible for the slightly positive strain in the [110] x direction. Stabilization is observed at 350 nm depth. Maximum strain levels of -0.3% are measured just below the corner of the gates. This can be due to the opposition of the compression induced by the CESL and the relaxation of the silicon which tends to push the planes further from the gates.

IV. RECESSED SIGE SOURCES AND DRAINS

The results corresponding to the transistors strained using recessed $Si_{0.65}Ge_{0.35}$:B sources and drains are shown in Fig. 2. Figure 2(a) is a Lorentz TEM image of the transistors. Dark-field (220) electron hologram and the reconstructed ε_{xx} strain map are shown in (b) and (c). The ε_{xx} strain map obtained by finite element simulation is shown in (d). Figure 2(e) is a zoom of the strain map (c) in the middle of the SiGe region; as indicated by a dotted square. Dark-field (004) hologram, experimental and simulated ε_{zz} strain maps are shown in (f)–(h). Profiles extracted from the strain maps according to the arrows are shown in (i) and (j). Here, the standard deviation of the strain in the substrate is 0.03% and 0.06% for the ε_{xx} and ε_{zz} strain maps, respectively.

The channel ε_{xx} compression is higher than in the case of the SiN CESL and the maximum value is -1.5%. From the silicon surface to the substrate, the strain decreases rapidly to -0.2% at 40 nm depth. Then the decrease is slower and the lattice is unstrained at 150 nm depth. The source and drain areas are positively strained with maximum values of 0.6% under the gate. If the epitaxial growth were perfect, the (220) interplanar distances should be the same in both the Si and SiGe regions at least far from the channel region. It means that the ε_{xx} strain which is defined here relative to the silicon substrate should be zero. This is approximately true in between two gates, in the region indicated by a dotted square in Fig. 2(c) (zoomed in Fig. 2(e)). However, some misfit dislocations are observed at the (001) Si/SiGe interface. For instance, a dislocation is pointed out by a white arrow in Fig. 2(e). It can be clearly seen that relaxation in the SiGe region flows from the dislocations. The simulated ε_{xx} strain in the source and drain is lower than the experimental strain. For example, at 180 nm in (i), the experimental strain is 0.6% against 0.3% for the simulation. Therefore, the relaxation of the SiGe is partly due to the geometry of the transistor but is also enhanced by the dislocations. The compression measured in the channel is not as high as expected by the simulation. It can be due to the dislocations or to the influence of the gate which was not taken into account in the model.

Arrows in the (004) hologram (f) indicate regions with very low contrast inside and below the source/drain region. This phenomenon is due to the relaxation of the strain at the free surfaces of the TEM lamella.[22] Reticular planes are curved which makes it difficult to obtain homogeneous diffracting conditions. The fringe contrast is reduced in those dark regions, leading to noise in the strain map (g). Therefore, the ε_{zz} profiles were extracted from the region that shows the best contrast. The SiGe is expected to be tensile strained in the [001] growth direction, in order to accommodate the compression of the lattice in the [110] direction. The dashed profile in (j) indicates a ε_{zz} strain of 1.5% in the sources and drains. Using the formula (1), the lattice mismatch between relaxed $Si_{0.6458}Ge_{0.3500}B_{0.0042}$ and relaxed Si which is defined $(a_{SiGe:B} - a_{Si})/a_{Si}$ with a the lattice parameter,

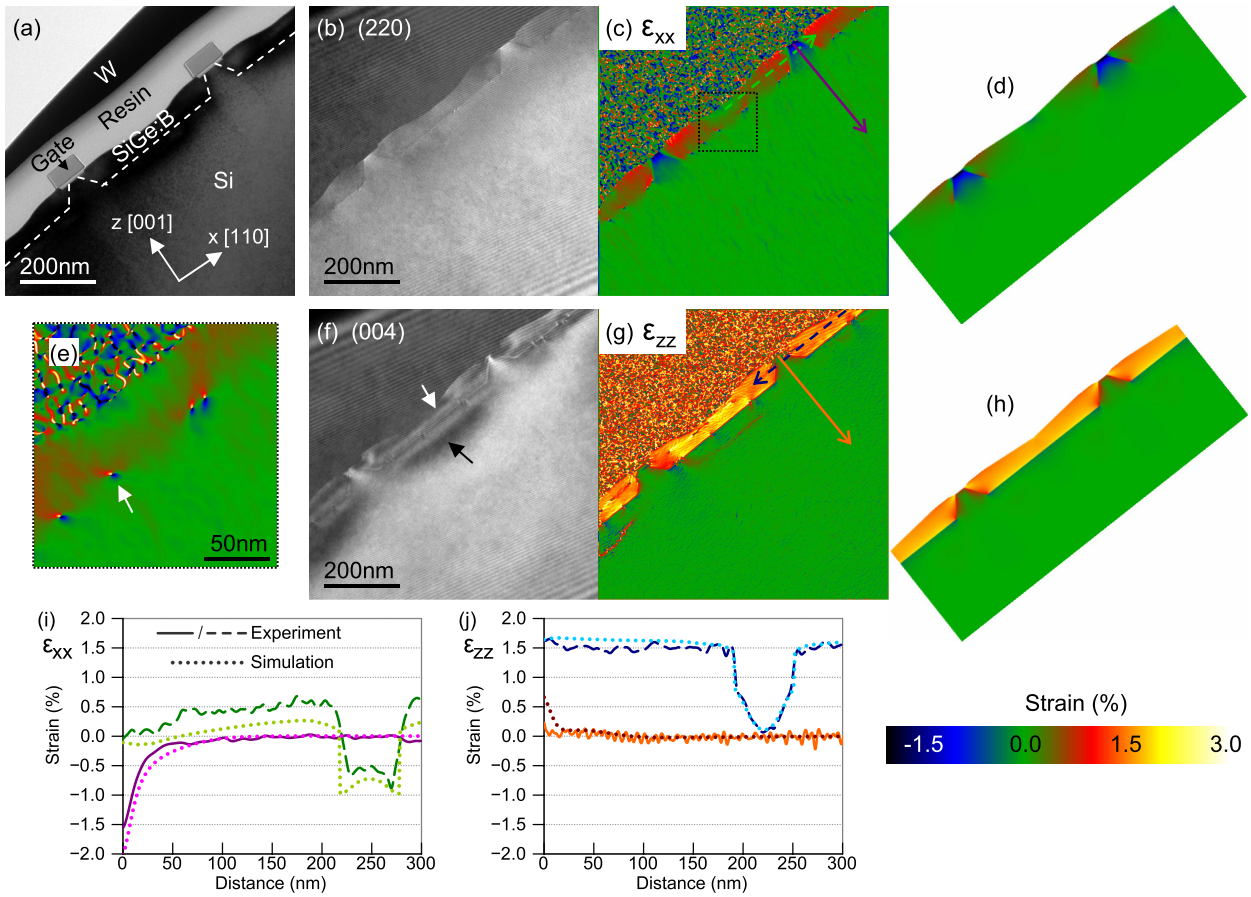

FIG. 2. (a) Lorentz image of the dummy gates strained using recessed $Si_{0.65}Ge_{0.35}$: B sources and drains. (b) Dark-field (220) hologram and (c) reconstructed ε_{xx} strain map. (d) Simulated ε_{xx} strain map. (e) Zoom of the ε_{xx} strain map in the region indicated by a dotted square in (c). (f) Dark-field (004) hologram, (g) experimental, and (h) simulated ε_{zz} strain map. Note that the measurements were performed on the same lamella but not exactly on the same devices for the two directions. (i) Profiles extracted from the ε_{xx} strain map according to the arrows drawn in (c). Profiles extracted from the simulation are shown as dotted lines. (j) Profiles extracted from the experimental and simulated ε_{zz} strain maps. The profiles were averaged over 6 nm in the perpendicular direction. The profiles along the channel direction (dashed) were placed at 20 nm below the channel surface.

can be estimated to be 1.2%. It confirms that the SiGe:B regions are indeed tensile strained relative to their relaxed state. The dislocations can be expected to reduce the ε_{zz} strain. However, the agreement with the simulation is quite good and there is no obvious sign of relaxation for this direction. There is almost no ε_{zz} strain in the middle of the channel (see plain profile in (j)). As shown by other authors using finite element simulations,[23] the ε_{zz} strain decays rapidly away from the inclined Si/SiGe interface. It is in good agreement with our simulation except in the first 10 nm below the gate oxide.

V. COMPRESSIVE SIN CESL AND SIGE SD

The results for the devices compressed using recessed $Si_{0.65}Ge_{0.35}$: B sources and drains and SiN CESL are shown in Fig. 3.

In the present case, the maximum in-plane ε_{xx} compression value below the gate is −1.8% (d) which is slightly higher in absolute value than in the previous situation. Moreover, the decrease of the strain as a function of depth is slower. For comparison, at 40 nm depth, the measured strain is −0.5% instead of −0.2%. Misfit dislocations are still observed at the (001) SiGe/Si interface. Some dislocations are also present at the inclined (111) interfaces, at the edge of the recesses. A dislocation is pointed out by a white arrow in Fig. 3(e). The ε_{xx} strain in the sources and drains is similar to what was observed for SiGe SD alone.

In the [001] growth direction (g) and (h), there is still no strain in the middle of the channel close to the surface. However, deeper in the substrate, the same phenomenon of round shaped strain field is observed as seen for SiN CESL alone (indicated by a dotted curve in Fig. 3(g)). At 100 nm depth, the ε_{zz} strain is −0.2%. Moreover, on the left part of the dashed profile (h), it can be seen that the variation at the vertical Si/SiGe interface is less abrupt than in the case of SiGe SD alone. It means that the influence of the SiN CESL goes through the SiGe sources and drains and decreases the ε_{zz} strain. The right part of this profile is affected by a dislocation.

Figure 4(a) is a zoom of the (220) dark-field hologram in the region indicated by a dashed square in Fig. 3(e). This region contains two misfit dislocations that can be seen by the rupture of the interference fringes. Figure 4(b) is a zoom of the ε_{xx} strain map reconstructed from the hologram. Figure 4(c) is a high resolution STEM-HAADF image of the same region. Dislocations were identified to be 60° dissociated dislocations with $1/2\langle 110\rangle$ type Burger vectors and $\{111\}$ slip

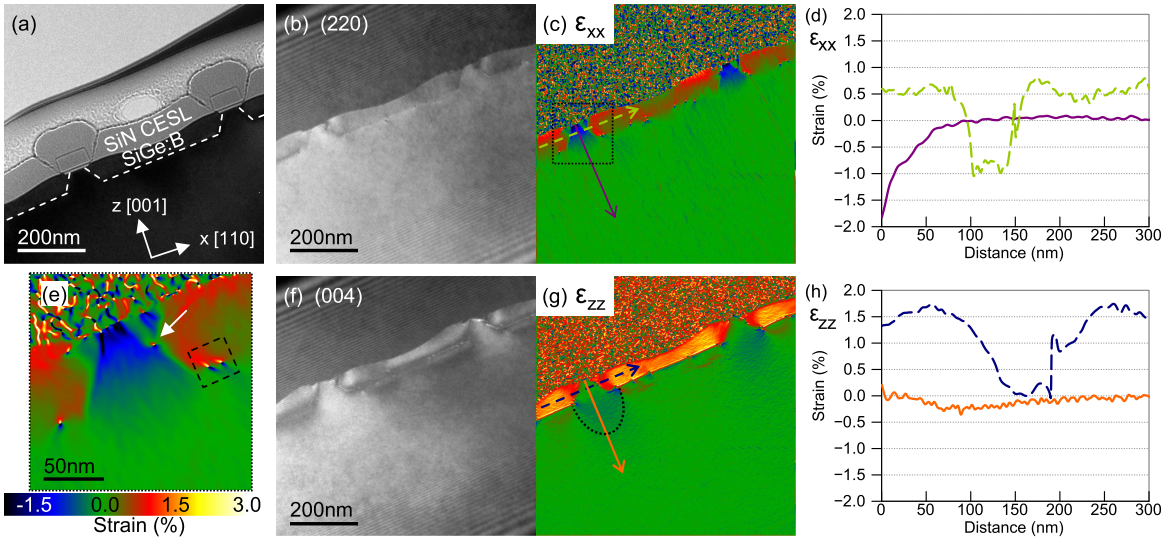

FIG. 3. (a) Lorentz image of dummy gates strained using recessed $Si_{0.65}Ge_{0.35}$: B sources and drains and a SiN CESL. (b) Dark-field (220) hologram and (c) reconstructed ε_{xx} strain map. (d) Strain profiles extracted from the maps according to the arrows. (e) Zoom of the ε_{xx} strain map in the region indicated by a dotted square in (c). (f) Dark-field (004) hologram, (g) ε_{zz} strain map, and (h) profiles extracted from the map. The profiles were averaged over 6 nm in the perpendicular direction. The profiles along the channel direction (dashed) were placed at 20 nm below the channel surface. Note that the measurements were performed on the same lamella but not exactly on the same devices for the two directions.

planes which are very common in Si and SiGe.[24,25] It can be noted that the step introduced by the dislocations at the SiGe/Si interface is clearly visible. Figure 4(d) is the ε_{xx} strain map reconstructed from (c) by geometrical phase analysis.[26] For comparison, the (220) spot was selected using a Gaussian mask of the same size used for the reconstruction of the hologram (the mask had a radius $3\sigma = 0.17\,\mathrm{nm}^{-1}$, was defined $\exp(-0.5(x-g)^2/\sigma^2)$ and was centered on g[27]). Despite the large difference in the size of the fringes between the two techniques, it is interesting to note that the reconstructed strain maps are fairly coherent. It confirms that DFEH can accurately map the strain field around such dislocations. Finally, we have noticed that the orientation of the dislocations is linked to the orientation of the closest inclined Si/SiGe interface. It is not always true but very often, the glide plane of the dislocations is the same as the plane defined by the closest (111) interface.

VI. SILICIDATION

Figures 5(a) and 5(b) compare two (220) dark-field electron holograms obtained before and after Ni-silicidation of a

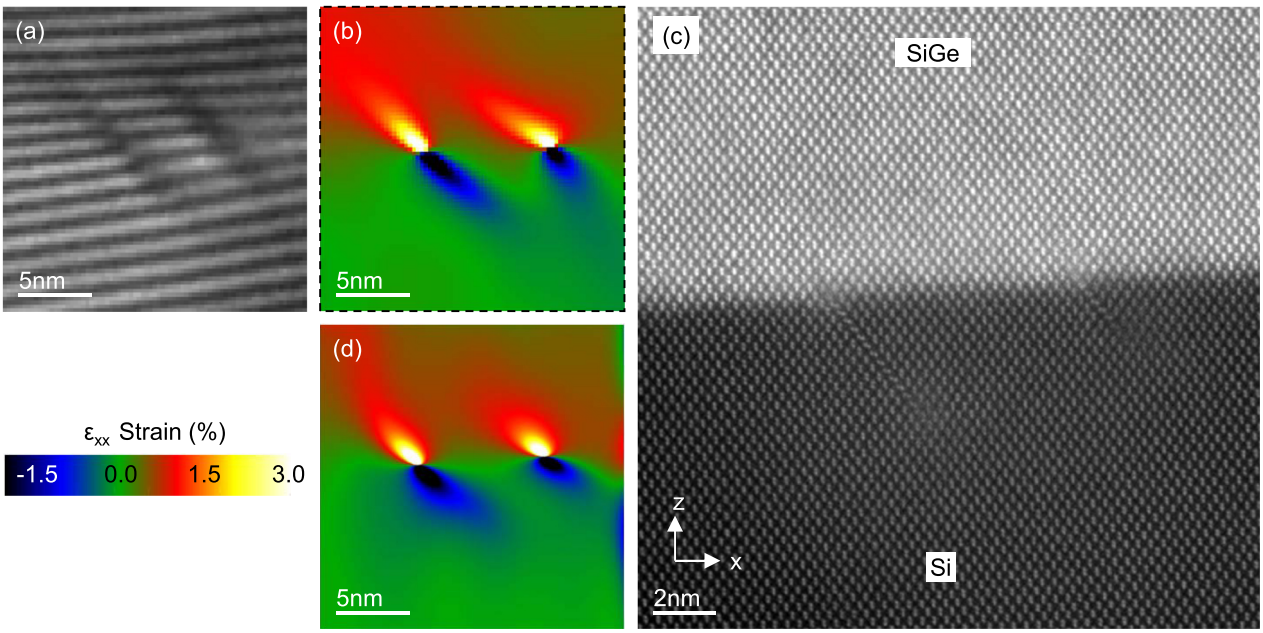

FIG. 4. (a) Zoom of the (220) dark-field electron hologram, in the region containing two dislocations, indicated by a dashed square in Fig. 3(e). (b) Zoom of the ε_{xx} strain map. (c) High resolution STEM-HAADF image of the same region. (d) ε_{xx} strain map reconstructed from (c) by geometrical phase analysis using a (220) spot. In both cases, (b) and (d), a Gaussian mask of radius $3\sigma = 0.17\,\mathrm{nm}^{-1}$ was used in Fourier space. A Hanning window was first applied on the high resolution image to minimize the artifacts of reconstruction at the boundaries of the image. The image was also cropped after reconstruction.

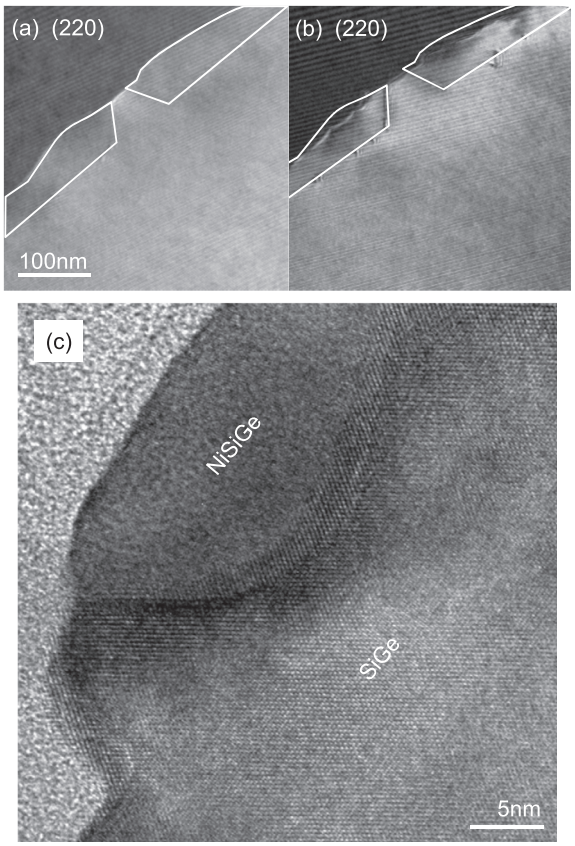

FIG. 5. (a) and (b) Dark-field (220) electron hologram (a) before and (b) after silicidation of the SiGe SD sample without CESL. (c) High resolution TEM image in the region of the germano-silicide layer.

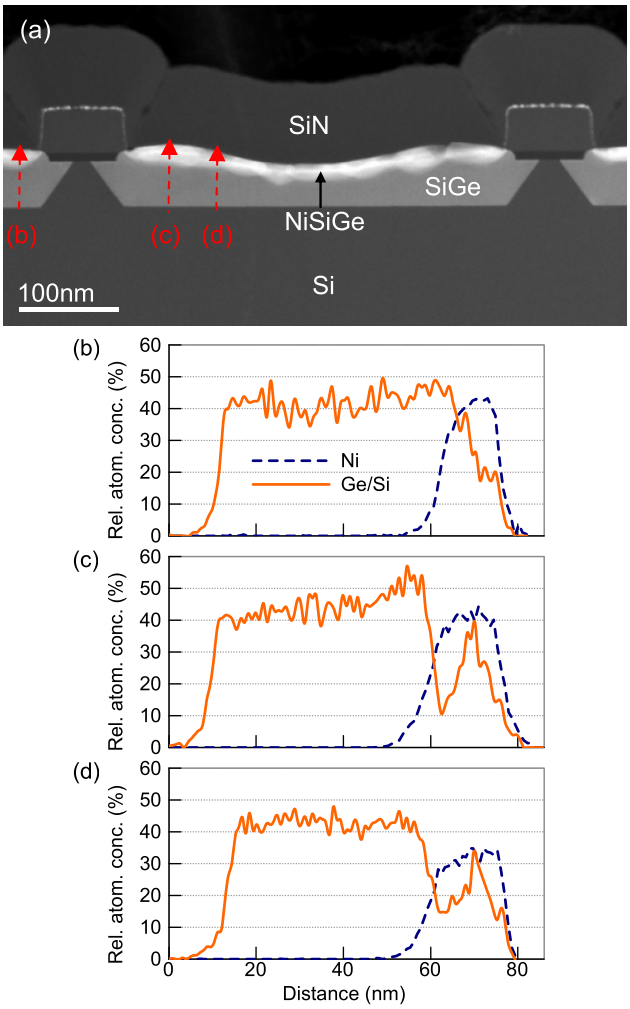

FIG. 6. (a) STEM-HAADF image of the sample strained using recessed SiGe SD and a SiN liner. (b)-(d) Relative atomic concentration profiles of Ni and Ge/Si ratio along the three dashed red arrows drawn in (a). For each graphic, 100 EDS spectra were acquired along the arrow. The relative atomic concentration of the element X is defined $[X]/([Ge]+[Si]+[Ni])$.

SiGe SD transistor without CESL. The outlines of the source and drain before silicidation (a) have been reported in (b). After silicidation, the contrast is less homogeneous. Moreover, it can be seen that the size of the diffracting area has decreased due to the absence of fringes at the top of the source and drain. Up to 20 nm of SiGe are not visible anymore as compared to (a) due to the formation of the germano-silicide layer. Figure 5(c) is a high resolution TEM image of the germano-silicide layer. It confirms that this region is no longer crystalline.

In a previous study,[28] it has been shown that the silicidation step decreases the strain in the channel, especially for high annealing temperatures. Other studies have reported an accumulation of Ge at the bottom the germano-silicide layer due to the preferential reaction of Ge with Si.[29] In this study, it was measured by NBED that this Ge accumulation leads to an increase of the strain in the transistor channel. To verify this, EDS was performed to analyze the variation of the Ge concentration in the sources and drains. Figure 6(a) shows a STEM-HAADF image of the silicided sample strained using both SiN liner and SiGe SD. The contrast is quite inhomogeneous in the germano-silicide layer along the source and drain which indicates some variations in the composition. Figures 6(b)–6(d) show the relative concentration profile of Ni and the Ge/Si ratio along the three dashed arrows drawn in (a). 100 EDS spectra were acquired along those arrows that go from the Si substrate to the SiN liner. For the three graphics, there is a decrease of the Ge/Si ratio at the bottom interface of the Ni rich region which is coherent with a preferential reaction between Ni and Si. In profile (b), the decrease of the Ge/Si ratio is continuous inside the Ni rich region. In profile (c), there is a decrease of the Ge concentration at the bottom interface but then an accumulation of Ge in the middle of the Ni rich region (at 70 nm). There is also a slight increase of Ge/Si ratio in the SiGe region below the Ni rich area (at 55 nm). For case (d), there is again an increase of the Ge concentration in the middle of the Ni rich region but no accumulation in the SiGe region. Therefore, the distribution of the germanium inside and around the germano-silicide layer is quite inhomogeneous and an increase of the channel strain due to Ge accumulation is not expected here.

Lorentz images, strain maps and strain profiles of the silicided SiGe SD sample are shown in Figs. 7(a)–7(d). Figures 7(e)–7(h) show the results corresponding to the silicided sample strained by both SiN CESL and SiGe SD. For both configurations, the strain distribution is less homogeneous than in the previous cases. Moreover some dislocations are found directly in the silicon regions, away from the

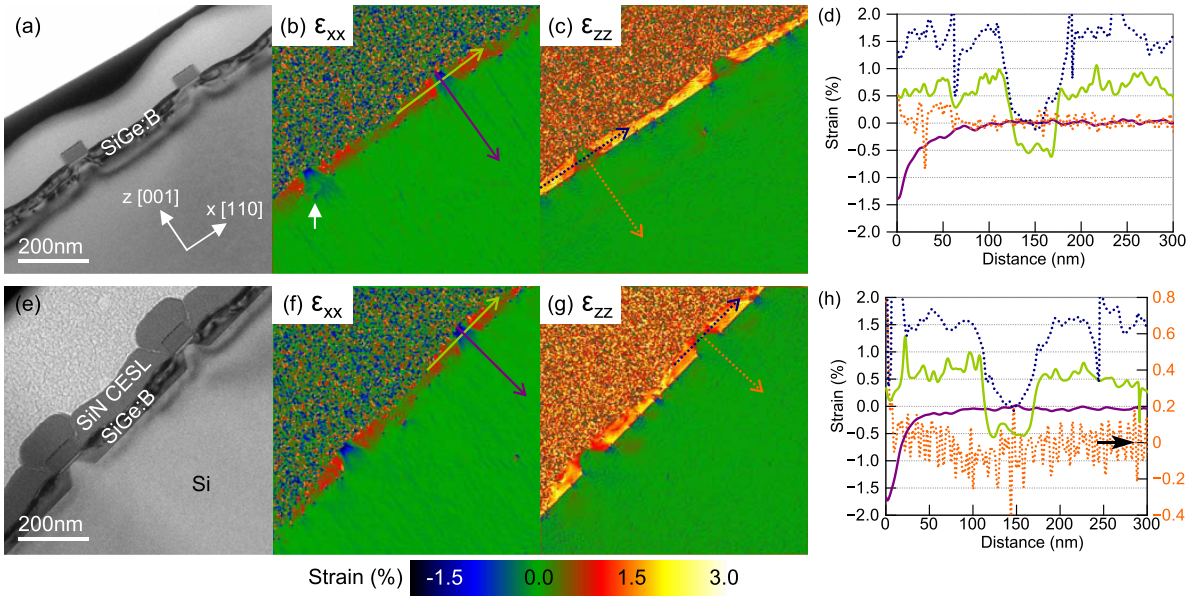

FIG. 7. (a) Lorentz image, (b) ε_{xx} strain map, (c) ε_{zz} strain map, and (d) strain profiles extracted from the maps for the silicided sample without CESL. (e)-(h) Image, strain maps, and strain profiles for the silicided sample with CESL. (h) For clarity, the ε_{zz} profile (dotted) along the z direction is linked to the right y-axis, as indicated by an arrow. The three other profiles are linked to the left y-axis.

interfaces (an example is pointed out by a white arrow in Fig. 7(b)). However, globally the strain levels in the channel and in the sources and drains are quite similar to what was observed previously without silicidation. For the configuration with CESL (e)–(h), the round shaped ε_{zz} strain is not as apparent as before. However, the dotted profile acquired along the z direction indicates a decrease of the strain to -0.1% at 100 nm. It is an argument that shows that the CESL still influences the strain in the transistor.

VII. COMPARISON

In order to compare the strain induced by the different configurations, the channel strain as a function of depth is reported in Fig. 8(a) for non-silicided and (b) silicided samples. For each case, 4 to 7 profiles are plotted, each one representing a different transistor in the lamella. The profiles were averaged over 15 nm in the [110] direction.

In the case of the SiN CESL configuration, the strain below the gates ranges from -0.3% to -0.4% depending on the device. This can be due to experimental noise as well as real variability of the strain from device to device. In the case of SiGe SD devices, the strain range is larger with values of -1.15% to -1.55%. This is partly linked to the distribution of the dislocations which varies from device to device. For the SiN and SiGe SD sample, the strain ranges from -1.65% to -1.95%. Despite this variation, the distribution of the profiles is quite clear. In all cases, the strain induced by the combination of CESL and SiGe SD is more important than for SiGe SD alone. For silicided samples (Fig. 8(b)), some profiles are significantly distant from the average. The silicidation process adds dispersion to the measurements. Globally, it appears that more strain is obtained when adding the SiN liner to the SiGe

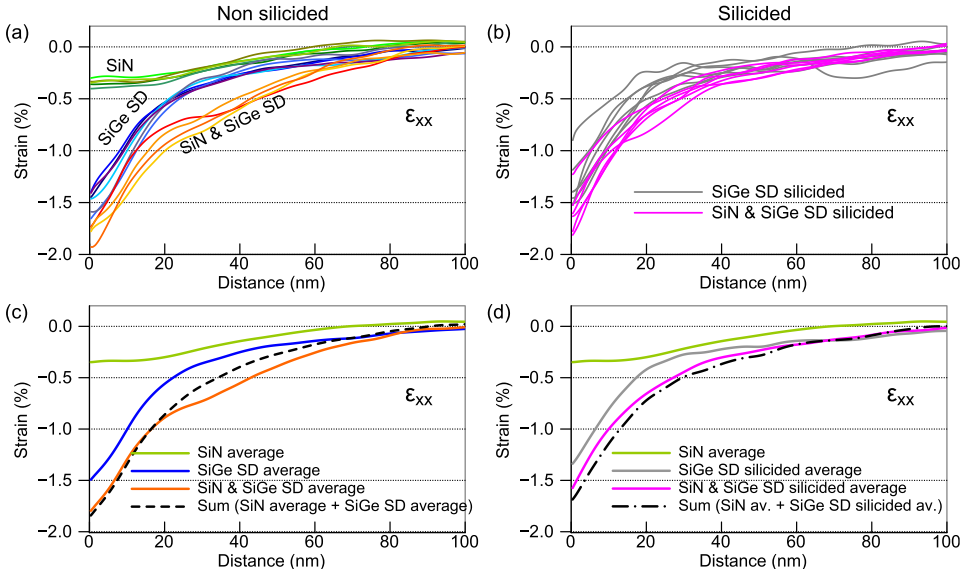

FIG. 8. Comparison of the ε_{xx} strain in the middle of the channel as a function of depth for the different configurations analyzed. Raw profiles measured on (a) non-silicided and (b) silicided devices. Profiles were averaged over 15 nm in the x direction. (c) and (d) Average of the profiles for the five different configurations. In both cases, non-silicided and silicided, the sum of the two individual cases (SiN CESL and SiGe SD) is plotted as a dashed or dotted line.

SD but the separation of the curves is less clear than for non-silicided samples.

Figure 8(c) shows the average of the different profiles for the three non-silicided configurations. In average, the strain induced by the SiN CESL alone is approximately constant down to a depth of 20 nm, then it decreases to zero at 70 nm depth. For both configurations with SiGe SD, the strain profile can be divided into two regions below and further than 20 nm where the strain variation is slower. The sum of the two individual cases is reported as a black dashed line for comparison with the combined configuration CESL and SiGe SD. Between 0 and 20 nm depth, the sum of the two independent configurations is close to the combined configuration. Between 20 and 80 nm, the combination leads to a larger value of strain than the sum of the individual components. The difference can be explained by the presence of dislocations placed at or close to the inclined (111) Si/SiGe interface in the combined configuration. As pointed out in Fig. 3(e), the compressive loop of the dislocations is orientated towards the substrate which gives a hint of compression at mid-depth of the trapezoidal shaped Si region.

After silicidation (d), the strain in the channel decreases of about 0.2% for both cases with and without CESL. The decrease is relatively small compared to what was measured previously (a decrease of 0.9%, (Ref. 15)). This is partly linked to the fact that the Ni layer deposited here was thinner (6 nm instead of 9 nm). After silicidation, the sum of the two individual cases fits quite well with the combined configuration from 0 to 100 nm depth. In the channel region, the difference between the combined curve and the sum of the individual cases is 0.1% which is quite small in the context of a TEM study. It can be a real difference or it can be an error due to the low statistics allowed by TEM as well as small differences of thickness between the thin foils combined with strain relaxation phenomena.

VIII. CONCLUSION

Spatially resolved strain mapping was performed on uniaxially strained devices using dark-field electron holography. The influence of compressive SiN CESL and SiGe sources/drains on the strain distribution was first analyzed and discussed individually for non-silicided samples. Then, the combination of the two techniques was tested to check for strain additivity. It was found that in the channel region, the compression induced by the combination of both processes corresponds to the sum of the individual components. The same investigation was then carried out with Ni-silicided devices. In spite of a slight reduction of the strain, it was observed that the strain additivity is approximately preserved. However, because the strain distribution is here influenced by the presence of dislocations, more investigations have to be performed on samples without defects. Note that in this study DFEH is particularly interesting since it provides both a large of field of view that allows to analyze two devices per image, and a nanometric spatial resolution that allows to map the strain field around dislocations. Finally, this study has also to face with the limits of TEM in terms of statistics. The analysis being limited to the number of transistors available on the thin foil, which is typically a few, it adds some uncertainty when dispersion is observed between measurements.

ACKNOWLEDGMENTS

This work has been funded by the Recherche Technologique de Base programme (RTB). It has been performed within the MINATEC's Nanocharacterization Center (PFNC). The CESL deposition process was developed by Laurent Vandroux. The Ni(Pt) deposition was developed by Stéphane Minoret and the silicidation process by Véronique Carron. We thank Jean-Michel Pedini for following the process flow. Armand Béché and Eric Robin are acknowledged for their help concerning the acquisition and the treatment of the EDX spectra.

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