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***Abstract* — We present recent advances made towards the realization of hole and electron spin quantum bits (qubits) localized within Si Quantum Dots (QDs). These devices, operated at cryogenic temperatures, can be defined by slightly modifying an SOI NanoWire FET fabrication flow, and are thus particularly relevant in the perspective of large-scale co-integration of qubits and their cryogenic control electronics.**

I. INTRODUCTION

By leveraging the phenomena of quantum superposition and entanglement, some specifically designed quantum algorithms [1] can achieve polynomial to exponential speed up when compared to their best classical counterparts, thus holding great promise for a variety of applications such as secure data exchange, database search, machine learning, and simulation of quantum processes. Quantum computers are envisioned as hybrid devices [2] where quantum cores operate in conjunction with classical circuitry, part of which is dedicated to programming, control and post-processing functions. While the engineering challenges span across various fields such as physics, electronics, computer science and computer engineering [3], we focus in the following on the matter of integrating qubits with long coherence times and high-fidelity operations. A common graphical representation of a qubit state space, the Bloch sphere, is shown Fig.1.

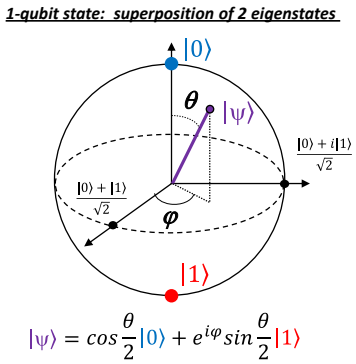

Fig. 1. Bloch sphere representation of the quantum state space. A qubit state can be described by a linear combination of eigenstates, *e.g.* "spin-up" and "spin-down".

Whereas a classical bit could only be represented by a vector pointing to either the North or the South Pole, a qubit may exist in a superposition of $|0\rangle$ and $|1\rangle$ and thus point to anywhere on the unit sphere. Furthermore, a state of N entangled qubits is expressed as a superposition of all N-tuples of the two basis-states, and is hence characterized by 2^N complex coefficients corresponding to their normalized probabilities.

The first of DiVincenzo's criteria [4] for a physical implementation of a quantum computer is the ability to define such two-level quantum-mechanical systems, and several candidates have emerged in the past decades. Roughly speaking, they can be divided into two main types. On one hand, systems in which the information is stored in the internal degree of freedom of the atom. Since those can be very well isolated, they tend to feature long relaxation and decoherence times, but are rather difficult to manipulate beyond the MHz. Furthermore, another issue is the difficulty of experimentally demonstrating their scalability. On the other hand, solid-state qubits which can be controlled electrically are generally thought to be more scalable and their manipulation can be performed at the GHz timescale, though it comes at the cost of shorter decoherence times. Among the latter, superconducting qubits have been historically leading the race in the implementation of quantum logic. These are however macroscopic objects and as such prone to coupling to probes and environment. Spin qubits, in which the quantum information is encoded in the spin degree of freedom of one [5] or several [6],[7] charged particles, offer a good compromise as they are microscopic objects and thus in principle more protected from external excitations.

II. SI-BASED SPIN QUBITS

Silicon spin qubits in particular have recently emerged as a promising option, first due to the recent observation of long coherence times and high fidelity [8]-[10], and second thanks to their compatibility with state-of-the-art technologies perfected over several decades by the IC manufacturing industry.

Regarding the first point, the latest notable achievements are the demonstration of single qubit Gates with >99% fidelity [10],[11], and the implementation of quantum algorithms on a two-qubit processor [12]. Fig. 2 shows the evolution of a figure of merit sometimes called "Q-factor" for experimental realizations in the relatively recent area of Si spin qubits. This quantity is related to how many operations can be performed

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on the qubit (*e.g.* a π rotation of the spin) before an error occurs (*e.g.* spin dephasing). One factor limiting the coherence of spin qubits is the possible interaction with nuclear spins in the host crystal. An advantage of Si versus other semiconductors (in particular III-V) is that ^{29}Si, its only stable isotope with non-zero nuclear spin, has a naturally low abundance (~4.7%). Yet notably, most of the best performing qubits on Fig.2 were fabricated on isotopically pure ^{28}Si.

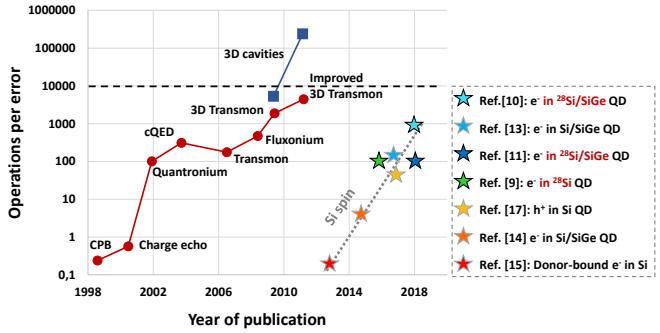

Fig. 2. Figure adapted from [16], showing the number of operations per error for various implementations of superconducting qubits vs. publication year. The added star symbols represent recent demonstrations of Si spin qubits. The figure of merit was estimated as the dephasing time T_2* divided by the time needed to induce a π-rotation of the spin (cf. angle θ on the Bloch sphere Fig.1).

The second point represents a key asset in the perspective of defining a very large number of identical objects, as well as for seamlessly co-integrating qubits with the classical electronics aimed at controlling and measuring them. In this context, single hole and electron spin qubits were recently implemented [17]-[19] on devices extremely similar to nanowire transistors realized on an SOI CMOS technology platform.

A popular way of isolating charges starts with forming a junction between two semiconductors of different bandgaps, such as Si and SiGe, hence forming a 2-Dimensional Electron Gas (2DEG) at the interface. Lateral confinement is then obtained by using several depletion Gates to tailor the potential into a Quantum Dot. The main advantages of this approach are the high quality of the confinement interface and a high degree of tunability. However, using many Gates for defining a single QD may get in the way of scaling up.

A more compact approach consists in using accumulation field-effect Gates to define the confinement potential under *e.g.* a Si/SiO_2 interface. Lateral definition can be assisted by patterning the Si active area (mesa or Shallow Trench Isolation). Carrier reservoirs are more or less remotely formed by ion implantation and coupled to the QDs. In [17]-[18], the fabrication only differs from a standard CMOS process flow by the deposition of larger SiN spacers with respect to the case of classical devices (typically 30nm vs. ~10nm). They are designed to protect the intrinsic Si film from self-aligned ion implantation, thus preserving the tunnel barriers coupling adjacent QDs and separating them from the leads. It is then straightforward to duplicate this structure with dense Gate pitch (≤ 80nm) along a silicon mesa to achieve a linear array of quantum dots [20], as shown on Fig. 3 (a).

Applying a Gate potential on a standard FET biased at large V_{DS} and operating at 300K induces a continuous flow of carriers from Source to Drain (Fig. 3 (b)). At very low temperatures (typically ~1K and below), adjusting the gate voltage allows controlling the number of charges confined in the QD (Coulomb blockade), hence enabling in principle to isolate a single electron or a single hole between the tunnel junctions (Fig. 3 (c)).

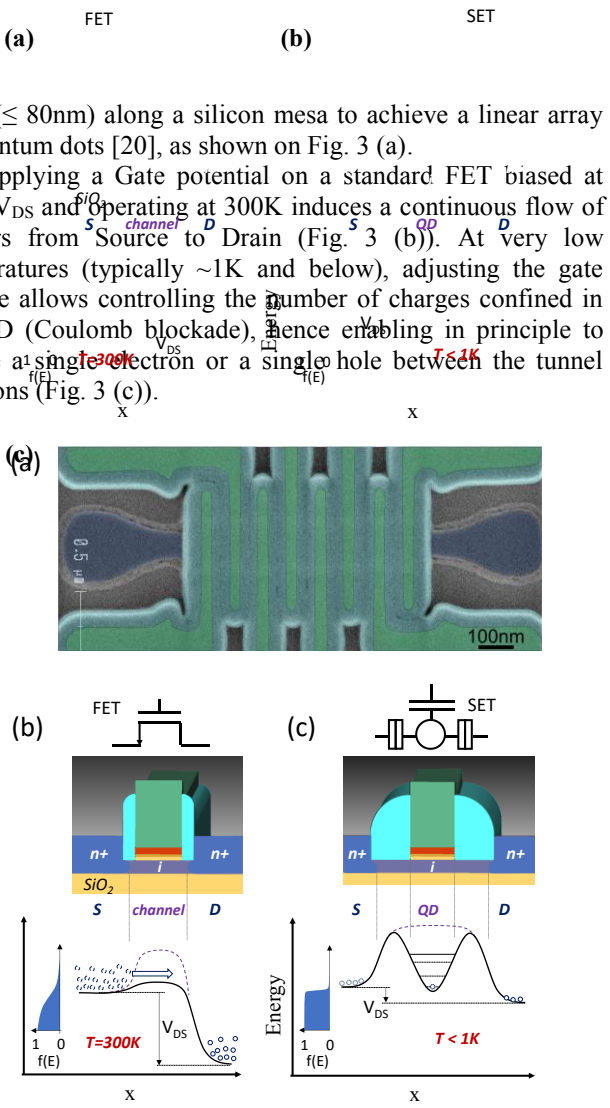

Fig. 3. (a) Scanning Electron Microscope (SEM) image of multiple quantum dots duplicated in series along a silicon nanowire. Schematic representations and energy profiles along (b) the channel of a silicon on insulator (SOI) FET operated at room temperature and (c) a Single Electron Transistor (SET) at cryogenic temperature.

The degeneracy between the spin states (spin-down $|\downarrow\rangle$ or spin-up $|\uparrow\rangle$) can then be lifted by applying a static magnetic field B, and the isolated particle can be used to encode a qubit. The separation (Zeeman) energy is $E_Z=|g|.\mu_B.B$, where g is a dimensionless quantity related to the gyromagnetic ratio of the particle, and μ_B is the Bohr magneton. Assuming a cryostat temperature on the order of ~100mK, the energy difference that can be resolved is of the order of 10μeV (implying B ~ 0.1T). Spin transitions may occur if an electromagnetic excitation of energy h.ν matching E_Z is provided to the system. Considering the above, it follows that the frequency of the control signal is typically a few GHz.

III. ELECTRICAL CONTROL OF THE QUBIT

A. *ESR and EDSR*

A first way of driving coherent rotation of a spin is through Electron Spin Resonance, or ESR (Fig. 4). Experimentally, one can deposit in close proximity of the device a microstrip line that is used to flow a large AC current

and generate an oscillating magnetic field resonant with the spin transition frequency [8],[9]. Coupling the spin to an RF magnetic field seems like the most straightforward method, although the excitation is hardly applied locally. This can be a drawback for maximizing the manipulation speed, which depends on the coupling strength.

A second mechanism is the Electric Dipole Spin Resonance (EDSR). In this case, the spin rotation is induced by an oscillating electric field, which can be provided by a field-effect Gate placed directly above the QD. If the properties of the system are such that Spin-Orbit Coupling (SOC) is significant, the orbital motion caused by an RF E-Field alone can drive spin rotations. Otherwise, a possible approach consists in embedding a micro-magnet as an auxiliary in the vicinity of the device, causing the particle traveling back and forth to perceive an oscillating B-field [10]-[14],[21]. Although efficient for fast manipulation of a few qubits, this technique may become problematic for the design and integration of large-scale qubit arrays.

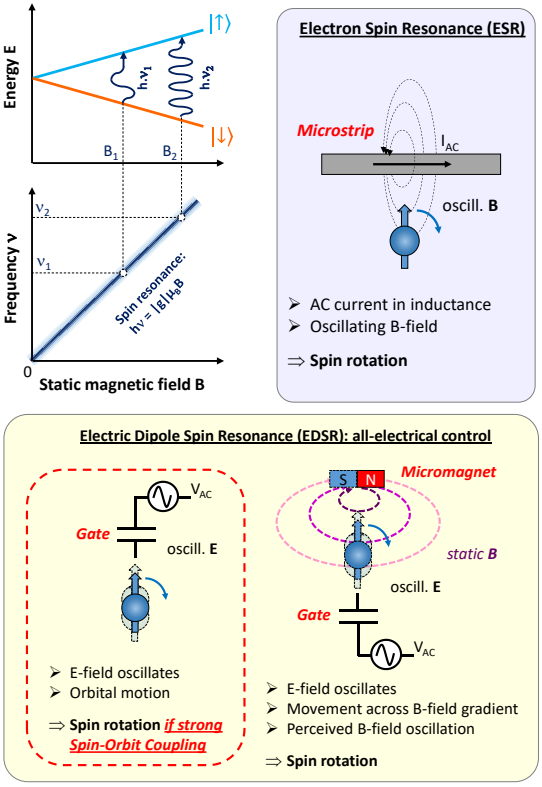

Fig. 4. (Top left) Principle of Zeeman splitting between $|\downarrow\rangle$ and $|\uparrow\rangle$, resonant transitions and spin resonance signature. (Top right) B-field-mediated ESR. (Bottom) E-field-mediated EDSR, either relying on intrinsic Spin-Orbit Coupling (SOC), or using a micro-magnet as an auxiliary.

B. *Hole spin qubits*

Luckily, SOC is relatively strong for holes in silicon and allows for more straightforward EDSR manipulations [22]. Typical results [17],[18] are presented on Fig. 5. The device is essentially a two-Gate pFET with wide spacers covering the inter-Gate separation and protecting it from self-aligned doping. Gate 1 defines the target qubit, Gate 2 is used to localize a particle with a spin initialized to a reference state, acting as a filter. Following Pauli's Spin Blockade (PSB), a charge confined under Gate 1 may only travel to the Drain via the QD under Gate 2 if the spins in each QD are antiparallel. A control burst is applied on Gate 1 at the resonant frequency of the target qubit. As the burst duration is varied, the probability of flipping the hole spin confined in the QD oscillates (Fig. 5(b) and (c)), with observed Rabi frequency up to 80 MHz (T_π= 6.25ns). A Ramsey pulse sequence (Fig. 5 (d)) leads to extracting a dephasing time T_2^* of 270 ns, hence a Q-factor of 43. Charge noise is believed to be the dominant factor limiting decoherence in this case, pointing to a trade-off between manipulation speed and longevity.

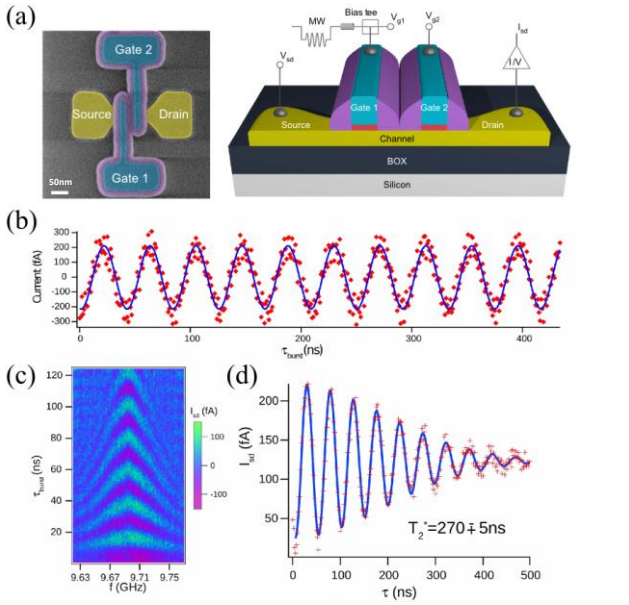

Fig. 5. (a) Top view Scanning Electron Microscope (SEM) image of the device, and schematics showing the connection to the experimental setup. (b) Rabi oscillations for a single hole spin (base temperature T=10mK). (c) Typical chevron pattern obtained when varying the excitation burst frequency and duration. (d) Dephasing measurement using Ramsey pulse sequence varying the free evolution time τ.

C. *Electron spin qubits*

In contrast with holes, the SOC is intrinsically quite weak for electrons in silicon. As a result, Si electron spin qubits were so far manipulated either by resorting to integrating ESR microstrips or magnets.

It was recently demonstrated experimentally that a slight difference in g-factors between two Si QDs with tunable exchange could be leveraged to drive resonant oscillations (f_{Rabi} ~ 0.2MHz) between the $|\uparrow\downarrow\rangle$ and $|\downarrow\uparrow\rangle$ states of a two-electron system using all-electrical control pulses [23].

In single-electron systems, it was shown that thanks to a combination of the multi-valley structure of silicon together with some specific device geometries resulting in broken

symmetries of the electron wavefunction, non-negligible coupling terms of inter-valley SOC could emerge [24]. In fact, devices with Gates wrapping over mesa-defined Si NanoWires lead to a "corner dot" confinement [25] (Fig. 6), and therefore fall into this category. When the valley splitting between low-lying v_1 and v_2 is close to the Zeeman splitting E_Z, mixing between the coupled $|v_1, \uparrow\rangle$ and $|v_2, \downarrow\rangle$ states occurs, giving access to spin control via inter-valley transitions. This mechanism enabled the first experimental measurement of E-field electron spin manipulation in silicon without micro-magnet [19].

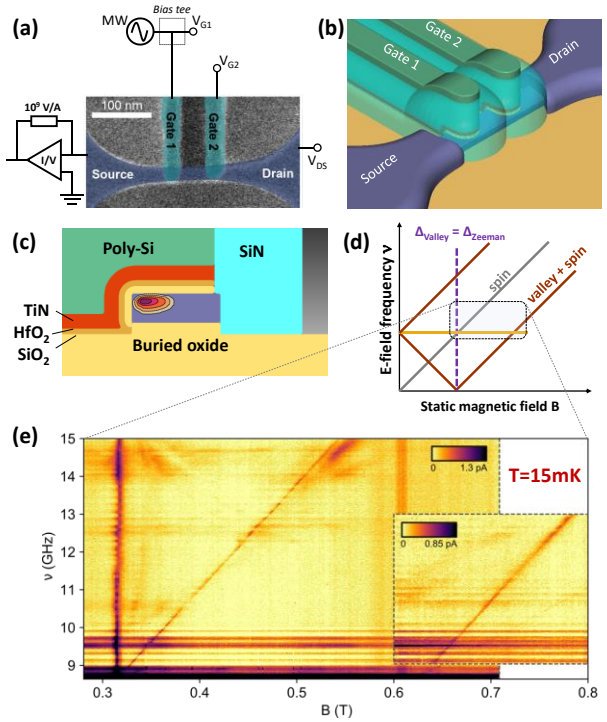

Fig. 6. (a) SEM image after gate patterning and measurement setup description. (b) Schematic view of the partially wrapping gates. (c) Cross-section along a gate showing the location of the asymmetrical electron wavefunction in the corner of the nanowire. (d) Diagram of the expected EDSR transition as a function of magnetic field, taking into account the inter-valley SOC. (e) EDSR signal measurement (T=15mK), showing spin transitions as a function of magnetic field and microwave frequency.

Furthermore, the fact that these devices are fabricated on SOI substrates offer the possibility of using the back-Gate in order to tune the valley splitting via vertical (de-)confinement. At fixed Zeeman energy, this implies the ability to travel adiabatically between two regimes for which the low-lying states are either $|v_1, \downarrow\rangle$ and $|v_1, \uparrow\rangle$ (spin qubit), or $|v_1, \downarrow\rangle$ and $|v_2, \downarrow\rangle$ (valley qubit), using only V_{BG} [26],[27]. The first one is stable but hardly addressable, the second one has a short coherence time but enables fast E-field manipulation. This scheme may hence be helpful towards optimizing the Q-factor trade-off.

IV. Tunable Coupling and Readout

While easy to implement and useful for proof-of-concept qubit demonstrations, the transport-based spin readout technique discussed shown in the previous section presents significant limitations: 1) it does not allow single-shot readout, *i.e.* the ability to perform individual spin measurements; 2) it is not scalable. In this section, we discuss an alternative two-gate geometry for which both of these limitations could be overcome.

A. *Tunable coupling*

Fig. 6 having introduced "corner dot" confinement, for large enough channel widths and fully overlapping Gates, two pronounced potential minima develop at the upper nanowire corners leading to a pair of clearly distinct QDs. These QDs can be controlled independently by splitting the Gate over the NW, resulting in the so-called "face-to-face" geometry. Once again, the SOI back-Gate can be used to tune the position of the electron confinement potential. Experimental evidence of adjustable capacitive coupling between two corner dots using the back-Gate is provided in [20]. Fig. 7 below shows numerical calculations carried out for a split-gate device with comparable geometrical parameters, showing the tunability of inter-dot tunnel coupling by V_{bg}. This feature is essential for the realization of two-qubit Gates, but also in certain readout schemes.

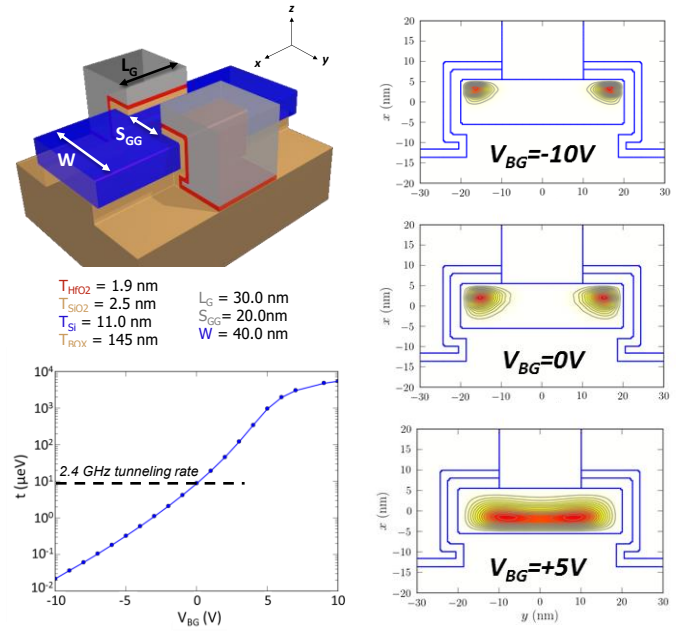

Fig. 7. (Top left) Structure and dimensions of the n-type face-to-face device with undoped channel. (Right) A two-band k.p model accounting for valley-orbit coupling was used to calculate single-electron states. The Configuration Interaction (CI) method was then used to calculate the two-electron states. The wave function squared of the corner states at V_{G1}=V_{G2}=0.2V, and respectively V_{BG}=-10V, 0V and +5V are shown. (Bottom left) Tunnel coupling t extracted versus V_{BG} from the anticrossing between the lowest single-electron states.

B. *Single-shot readout*

The DC transport-based Pauli Spin Blockade readout scheme shown in section III needs to be re-initialized and repeated as fast and for as many times as it takes to obtain a measurable current. This, of course, is quite incompatible with both the notion of large-scale computing and any expected "quantum speedup". Provided that it is mapped to a spin event, a single charge event should be sensed practically as it occurs, and if possible without losing the particle carrying the quantum information.

Coupling the QD to a charge detector, *e.g.* a Single Electron Transistor (SET) or Quantum Point Contact (QPC) device enables to indirectly monitor spin-dependent transport by choosing an appropriate read point and monitoring the time-evolution of the channel impedance (Fig. 8). This was done by I_{SET} current measurement in [28], enabling to extract spin relaxation times in a corner dot of a "face-to-face" device. Notably, the ability to tune the cross-capacitance C_{CROSS} by using the SOI back-Gate can lead to improving the measurement speed/fidelity trade-off.

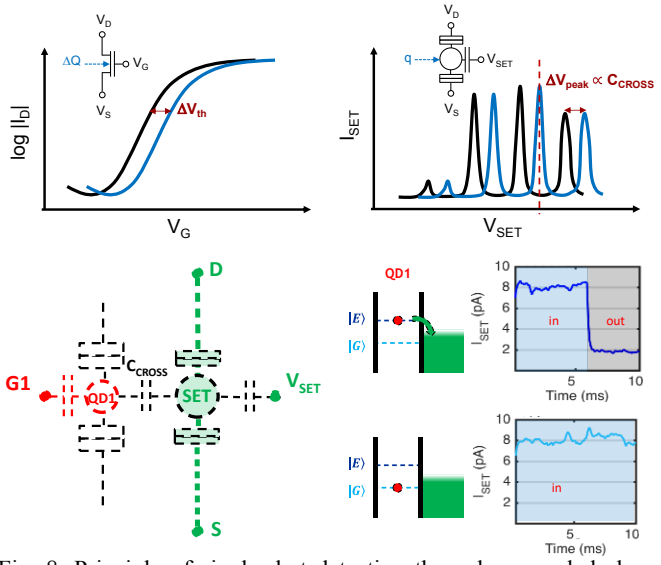

Fig. 8. Principle of single-shot detection through a coupled charge detector. (Top) In the same way that a charge coupled to the channel would shift the transfer characteristics of a MOSFET by ΔV_{th}, a single charge event occurring near an SET causes a shift of the Coulomb peaks proportional to the cross-capacitance C_{CROSS}. (Bottom left) Charge detector coupled to a Quantum Dot. The spin-charge conversion mechanism is energy-selective readout [29], *i.e.* charge movement may occur for the excited spin state $|E\rangle$, but not for the ground state $|G\rangle$. Observing the current trace through the SET detector determines the spin state of the qubit in QD1.

Alternatively, the impedance shift can be observed by RF reflectometry. In principle, it consists in connecting an LC tank circuit to the impedance to be probed, and analyzing the amplitude and/or phase of the reflected signal. The LC resonator may be connected directly to the dot-defining Gate [30]-[32]. In the face-to-face geometry, this technique can be used to sense the spin-dependent quantum capacitance between the two coupled corner QDs. One can then imagine having the actual qubit on one side, and on the other side a "helper dot" initialized in the reference spin state, connected to the reflectometry setup for parallelism measurements (Fig. 9). Since coupling to the reservoirs near each QD is no longer necessary, this elementary tile can be extended into a linear array of QDs [20],[33].

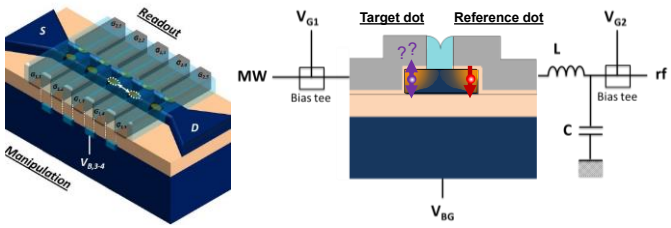

Fig. 9. Principle of the RF Gate reflectometry measurement setup applied to a face-to-face device, enabling scalable, fast single-shot readout of the spin qubit state under G1. Operations are performed on the target dot while the reference dot is kept in its initial known state. Owing to PSB, tunnel coupling between the (1,1) and (0,2) charge states and the measurement of the associated quantum capacitance is only possible if the two-electron system is in the singlet configuration. Thus, information on the target spin can be sensed by reflectometry.

V. Conclusion and Perspectives

Among all possible implementations of quantum bits, spins in Si offer an interesting trade-off between fast manipulation and stability. Within this rapidly growing field, each existing embodiment of the elementary building block comes with its own balancing of some qualities which are all desirable for a scalable quantum computer; *i.e.* fidelity, tunability, compactness, addressability, and compatibility with classical control electronics. We shed light on SOI devices which were obtained by a relatively straightforward adaptation of a NanoWire FET process flow. Their characteristics and geometry allow investigating various manipulation and readout schemes for electron and hole spin qubits, some of which enabled or enhanced by the additional lever that is the back-Gate. In the context of cryo-CMOS for control electronics [34], this technology platform also displays a strong potential stemming from the back-biasing functionality. Power dissipation close to the qubits being a major challenge, it puts high performance, low V_{DD} operation back within reach despite the conjunction of steepening subthreshold slope and rising threshold voltages at low temperature [35]. Building from this starting ground, future efforts may be directed towards developing architectures with increased connectivity, compatible with the implementation of Quantum Error Correction (QEC) codes for large-scale fault-tolerant computing.

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REFERENCES

[1] http://math.nist.gov/quantum/zoo/

[2] R. Van Meter, C. Horsman, "A Blueprint For Building a Quantum Computer", *Communications of the ACM*, 56, 10, 2013.

[3] C. G. Almudever *et al.*, "The engineering challenges in quantum computing", *IEEE Design, Automation & Test in Europe Conference & Exhbition (DATE)*, 2017.

[4] D. P. DiVincenzo, "The Physical Implementation of Quantum Computation", *arXiv:quant-ph/0002077*, 2000.

[5] D. Loss, D. P. DiVincenzo, "Quantum computation with quantum dots", *Phys. Rev. A*, 57, 120, 1998.

[6] D. P. DiVincenzo *et al.*, "Universal quantum computation with the exchange interaction", *Nature*, 408, 339-342, 2000.

[7] J. Levy, "Universal Quantum Computation with Spin-1/2 Pairs and Heisenberg Exchange", *Phys. Rev. Lett.*, 89, 147902, 2002.

[8] M. Veldhorst *et al.*, "An addressable quantum dot qubit with fault-tolerant control-fidelity," *Nat. Nanotechnol.*, 9, 981-985, 2014.

[9] M. Veldhorst *et al.*, "A two-qubit logic gate in silicon," *Nature*, 526, 410-414, 2015.

[10] J. Yoneda *et al.*, "A quantum-dot spin qubit with coherence limited by charge noise and fidelity higher than 99.9%", *Nat. Nanotechnol.*, 13, 102-106, 2018.

[11] D. M. Zajac *et al.*, "Resonantly driven CNOT gate for electron spins", *Science*, 359, 439-442, 2018.

[12] T. F. Watson *et al.*, "A programmable two-qubit quantum processor in silicon", *Nature*, 555, 633-637, 2018.

[13] K. Takeda *et al.*, "A fault-tolerant addressable spin qubit in a natural silicon quantum dot", *Science Advances*, 2, 8, 2016.

[14] E. Kawakami *et al.*, "Electrical control of a long-lived spin qubit in a Si/SiGe quantum dot," *Nat. Nanotechnology*, vol. 9, pp. 666-670, 2014.

[15] J. J. Pla *et al.*, "A single-atom electron spin qubit in silicon", *Nature*, 489, 2012.

[16] M. H. Devoret, R. J. Schoelkopf, "Superconducting Circuits for Quantum Information: An Outlook", *Science*, 339, 6124, 2013.

[17] R. Maurand *et al.*, "A CMOS silicon spin qubit," *Nature Commun.,* vol. 7, 13575, 2016.

[18] L. Hutin *et al.*, "Si CMOS platform for quantum information processing," *IEEE Symposium on VLSI Technology*, 2016.

[19] A. Corna *et al.*, "Electrically driven electron spin resonance mediated by spin-valley-orbit coupling in a silicon quantum dot," *npj Quantum Information*, vol. 4, 6, 2018.

[20] S. De Franceschi *et al.*, "SOI technology for quantum information processing," *IEEE International Electron Devices Meeting (IEDM)*, 2016.

[21] M. Pioro-Ladrière *et al.*, "Electrically driven single-electron spin resonance in a slanting Zeeman field," *Nat. Phys.*, vol. 4, 10, pp. 776-779, 2008.

[22] A. Crippa *et al.*, "Electrical spin driving by g-matrix modulation in spin-orbit qubits," *Phys. Rev. Lett.*, 120, 137702, 2018.

[23] P. Harvey-Collard *et al.*, "All-electrical universal control of a double quantum dot qubit in silicon MOS", *IEEE International Electron Devices Meeting (IEDM)*, 2017.

[24] W. Huang *et al.*, "Electrically driven spin qubit based on valley mixing", *Phys. Rev. B*, 95, 075403, 2017.

[25] B. Voisin *et al.*, "Few-Electron Edge-State Quantum Dots in a Silicon Nanowire Field-Effect Transistor", *Nano Lett.*, 14, 4, 2014.

[26] L. Bourdet, Y.-M. Niquet, "All-electrical manipulation of silicon spin qubits with tunable spin-valley mixing", *Phys. Rev. B*, 97, 155433, 2018.

[27] L. Hutin *et al.*, "All-electrical control of a hybrid electron spin/valley quantum bit in SOI CMOS technology", *IEEE Symposium on VLSI Technology*, 2018.

[28] M. Urdampilleta *et al.*, "Towards Quantum Computing in Si MOS Technology: Single-shot Readout of Spin states in a FDSOI Split-Gate Device with Built-in Charge Detector", *IEEE Symposium on VLSI Technology*, 2017.

[29] M. Elzerman *et al.*, "Single-shot read-out of an individual electron spin in a quantum dot", *Nature*, 430, 431-435, 2004.

[30] J. I. Colless *et al.*, "Dispersive Readout of a Few-Electron Double Quantum Dot with Fast rf Gate Sensors", *Phys. Rev. Lett.*, 110, 046805, 2013.

[31] A. C. Betz *et al.*, "Dispersively Detected Pauli Spin-Blockade in a Silicon Nanowire Field-Effect Transistor", *Nano Lett.*, 15, 7, 2015.

[32] A. Crippa *et al.*, "Level Spectrum and Charge Relaxation in a Silicon Double Quantum Dot Probed by Dual-Gate Reflectometry", *Nano Lett.*, 17, 2, 2017.

[33] C. Jones *et al.*, "A logical qubit in a linear array of semiconductor quantum dots", *arXiv:1608.06335v2*, 2017.

[34] E. Charbon *et al.*, "Cryo-CMOS Circuits and Systems for Scalable Quantum Computing", *IEEE International Solid-State Circuits Conference (ISSCC)*, 2017.

[35] H. Bohuslavskyi *et al.*, "28nm Fully-depleted SOI technology: Cryogenic control electronics for quantum computing", *IEEE Silicon Nanoelectronics Workshop*, 2017.