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Very High Sustainable Forward Current Densities on 4H-SiC P⁺N⁻ Junctions formed by localized VLS P⁺ epitaxy

S. Sejil^{1,2a*}, L. Lalouat^{1,2b}, M. Lazar^{2c}, D. Carole^{1d}, C. Brylinski^{1e},
F. Jomard^{3f}, D. Planson^{2g}, G. Ferro^{1h}, C. Raynaud²ⁱ,

¹Laboratoire des Multimatériaux et Interfaces, UMR 5615, Université de Lyon, LYON 1, CNRS,
69622 Villeurbanne, France

²AMPERE, INSA Lyon, Ecole Centrale de Lyon, CNRS, 69621 Villeurbanne, France

³GEMAC, Université Versailles-Saint-Quentin, CNRS, 78035 Versailles, France

^aselsabil.sejil@etu.univ-lyon1.fr, ^bloic.lalouat@ec-lyon.fr, ^cmihai.lazar@insa-lyon.fr,
^ddavy.carole@univ-lyon1.fr, ^echristian.brylinski@univ-lyon1.fr, ^ffrancois.jomard@uvsq.fr
^gdominique.planson@insa-lyon.fr, ^hgabriel.ferro@univ-lyon1.fr, ⁱchristophe.raynaud@insa-lyon.fr,

This study deals with electrical and structural characterization of p-n junctions fabricated on a 4° off-axis 4H-SiC with a N⁻ epilayers ($1 \times 10^{16} \text{ cm}^{-3}$), on which a P⁺⁺ epitaxial area was grown by Vapour-Liquid-Solid (VLS) transport [1], localized in etched wells with 1 μm depth. Previously, a High Temperature Annealing (HTA) process ($\sim 1700^\circ\text{C}$), following this localized doping technique, has led for the first time to high quality PN junction [2]. Moreover, this technique has provided p-type material with very low resistivity and led to ohmic contacts on it with specific contact resistance values as low as $1.3 \times 10^{-6} \Omega \cdot \text{cm}^2$ [3].

Further works have been focused on the optimization of the localization process and the VLS growth parameters. At first, the influence of the type of carrier gas (Ar or H₂) has been investigated in terms of quality of growth morphology, deposit thickness and electrical behavior of the obtained P/N junction [4]. A dramatic improvement has been obtained using H₂ as compared to Ar. Under H₂, an excellent and uniform step-bunching morphology was observed over the entire zones of deposition, but the thickness of the P⁺ SiC deposit was rather thin $\sim 50 \text{ nm}$. Moreover, the expected $\sim 3 \text{ V}$ threshold voltage of the p-n junction was measured in direct bias. This electrical behavior had never obtained before with such low temperature process (1100°C).

Recently [5], we have reported on the optimization of other VLS growth parameters like growth duration, propane flow rate (carbon precursor). Increasing the initial amount of silicon and aluminium have led to a dramatic increase of the thickness of VLS epilayers, reaching the range 200 - 900 nm depending on the width of the wells, without degradation of the crystalline quality (Figure 1). Implementing these new P-type VLS layers with an adequate technological process has allowed us to obtain 4H-SiC diodes withstanding spectacular high current densities in forward bias while preserving a low leakage current density in reverse bias. Hereafter are presented elements of the technological process and the I-V characteristics of these diodes which clearly present a bipolar behavior (light emission in forward bias).

At first, after VLS growth, we have checked the Al doping level by Secondary Ion Mass Spectrometry (SIMS) to make a correlation between electrical behavior and deposit thickness as a function of the diameters of the wells (Figure 2). Then, classical Ni-based ohmic contact, RTA annealed at 900°C , was implemented on the back face of the n-type substrate. Because of the high doping level of the VLS P⁺⁺ zone (confirmed by SIMS), it has been possible to get ohmic contacts on these VLS p-type layers by the sputtering deposition and patterning of a simple layer of Al metal (Figure 3) thick enough to get full coverage of the rather rough VLS layer surface.

corresponding author: selsabil.sejil@etu.univ-lyon1.fr

I-V current-voltage measurements on the PN junction formed this way have been performed and one example is presented on figure 4. The reverse leakage current density is quite low while very high current densities (several kA/cm^2) are sustainably obtained in forward bias, similar on a wide range of diode diameters the total current being limited to 1A in all cases due to instrumental limitations of the Keithley 2636 SMU unit.

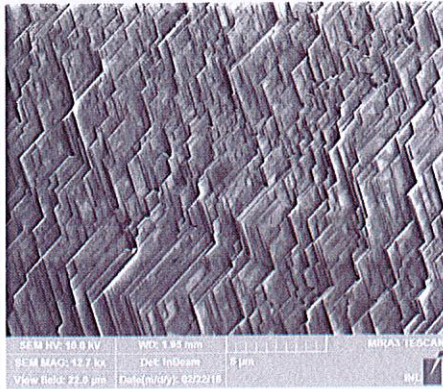


Figure 1: SEM image, surface morphology of a VLS thick layer

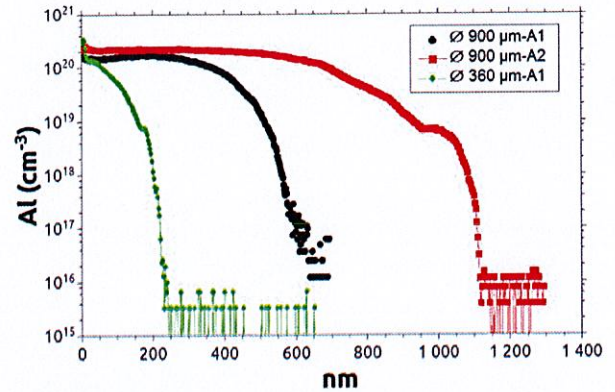


Figure 2: SIMS Al profiles on wells with variable \varnothing

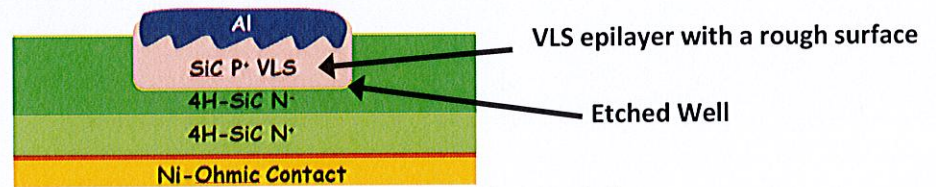


Figure 3: Schematic cross sectional view of the bipolar diode used for electrical tests

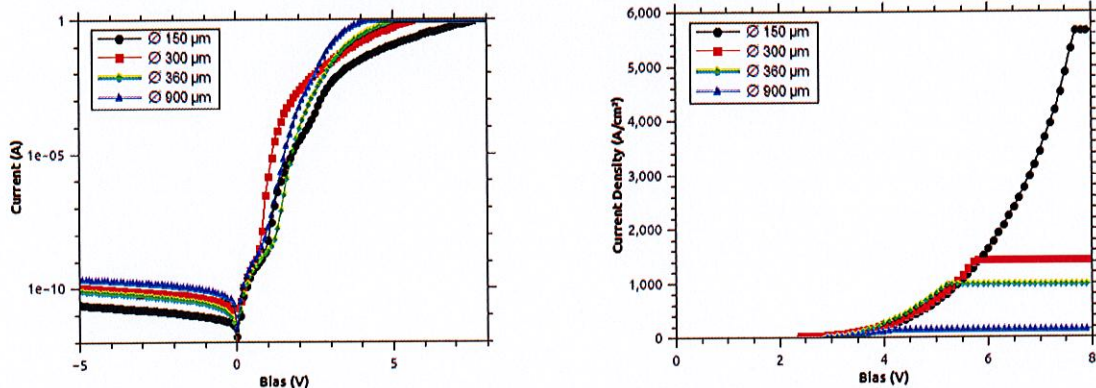


Figure 4: I-V measurements in semi logarithmic scale (in the left) and current densities in linear scale (in the right) for PN diodes with various diameters VLS wells

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