

# Vertical termination filled with adequate dielectric for SiC devices in HVDC applications

T.T.H. Nguyen-Bui\*, M. Lazar, J.-L. Augé, H. Morel, L.V. Phung, D. Planson  
Université de Lyon, CNRS, Laboratoire Ampère, INSA-Lyon, Université Claude Bernard Lyon 1,  
UMR 5005, F-69621, France  
\*thi-thanh-huyen.bui@insa-lyon.fr

To fully achieve the performance which SiC power devices potentially have, it is necessary to reduce the electric field crowding effect taking place at the junction edges. So far, numerous techniques have been adapted to improve the breakdown voltage mainly under the planar technology, using for example, guard ring [1], field plate (FP) [2], semi-insulating polycrystalline (SIPOS) [3], junction termination extension (JTE) [4], 3D RESURF [5,6]... However for high voltage devices, these techniques have the drawback of consuming large areas. Recently, thanks to the advancement in the Micro Electro Mechanical Systems (MEMS) process technology, the deep trench termination (DT2) technique becomes an appropriate choice for future high voltage power device. The edge termination design used for improving the breakdown voltage ( $V_{BR}$ ) and reducing drastically the chip area comparing to the above conventional structures. This concept has been already demonstrated in Si technology [7].

In this work, the DT2 used for a 3kV 4H-SiC bipolar diode is presented. The structure of the diode has been studied and optimized by finite elements electrical simulations using TCAD SENTAURUS software [8]. The vertical diode structure is composed by a top  $1\mu\text{m}$ ,  $1.10^{18}\text{ cm}^{-3}$   $\text{P}^+$  epilayer on a lower doped ( $8.10^{14}\text{ cm}^{-3}$ ) and  $18\mu\text{m}$  thick  $\text{N}^-$  epilayer and a  $\text{N}^+$  substrate. The ideal breakdown voltage for one dimensional PiN diode structure with an i-layer thickness of  $18\mu\text{m}$  is 3354V. A deep trench is created in the epilayers and filled with an insulated material, as  $\text{SiO}_2$  or BCB (Benzocyclobutene), to realize the junction termination. A field plate is needed to draw out the electrostatic potential in the trench (Figure 1). Our simulation results show that it is possible with this type of trench to protect effectively up to 98% of the ideal  $V_{BR}$ . Even if this efficiency is obtained with JTE protection, DT2 method has advantages in the technical realization (i.e. avoiding the use of ion implantation needed for JTE fabrication) and in the decrease of the chip area.

In order to validate the DT2 method for 4H-SiC vertical power devices, some experiments were done to create the trench on the 4H-SiC material by ICP (Inductively Coupled Plasma) and RIE (Reactive Ion Etching) techniques.  $\text{SF}_6$  and  $\text{SF}_6/\text{O}_2$  plasma chemistries have been used, protecting the unetched surface with a hard Ni-based mask [9]. The obtained results show that more than  $20\mu\text{m}$  of depth trench could be obtained (Figure 2). The process duration is reasonable. A etching rate of  $\sim 0.2\mu\text{m}/\text{min}$  has been used in order to obtain smooth wells and to avoid doing asymmetric micro-trenching (an increasing of the etching rate near the corners compared to the center of the trench) [10].

Figure 3 shows a clear relationship between the trench depth and width on the  $V_{BR}$ . There is no field plate. The insulating material in the trench is  $\text{SiO}_2$ . These curves point out that even shallow trenches can reduce the termination length. Moreover, it is found that the trench width for each trench depth has no influence on the  $V_{BR}$  above a threshold value. It exists an optimum value of the width of the trench for each depth. For each width of the trench, the  $V_{BR}$  increases significantly with the trench depth.

Dielectric constant ( $\epsilon_r$ ) of trench filler material significantly affects also the  $V_{BR}$  (Figure 4). The maximum value increases from 2335V (70% efficiency) up to 2830V (85% efficiency) by using BCB ( $\epsilon_r=2.65$ ) instead the  $\text{SiO}_2$  ( $\epsilon_r=3.9$ ). In order to increase the  $V_{BR}$ , the field plate can be added. The simulation results show thus a 98% efficiency of the DT2 protection is obtained.

In multi-material devices, thermal variations induce a mechanical stress. Thus it is possible that fixed charges appear at the interfaces. For the couple SiC/BCB, the positive and negative fixed charges have been considered. The influence of these charges was studied qualitatively and quantitatively. The results show in the Figure 5 correspond to a  $7\mu\text{m}$  depth trench filled with BCB.

It is worth noting that for positive or negative charge densities below  $10^{11}\text{ cm}^{-2}$ , the  $V_{BR}$  is not changed (cf right graph in the Figure 5 which details the  $V_{BR}$  for this range of charge densities). Below  $-10^{11}\text{ cm}^{-2}$  of negative charge density, the  $V_{BR}$  increases rapidly and above  $10^{11}\text{ cm}^{-2}$  positive charges density the  $V_{BR}$  decreases also rapidly. This  $V_{BR}$  behavior is correlated with a shift of the boundaries of the space charge region by increasing or decreasing the distance between the equipotential lines.

At the conference and in the final paper will be presented complementary results as electrical measurements on structures which are under technological process.

[1] Y. C. Kao, E. D. Wolley, "High-Voltage Planar p-n Junction", Proceedings of the IEEE, vol. 55, 1967.

[2] C. B. Goud, K. N. Bhat, "Two-dimensional analysis and design consideration of high-voltage planar junctions equipped with field plate and guard ring", IEEE Trans. Electron Devices, vol. 38, pp. 1497-1504, Sept. 1991

[3] D. Jaume, G. Charitat, J.M. Reynès, P. Rossel, "High voltage planar devices using field plate and semi-resistive layers", IEEE Trans. Electron Devices, vol. 38, pp. 1681-1684, July 1991.

[4] V. A. K. Temple, W. Tantraporn, "Junction termination extension for the near-ideal breakdown voltage in p-n junction", IEEE Trans. Electron Devices, vol. ED-33, pp. 1601-1608, Oct. 1986.

[5] Y. Bai, A. Q. Huang, X. Li, "Junction termination technique for Super Junction devices", Proceedings ISPSD'2000, Toulouse (France), pp. 257-261, May 2000

[6] Z. Qu, "Termination structure for Superjunction device", US Patent N°US 6621122, 2003.

[7] D. Dragomirescu, G. Charitat, F. Morancho, P. Rossel, "Novel concepts for high voltage junction termination techniques using very deep trenches", Semiconductor Conference, 1999. CAS '99 Proceedings. 1999 International.

[8] <http://www.synopsys.com/Tools/TCAD>

[9] M. Lazar, H. Vang, P. Brosseard, C. Raynaud, P. Cremillieu, JL Leclercq, et al., "Deep SiC etching with RIE," Superlattices and Microstructures, vol. 40, pp. 388-392, Oct-Dec 2006

[10] R.J. Hoekstra, M.J. Kushner, V. Sukharev, P. Schoeborn "Microtrenching resulting from specular reflection during chlorine etching of silicon", J. Vac. Sci. Technol. B 16, 4, Jul/Aug 1998, p2102

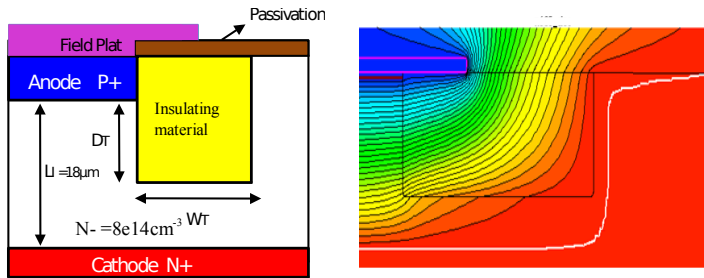


Figure 1: 2D cross section of the vertical P/N diode with DT2 protection and the potential distribution

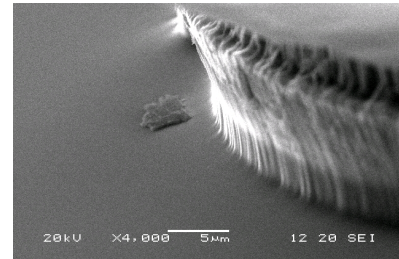


Figure 2: SiC etched trenches observed by Scanning Electronic Microscope

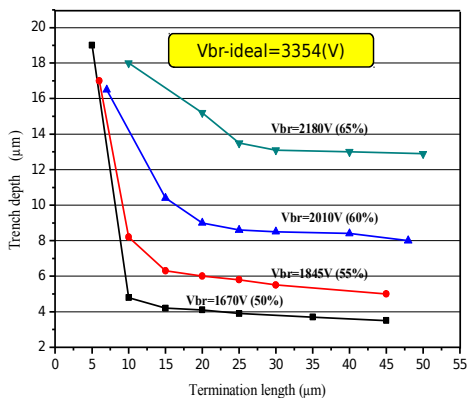


Figure 3: Breakdown voltage as a function of trench depth and trench width

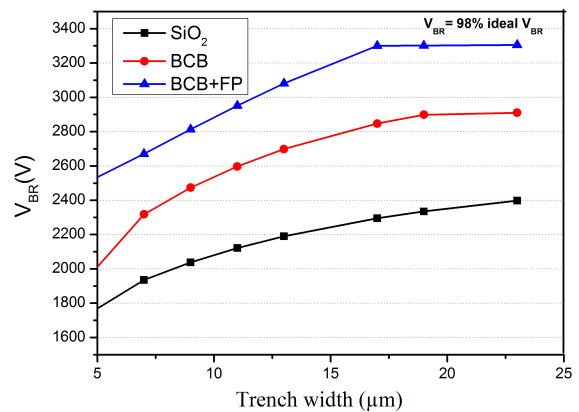


Figure 4: Breakdown voltage as a function of trench width and dielectric material

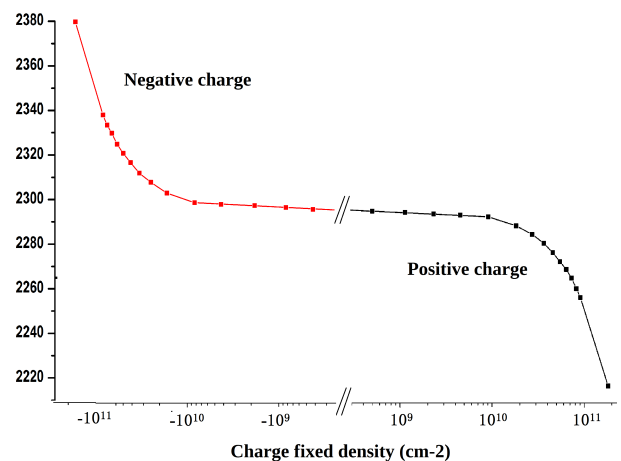
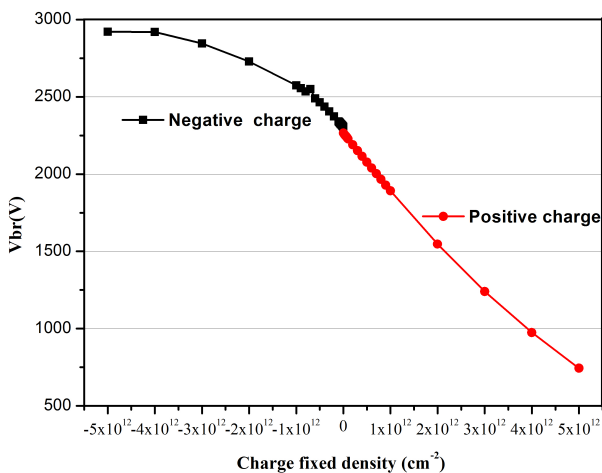


Figure 5 :  $V_{BR}$  as a function of charge density for a structure with 7  $\mu\text{m}$  DT2 depth filled with BCB