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Reliability Assessment of 4GSP/s Interleaved SAR ADC

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Abstract—For high performance applications like satellite receivers, Interleaved Successive-Approximation-Register (ISAR) Analog to Digital Converter (ADC) are widely used because they have good tradeoff between high performance sampling rate, effective resolution, power and small area in GHz range. Very few work is reported about the impact of aging induced degradation in SAR ADC. After presenting the design content, experimental results of aging at 40°C and 125°C are shown. Degradation of static and dynamic performance parameters will be illustrated. Then, the analysis of reliability for all the critical sub-blocks of the ADC is discussed, i.e. switches in capacitor array, comparator and latch. In conclusion, the sub-block which is mainly responsible for performance degradation is the latch.

Keywords: 28FDSOI, Aging, Degradation analysis, Reliability, TI-SAR ADC.

I. INTRODUCTION

Systems usually used in space, biomedical and avionics applications consist in an analog front-end, to collect data for control and observation purposes, and a digital unit to process the collected data. Important research efforts have been made to develop robust digital circuits, with dedicated sensors to monitor reliability. In contrast, very few studies have been done to address analog circuits and especially ADCs which are integral parts of most mixed-signal circuits [1, 2]. Hence, aging simulations and degradation analysis become necessary.

Different degradation mechanisms, including negative-bias temperature instability (NBTI), hot carrier injection (HCI), time-dependent dielectric breakdown (TDDB), and electromigration (EM), are resulting in performance degradations in these aging-sensitive complex systems [3]. In literature, the great majority of reliability studies reported in this field have focused on studying ADC degradation only in simulations based on device-level models. Some works have shown that the degradation in the input buffer and bootstrapped switches can be ignored. However, the asynchronous SAR logic and comparator can suffer from NBTI. Some work [1] focus on the comparison of degradation in the buffer and comparator with reference to

the degradation in the capacitor array and they conclude that most of the static and dynamic performance parameters are severely affected by the DAC capacitor-array degradations. Whereas, in case of the buffer and comparator degradations, only offset from the static performance parameters and all of the dynamic performance parameters are severely affected [2]. In this paper, we analyze the degradation effects in the static and dynamic performance parameters include offset gain, skew, signal to noise and distortion (SINAD), total harmonic distortion (THD), and effective number of bits (ENOB).

The paper is organized as following. Section II will briefly describe the sub-blocks of TI-SAR ADC. Section III will investigate experimental results to analyze the static and dynamic performance parameters which will be compared to simulation results illustrated in section IV. Conclusions will be provide in section V followed by some important references in section VI.

II. INTERLEAVED SAR ADC

Basically, a SAR ADC is composed of a comparator, DAC and self-timing asynchronous digital logics, **Fig.1**. The comparator is made of a preamplifier followed by a clocked inverter that drives a latch [4].

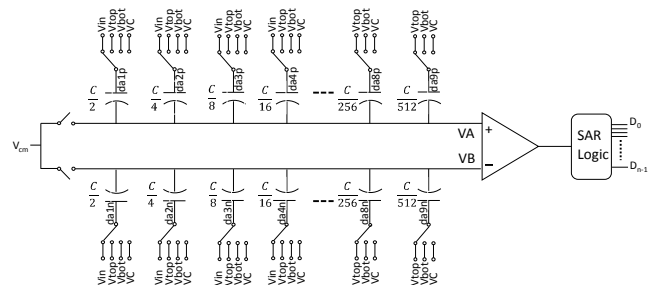


Fig.1: Conventional SAR ADC schematic

The input signal V_{in} is successively compared to different voltage levels and depending on the latch decision the top

plate of the sampling capacitor can switch from the intermediate voltage $V_c=500\text{mV}$ to either $V_{\text{top}}=750\text{mV}$ or $V_{\text{bot}}=250\text{mV}$. The bottom plate is connected to a fixed-voltage $V_{\text{cm}} = 700 \text{ mV}$. To increase the effective sampling rate, interleaved ADC architecture can be used by multiplexing several identical ADC in parallel. As illustrated in **Fig.2**, the block diagram under investigation consists in 16 interleaved 12-bit fully differential SAR ADC.

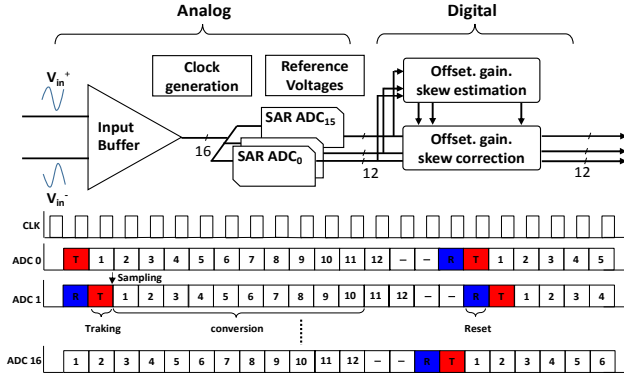


Fig.2: Overall circuit diagram of the interleaved SAR ADC and sequence of conversion.

First, the input signal is buffered by a follower stage to supply enough current to charge the SAR ADC sampling capacitor tanks, then data to be evaluated is maintained with sample hold circuit [5], and binary-weighted conversion is performed in 16 clock cycles. The sequence of conversion is piloted by the SAR logic which generates the control signals for the comparator and the switches. The 16 SAR ADC give an effective conversion rate of $16 \times 0.25\text{GS/s}$.

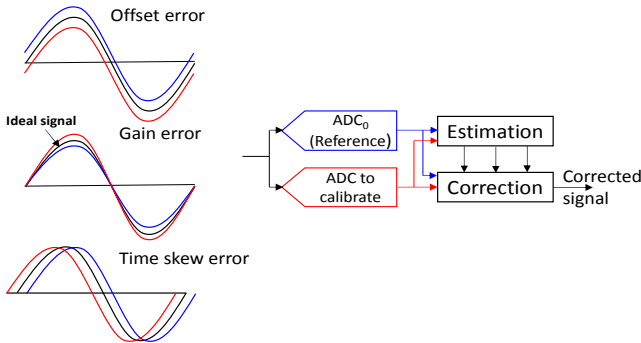


Fig.3: Offset, gain and skew calibration principle

This architecture natively suffers from mismatch between the different channels, it results in a degraded SNR, SFDR, and ENOB. To fulfill high dynamic performance, intensive research is developed in self-compensation or self-calibration schemes. For 8-10 bits resolution, the compensation of process mismatch capacitor bank and nonbinary-weighted conversion is not necessary but important efforts has been spent to calibrate skew of ISAR [6]. Here, these effects are compensated with digital derivative-based estimation of

timing mismatches, **Fig.3**. Gain, offset and skew mismatch calibrations are performed entirely in the digital domain through equalization of the averages of each sub-ADC output to the average of the sub-ADC0 output [6].

III. EXPERIMENTAL RESULTS

The circuit, composed of low-Vt flavor, is fabricated in 28nm Ultra-Thin Body and Box fully depleted (UTBB) SOI technology fabricated by STMicroelectronics for its performances and body bias capability.

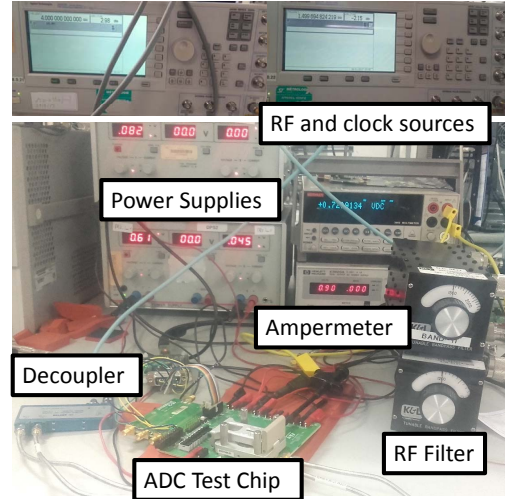


Fig.4: Setup of ADC board measurement. External RF clock and analog sin-wave. Analog and digital supply voltages: 1.1V and 0.9V.

The chip is packaged and located in the socket of PCB board. As illustrated in **Fig.4**, the ADC on-board measurement environment is composed of external power supply (one for analog and a second one for digital blocks) RF source clock and sin-wave analog signal with band pass filters. Data is converted and stored in SRAM memory on chip. The final data is finally read at low speed through a JTAG controller. Then it is transferred through SPI interface on computer.

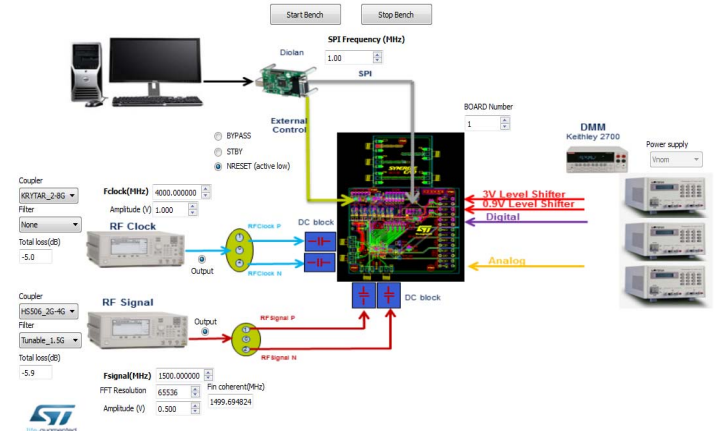


Fig.5: Setup of Python software full custom GUI environment for dynamic performance characterization.

Raw data is post processed in Python software with full custom GUI as illustrated by the setup of Fig.5.

As shown in the Fig.6, the ISAR-ADC output spectrum measured without digital compensation exhibits some interleaving spurs that can be removed with the digital background mismatch calibration.

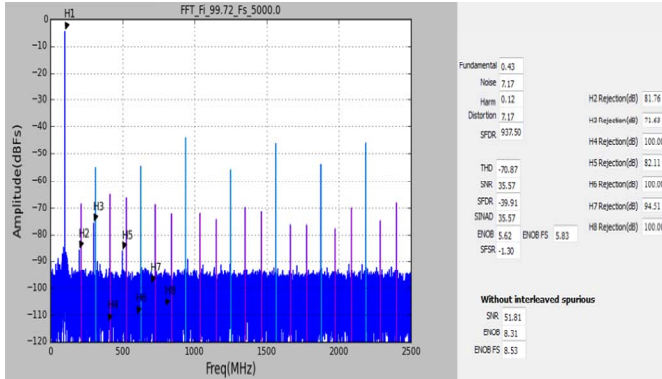


Fig.6: ISAR ADC output spectrum exhibits some interleaving spurs.

In order to mimic aging experiences during operating life, stress conditions consist in applying over supply in the chip for a short period to exacerbate the relevant wear out failure mechanisms.

The aging of the circuit is performed with a heater system located on the top of the package. A 48h stress are performed at 40°C and 125°C with different read points. During stress the circuit is operating at 4GHz clock and analog data is a high speed sine wave signal, supply voltages are increased at Vnominal+60%. A second stress of 5 days was done at 125°C and during stress the circuit is operating at 3GHz clock and low speed analog sine wave signal. Supply voltages are increased at Vnominal+40% to mimic High Temperature Operating Lifetime condition. For the sake of understanding the aging effect, analog supply is reduced at 0.9V during read point, although it affects significantly the performance, the circuit is more sensitive to degradation. Extracted performances are gain, skew and offset given by digital estimator, and SNR, ENOB, SINAD, SNDR, SFDR and THD are post-processed by the FFT of the output codes.

As depicted in Fig.7 and Fig.8, during the first stress at 40°C, the offset of all SAR ADC has changed and can reach up to 6mV, absolute skew (with reference ADC₀) can be 4ps while relative gain (with reference ADC₀) seems to be unchanged. Interestingly, the offset dispersion of all channels SAR ADC seems to be increased. Assuming the same activity of the comparator differential pair, due to the stochastic nature of interface defect density caused by HCI and BTI, the offset mean value should be null while standard deviation is degraded. The same conclusion is drawn for skew degradation, skew is issued from phase shift between the different channels due to local mismatch. Only the spread inter SAR ADC is degraded.

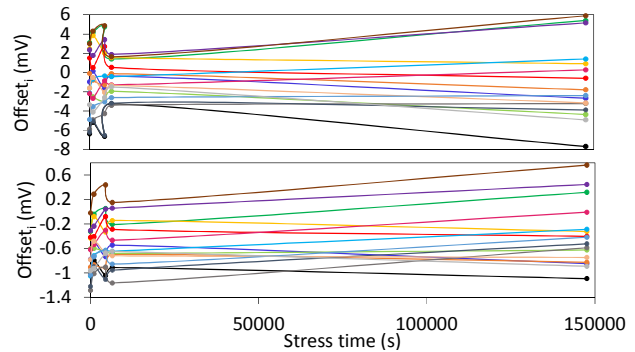


Fig.7: 16 ADCs Offset Measurements at 40°C after stress without (top) and with (bottom) analog and digital compensation.

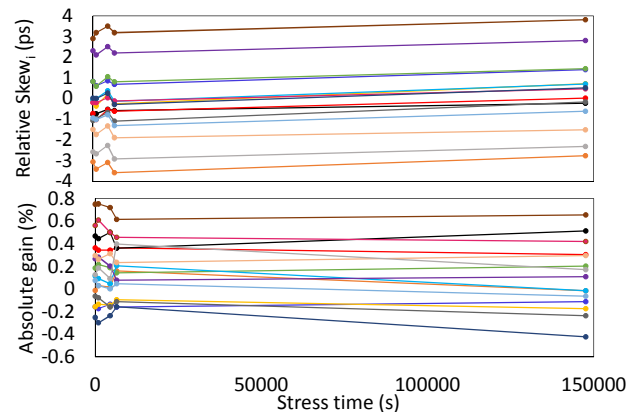


Fig.8: Relative skew regarding skew₀ (top) and absolute gain in (%) with reference to gain of ADC₀ (bottom) after different stress durations at 40°C.

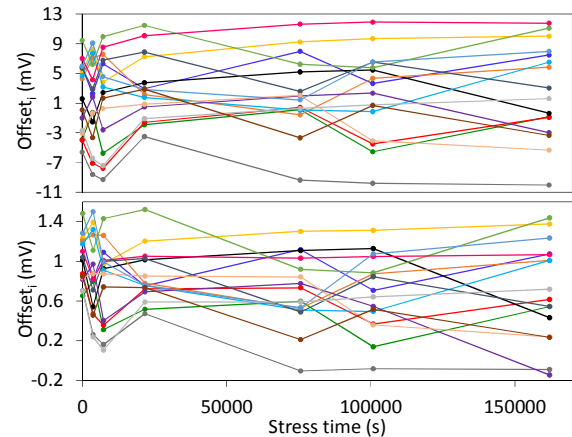
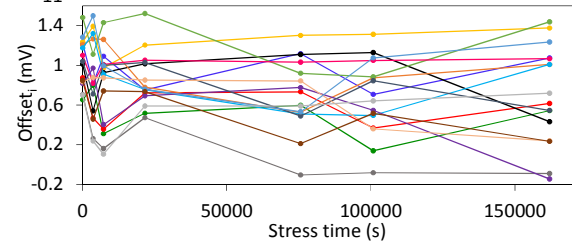


Fig.9: 16 ADCs Offset Measurements at 125°C after stress without (top) and with (bottom) analog and digital compensation.



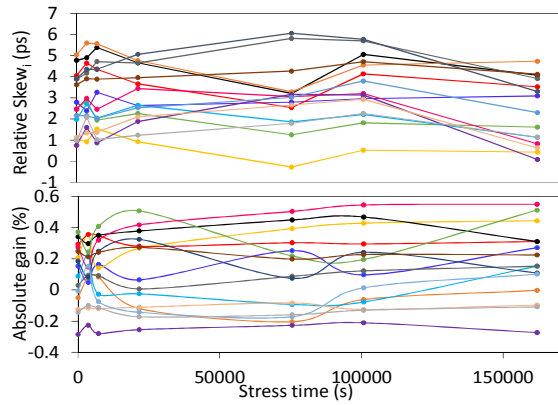


Fig.10: Relative skew regarding skew₀ (top) and absolute gain in (%) with reference to gain of ADC₀ (bottom) after different stress durations at 125°C.

The same behavior is observed for a 125°C stress as shown in Fig.9 and Fig.10. Spread of skew and offset seems to be more important than at lower temperature stress. Note that digital compensation enables to correct perfectly the offset and gain deviation in time. The table 1 summarize the figure of merit for the two stress and show a significant degradation of SNR of 2.4dB after a stress at 125°C.

	T= 40°C				T= 125°C			
	No compensation		With compensation		No compensation		With compensation	
	Fresh	Aged	Fresh	Aged	Fresh	Aged	Fresh	Aged
SNR (dB)	29.2	-1.41	42.9	-0.06	26.1	-2.41	40.927	-0.14
SINAD (dB)	28.9	-1.32	38.41	-0.05	26.15	-2.407	40.64	-0.2
SFSR (dB)	10.29	0.01	10.46	-0.001	10.6	-0.012	10.7	-0.01
ENOB(bits)	6.22	-0.22	7.83	-0.008	5.82	-0.398	8.24	-0.04
THD (dB)	40.3	-0.03	40.3	-0.041	53.6	-0.001	52.69	-1

Table 1: Measurement results of ISAR ADC performances variation after first stress either at 40°C or 125°C.

Second stress was applied with the same procedure of read points but at different conditions. The stress was performed only at 125°C. Unlike previous measurement done at high speed sine wave input signal, measurements in this case were done at low speed. The dynamic performances degradations were illustrated us summarized in table 2. SNR degradation of 8dB is very important.

	No compensation		With compensation	
	Fresh	Aged	Fresh	Aged
SNR (dB)	35.6	-2	49.9	-8.9
SINAD (dB)	37	-3.46	49.9	-8.9
SFSR (dB)	1.2	-3.78	1	-3.8
ENOB(bits)	5.83	-0.29	8.19	-0.83
THD (dB)	70.8	-1.95	70.1	-2.9

Table 2: Measurement results of ISAR ADC performances variation after second stress at 125°C.

In table 3 we can observe the SNR degradation of each ADC for the second stress. Degradation before interleaving is more important. The same behavior is observed in Fig.11 and Fig.12 for the skew, gain and offset

	ADC1	ADC2	ADC3	ADC4	ADC5	ADC6	ADC7	ADC8	ADC9	ADC10	ADC11	ADC12	ADC13	ADC14	ADC15	ADC16
SNR Fresh	51.79	51.77	51.88	51.54	52.01	51.86	52.12	51.84	51.91	52.07	52.06	51.84	51.82	52.01	51.95	51.89
SNR aged 125°C	41.32	41.28	41.13	41.23	41.18	41.23	41.24	41.23	41.24	41.34	41.25	41.3	41.25	41.38	41.25	41.32

Table 3: SNR variation before and after aging at 125°C for all ADCs.

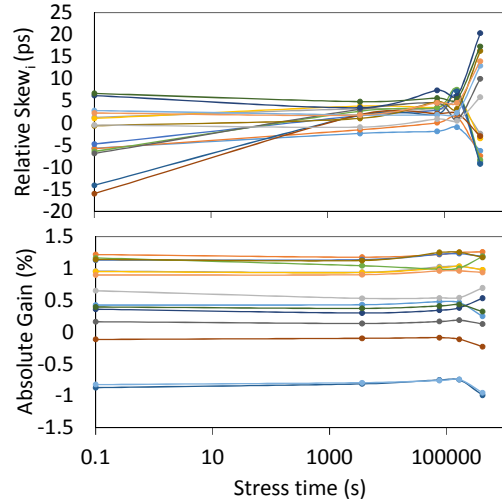


Fig.11: Relative skew regarding skew₀ (top) and absolute gain in (%) with reference to gain of ADC₀ (bottom) after different stress durations at 125°C.

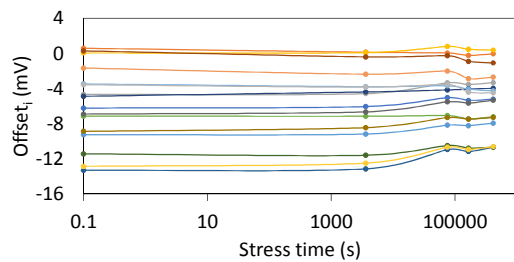


Fig.12: 16 ADCs Offset Measurements at 125°C after second stress

IV. SIMULATION RESULTS

To analyze those degradations, Design-in-Reliability simulation is performed at low speed input signal. Measurements results of the second stress condition were compared with simulation results. Extracted Fast Fourier Transform (FFT) for each condition is shown in Fig.13 after stress of all-ADC blocks.

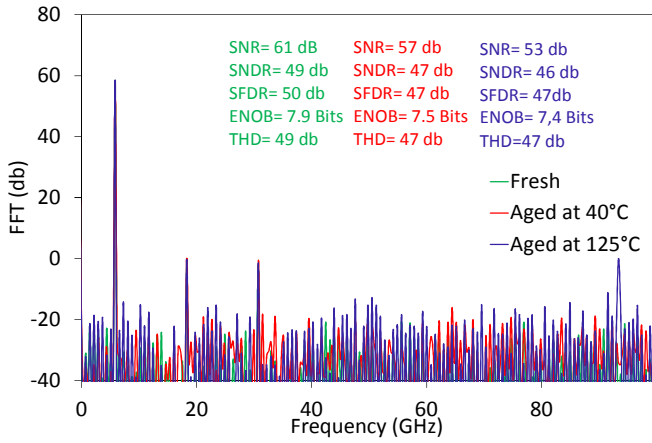


Fig.13: Simulated FFT extracted at fresh condition and after stress at 40°C and 125°C.

To investigate the aging effects in static and dynamic performance parameters of TI-SAR ADC and to analyze the sensitivity of the different sub-blocks, whole system has been divided into its sub-blocks and the degradation effects of each individual block have been incorporated into its system-level models. Aging models developed on device level was used as input of Design-in-Reliability simulation.

Table 4 summarize in detail the CAD-Si results of extracted performances after aging at 40°C and 125°C. Qualitative agreement between measurement and simulation is observed at 125°C.

	Fresh	Aged at T=40°C			Aged at T=125°C		
		Overall ADC	Only T&H switches	Comparator & Latch	Overall ADC	Only T&H switches	Comparator & Latch
SNR (dB)	61.7	-3.8	0.19	-6.24	-8.3	0	-11
SNDR(dB)	49.4	-2.1	-1.07	-1	-3.19	-0.33	-2.5
SFDR(dB)	50.01	-2.06	-1.16	-0.34	-2.59	-0.35	0.38
ENOB(Bits)	7.92	-0.35	-0.17	-0.16	-0.52	-0.05	-0.42
THD (dB)	49.7	-2	-1.14	-0.29	-2.51	-0.35	-0.42

Table 4: Simulation results of ISAR ADC performances variation after aging of different ADC blocks at different temperatures.

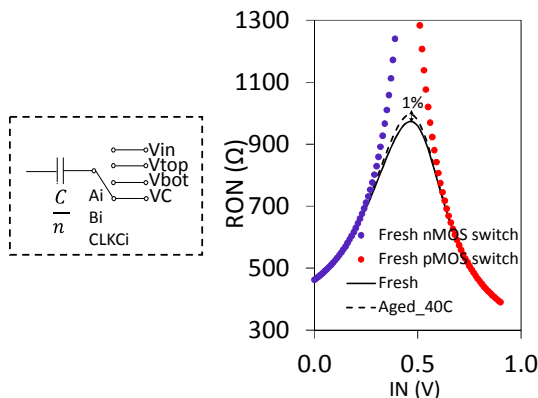


Fig.14: “ON” Resistance (Ron) of fresh and aged transmission gate switches

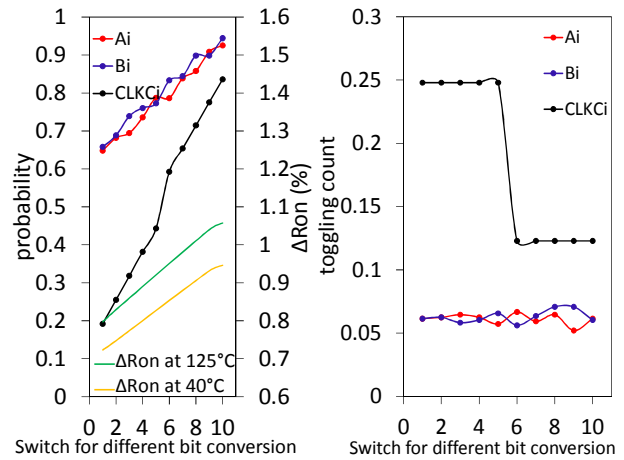


Fig.15: Probability and toggling of different switches commands (Ai, Bi, CLKCi)

As reported in the **Table 4**, when considering only aged devices in track and hold switches the overall contribution is minor. While for comparator and latch the impact is more significant. Note that the difference CAD-Si is due to the fact that simulation is noiseless. The first sub-block under investigation is the switches, indeed the sampling speed of the switch capacitor circuit depends on the value of C and the on-resistance of MOS transistor Ron. The top plate switches are transmission gates to improve linearity and to reduce the signal-dependent on-resistance. The Ron degradation is analyzed, it always remains smaller than $LSB/2$, **Fig.14**. Note that activity and probability for the different switches of capacitor bank presented in **Fig.15** are very different. Activity is given by toggling count and probability leads to unbalanced Ron degradation.

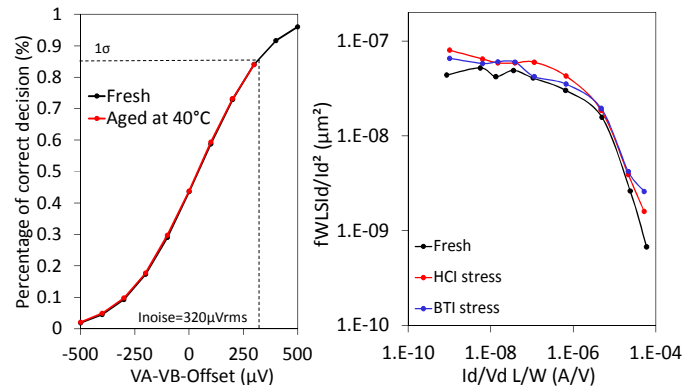


Fig.16: Input-referred noise simulation (left). Noise spectral density (right) measured at wafer level. No effect of HCI and NBTI on noise performances.

The second sub-block reviewed is the comparator. Irms noise of comparator, **Fig.16 (left)**, is studied assuming a Gaussian distribution of input offset, $I_{rms}=320\mu V_{rms}$ is not impacted by aging. To confirm that no interaction occurs during HCI or BTI and low frequency noise performance, wafer level

measurement is performed in **Fig.16 (right)**, noise spectral density is not modified by aging, in linear or saturation regime.

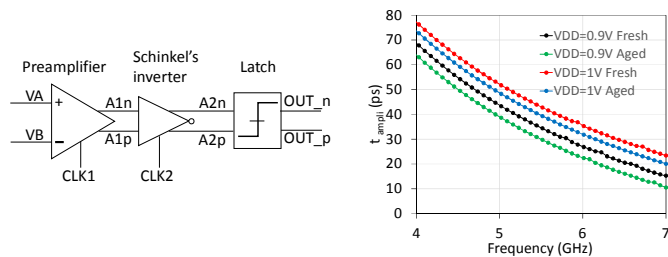


Fig.17: Comparator blocks and the variation of amplification time versus frequency before and after aging.

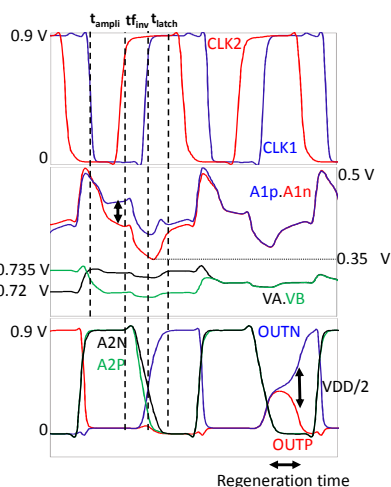


Fig.18: Different time windows for each sub-block

When evaluating the preamplifier gain, a dependence is observed with clock frequency and aging, **Fig.19**. The slew rate of comparator is not modified by aging, but the time for which the gain is the highest (t_{amp}) is decreased with frequency and aging (**Fig.17**), it results in SNR degradation (**Fig.19**).

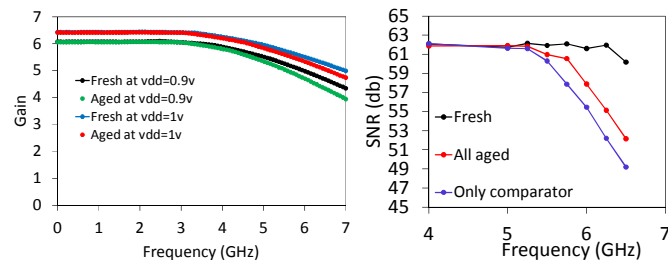


Fig.19: The gain of the comparator at rising CLK2 is decreased after aging, resulting in SNR degradation.

Note the time windows shown in **Fig.18**: t_{amp} , time for Schinkel inverter falling edge (t_{inv}), time for latch (t_{latch}) are generated by asynchronous digital logic and are modified with aging, **Fig.20**, which can lead to a wrong decision.

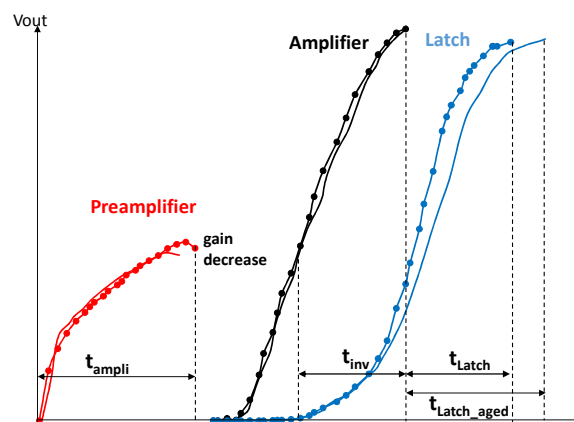


Fig.20: Characteristic settling time for preamp, amp and latch before and after stress.

V. CONCLUSIONS

In this paper, dynamic performances of an ISAR-ADC due to aging is investigated and compared with measurement. Digital compensation can correct the offset and skew spread increase. The slight degradation of SNR is due to a reduction of time windows for both the comparator gain, and regeneration time for latch. The time window is driven by self-timing digital logic which is affected by aging.

VI. REFERENCES

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