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## 4H-SiC VJFETs with self-aligned contacts

Konstantinos Zekentes<sup>1, a, \*</sup>, Antonis Stavrinidis<sup>1)</sup>, George Konstantinidis<sup>1)</sup>, Maria Kayambaki<sup>1)</sup>, Konstantinos Vamvoukakis<sup>1)</sup>, Emmanouil Vassakis<sup>1)</sup>, Konstantin Vassilevski<sup>2)</sup>, Alton B. Horsfall<sup>2)</sup>, Nick G. Wright<sup>2)</sup>, Pierre Brosselard<sup>3)</sup>, Shiqin Niu<sup>3)</sup>, Mihai Lazar<sup>3)</sup>, Dominique Planson<sup>3)</sup>, Dominique Tournier<sup>3)</sup>, Nicolas Camara<sup>4)</sup>

<sup>1</sup> MRG-IESL/ FORTH, Vassilika Vouton, PO Box 1385 Heraklion, Greece

<sup>2</sup> School of Electrical and Electronic Engineering, Newcastle University, Newcastle upon Tyne, NE1 7RU, England, United Kingdom

<sup>3</sup> INSA de Lyon, Laboratoire Ampère, 21 Avenue Jean Capelle, 69621 Villeurbanne Cedex, France

<sup>4</sup> GREMAN (UMR-CNRS 7347), 16 rue Pierre et Marie CURIE FRANCE

<sup>a</sup>[trifili@physics.uoc.gr](mailto:trifili@physics.uoc.gr), <sup>b</sup>[astav@physics.uoc.gr](mailto:astav@physics.uoc.gr), <sup>c</sup>[aek@physics.uoc.gr](mailto:aek@physics.uoc.gr), <sup>d</sup>[mmic@physics.uoc.gr](mailto:mmic@physics.uoc.gr), <sup>e</sup>[vamvk@hotmail.com](mailto:vamvk@hotmail.com), <sup>f</sup>[vassakise@hotmail.com](mailto:vassakise@hotmail.com), <sup>g</sup>[Konstantin.Vasilevskiy@newcastle.ac.uk](mailto:Konstantin.Vasilevskiy@newcastle.ac.uk), <sup>h</sup>[ca.b.horsfall@ncl.ac.uk](mailto:ca.b.horsfall@ncl.ac.uk), <sup>i</sup>[dn.g.wright@ncl.ac.uk](mailto:dn.g.wright@ncl.ac.uk), <sup>j</sup>[pierre.brosselard@insa-lyon.fr](mailto:pierre.brosselard@insa-lyon.fr), <sup>k</sup>[shiqin.niu@insa-lyon.fr](mailto:shiqin.niu@insa-lyon.fr), <sup>l</sup>[mihai.lazar@insa-lyon.fr](mailto:mihai.lazar@insa-lyon.fr), <sup>m</sup>[dominique.planson@insa-lyon.fr](mailto:dominique.planson@insa-lyon.fr), <sup>n</sup>[dominique.tournier@insa-lyon.fr](mailto:dominique.tournier@insa-lyon.fr), <sup>o</sup>[nicolas.camara@univ-tours.fr](mailto:nicolas.camara@univ-tours.fr), \*corresponding author

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**Abstract.** Trenched-implanted-gate 4H-SiC vertical-channel JFET (TI-VJFET) have been fabricated with self-aligned nickel silicide source and gate contacts using a process sequence that greatly reduces process complexity as it includes only four lithography steps. The effect of the channel geometry on the electrical characteristics has been studied by varying its length (0.3 and 1.2 $\mu\text{m}$ ) and its width (1.5-5 $\mu\text{m}$ ).

The transistors exhibited high current handling capabilities (Direct Current Density 330A/cm<sup>2</sup>). The output current reduces with the increase of the measurements temperature due to the decrease of the electron mobility value. The voltage breakdown exhibits a triode shape, which is typical for a static-induction transistor operation.

### Introduction

SiC JFETs may have the lowest overall losses of switching devices and can operate at temperatures over 400°C. Over different JFET designs the trenched and implanted (TI) gate vertical JFET is very attractive since it may have the lowest on-resistance and its fabrication does not require epitaxial overgrowth or multiple angled ion implantations [1]. The main difficulty of TI-JFETs processing deals with the small dimensions of the source pillars.

This paper reports on the fabrication of SiC TI-VJFET with self-aligned nickel silicide source and gate contacts using a process sequence that greatly reduces process complexity as it includes only four lithography steps.

### Device processing

Two epitaxial structures on the top of the n<sup>+</sup> 4H-SiC wafers have been employed for fabricating the devices (Fig.1). The first epitaxial structure (structure A) was composed by a 34.5  $\mu\text{m}$  thick blocking n-layer with donor concentration ( $N_D$ ) of  $2.2 \cdot 10^{15} \text{ cm}^{-3}$  and a top 0.32  $\mu\text{m}$  thick n+ layer with  $N_D=1.1 \cdot 10^{19} \text{ cm}^{-3}$ . The second epitaxial structure (structure B) was composed by a 8  $\mu\text{m}$  thick blocking n-layer with donor concentration ( $N_D$ ) of  $5.5 \cdot 10^{15} \text{ cm}^{-3}$  and a top 2  $\mu\text{m}$  thick n+ layer with  $N_D=1 \cdot 10^{19} \text{ cm}^{-3}$ . Source fingers and gate trenches were formed by reactive ion etching (RIE) by using the first lithographic step. Gate regions were formed by ion implantation followed by a

thermal annealing at 1600°C. The gate depth for the structure A was 1.1µm thick while for the structure B was 0.3µm thick. Then, the samples were oxidized to form a 35 nm thick oxide on the Si-face and a 240 nm thick oxide on mesa-structure sidewalls. The horizontal oxide has been removed by RIE. Following, 50 nm thick Ni contacts were deposited by e-beam evaporation and

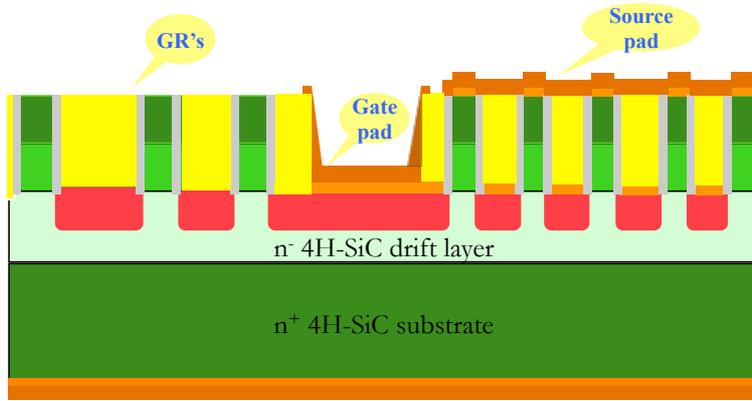


Fig.1. Schematic of the device cross-section (Dark to light green: higher to lower doping n-type SiC, red: p-type SiC, yellow: cyclotene, grey: SiO<sub>2</sub>, light orange: Ni contact, dark orange: Au overlay.

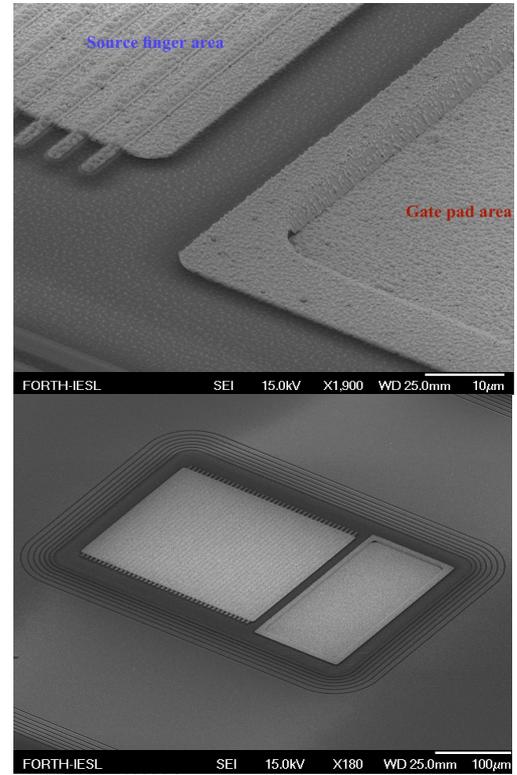


Fig.2. SEM photos of the completed device.

patterned (2<sup>nd</sup> photolithography step) to remove the metal from the edge termination and device separation regions. A 100 nm thick Ni layer has been also deposited on the wafer back side and then, the samples were annealed to form ohmic contacts. The next process step was the application of a trench filling dielectric (cyclotene<sup>c</sup>), its curing and etching-back to expose the mesa-structure tops with source contacts. Then, the dielectric has been etched by RIE to open the gate pad contacts at the third lithography step. Finally, a final fourth lithographic step was employed for depositing and patterning the common source and gate pad Au metal overlay (Fig.2). Edge termination is provided by a self-aligned multiple floating-guard-ring structure. The transistors with the structure A can be grouped in 4 categories according to the specific lithography conditions (exposure time etc.). More details on the device processing and its optimization are given in [2].

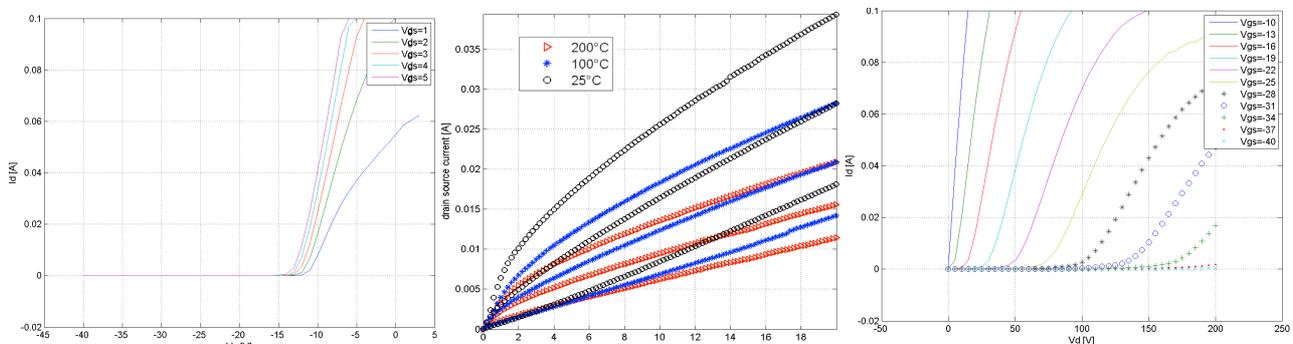


Fig.3. DC transfer (left), on-state at three temperature values (middle) and blocking (right) I-V characteristics of SiC TI-VJFETs fabricated on structure A.

## Electrical characterization results

DC I-V measurements are reported in Fig. 3 and 4 for the devices fabricated on structures A and B respectively. The reported results are from devices with a source finger widths of 2.5  $\mu\text{m}$  (structure

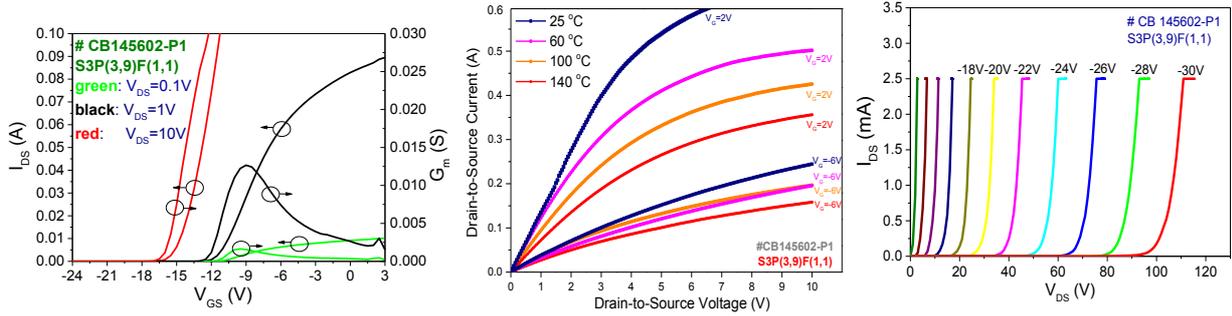


Fig.4. DC gate-source (left), on-state at three temperature values (middle) and blocking (right) I-V characteristics of SiC TI-VJFETs fabricated on structure B. The transistor blocking exhibits a triode shape, which is typical for a static-induction transistor operation showing on-air blocking voltages exceeding 250 V (best case of transistors with structure A) and 100 V (structure B). From these characteristics a series of device parameters can be extracted like the  $R_{ON}$  (7-15  $\text{m}\Omega\cdot\text{cm}^2$ /structure A and 4-8  $\text{m}\Omega\cdot\text{cm}^2$ /structure B), the threshold voltage  $V_{TH}$  (10-15V/structure A and -7.5V/structure B for  $V_{DS}=1\text{V}$ ), the  $I_{DS}$  leakage current at  $V_{TH}-20\text{V}$  &  $V_{DS}=0\text{V}$  (1nA/structure A and 0.37mA/structure B) and the voltage gain (from 4.1 to 13.3 for structure A and 3.6/structure B).

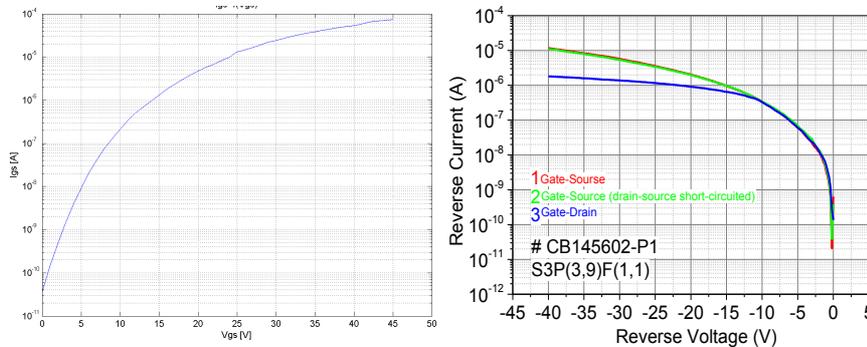


Fig.5. DC gate-source of SiC TI-VJFETs fabricated on structure A (left) and on structure B (right). structure A and 3.6/structure B).

The transistors exhibited high current handling capabilities (DC 330A/cm<sup>2</sup> for both structures). The output current reduces with the increase of the measurements temperature due to the decrease of the electron mobility value.

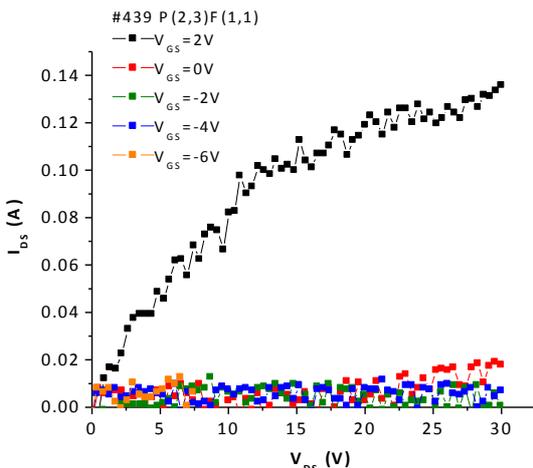


Fig.6. Pulsed I-V characteristics of normally-off SiC TI-VJFETs fabricated on structure A. The 4H-SiC TI-VJFETs demonstrated both normally-on and normally-off (Fig.6) operation depending on the source width and specific lithography conditions.

The gate-source/drain characteristic evaluates the quality of the gate junction and can be used for determining the transistors—measurements conditions for the conduction (ON-) and the blocking (OFF-) characteristics. The extracted values are the knee voltage (around 2.7 V for both structures) and the breakdown voltage defined as the reverse voltage value at 1  $\mu\text{A}$  current (-20V for structure A and -35V for structure B). The majority of the  $I_{GS}(V_{GS})$  characteristics didn't exhibit any double barrier.

On-state I-V characteristics were also performed in pulsed mode to avoid self-heating of the devices and the gate has been biased below its 2.7-V built-in potential value to maintain voltage-control capability (high  $I_D/I_G$  gain). The 4H-SiC TI-VJFETs demonstrated both normally-on and normally-off (Fig.6) operation depending on the source width and specific lithography conditions.

C-V measurements have been also performed to determine dynamic operation parameters (Fig. 7). We observe that below the cut-off voltage  $C_{GS}$  and  $C_{G-DS_{sc}}$  take a practically constant value ( $\sim 1.8\text{pF}$  and  $\sim 1.6\text{pF}$  respectively) while there is a continuous decrease of the  $C_{GD}$  with decreasing

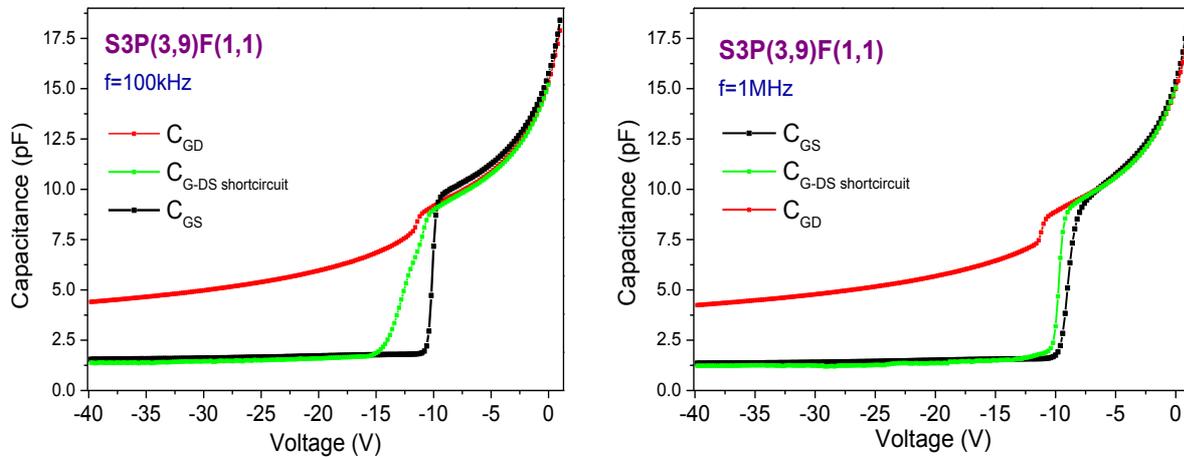


Fig 7.  $C_{GD}-V_{GD}$ ,  $C_{GS}-V_{GS}$  and  $C_{G-DS_{sc}}-V_{G-DS}$  from a transistor with structure B for  $f=100\text{kHz}$  (left) and  $f=1\text{MHz}$  (right). In addition,  $C_{GD}$  has always a higher value than  $C_{GS}$  and  $C_{G-DS_{sc}}$ . Both effects are related to the fact that the depletion region between the gate and the source are more or less constant below the cut-off voltage while the extension of that between the gate and the drain continuously increases. Just above the cut-off voltage (or equivalently the pinch-off), an abrupt transition phenomenon is observed due to the fact that the channel has just opened. This transition phenomenon is more intense for  $C_{G-DS_{sc}}$  and  $C_{GS}$  (especially for the  $C_{GS}$ ).

According to the C-V results (especially from that with D-S short-circuited) the threshold voltage value is in the range  $-12.5 < V_{TH} < -9\text{V}$ , which is close to that determined from I-Vs. Therefore, there is no a trap-related problem in our transistors.

## Conclusions

4H-SiC TI-VJFETs with different channel lengths and channel widths have been fabricated and characterized. The electrical characteristics showed that the deeper gate transistors exhibit higher on-resistance values and lower leakage currents as expected. The threshold voltage values and gate-source characteristics are similar for the two types of transistors. The blocking characteristics are determined by a static induction effect and therefore rather from the channel geometry than from the drift layer doping and thickness.

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