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► **To cite this version:**

Maxime Berthou, Dominique Planson, Dominique Tournier. Short-Circuit Capability Exploration of Silicon Carbide Devices. Materials Science Forum, 2015, 821-823, pp.810-813. 10.4028/www.scientific.net/MSF.821-823.810 . hal-02133674

**HAL Id: hal-02133674**

**<https://hal.science/hal-02133674>**

Submitted on 19 May 2019

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# Short-Circuit Capability Exploration of Silicon Carbide Devices

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**Keywords:** Short-circuit, Silicon-Carbide, MOSFET, JFET, BJT, Current limiter

**Abstract.** This paper presents our study of SiC MOSFETs, JFETs and BJT under capacitive load short-circuit up to 600V. BJTs show heterogeneous results due to unstable technology. In the contrary MOSFETs critical short circuit show bus voltage dependency with critical time of about 10 $\mu$ s at 600V. The failure is repetitive and characterized by a gate to source short-circuit due to self-heating. On the other hand, LV-JFET device, despite its normally-on disadvantage and higher resistivity, and thanks to its current limiting capability, shows superior SC capability with critical time over 600 $\mu$ s at 600V. Exploitation of this feature allowed us to produce a current limiter prototype capable to strongly limit the current in order to stand short-circuit during 200ms at 400V.

## Introduction.

With the commercial availability of Silicon Carbide (SiC) power MOSFETs of good reliability, this decade will mark an important breakthrough in power transistor technology. However, in power electronic systems, driving errors or external disturbances may place power transistors in short-circuit condition and little knowledge exist about SiC devices short-circuit (SC) capability.

Thanks to its exceptional thermal properties; high cohesive energy, thermal conductivity and capacity, and mechanical strength, we expect superior short-circuit capability from SiC devices [1,2]. However, depending on the device, it may not solely depend on SiC properties. Structural layers above the crystal present different thermal properties, which will have an influence on the devices ruggedness.

This paper presents our study of different device structures under capacitive load short-circuit. We will first present the final setup used to characterize the devices, then we present our measurement results on MOSFETs, BJT, JFETs and JFET current limiters.

## Experimental Setup

The SC capability of the devices was tested under capacitive load as shown in figure 1, which allows a good control of the drain to source voltage bias and pulse width. Each driver is isolated and receives an optical command from a custom circuit capable of generating pulses of length between 600 ns and 20 ms with raise/fall time smaller than 10 ns. The control circuit is a programmable micro-controller, which allows generating a custom signal. The voltage source serves to charge the load capacitance and, its connection to the system is controlled by an IGBT. The load capacitance is dimensioned in function of the required bus voltage ( $V_{CC}$ ), and short-circuit energy. The device under test (DUT) is closed before and opened after the SC pulse to minimize parasitic effects due to its gate biasing. Finally, the SC pulse is created by the second IGBT controlled by DRIVER3. The SC current is measured by a 25m $\Omega$  (1200MHz) current sense resistor ( $R_{SENS}$ ) on the low side. Neglecting the voltage drop between  $R_{SENS}$  terminals, we measure the SC voltage on the DUT drain with a high voltage passive probe (1kV-500MHz). To reach and determine the critical SC of the device, the pulse time was gradually increased by 10% steps until failure of the device and the waveforms were captured systematically. The failure was identified by the loss of the device's gate control or blocking capability.

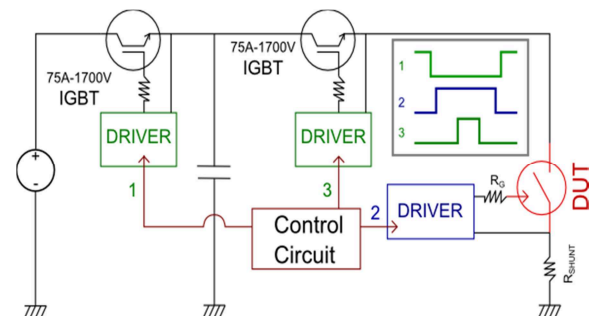


Fig. 1 – Schematic of short-circuit test circuit with capacitive load

## Measurement Results

Three types of SiC devices with comparable current and voltage capability have been studied; MOSFET, BJT and JFET.

**MOSFET.** Three models of 1200V MOSFETs, from CREE and ROHM, have been tested in similar conditions. 80mΩ CREE devices (C2M0080120) showed SC current of 200A and broke parts of our test circuit, to lower the SC current we chose a twice smaller device from the same range of products (C2M0160120). It effectively showed twice lower current peak (see figure 2).

ROHM devices show lower saturation current than the CREE ones. As we had only the 80mΩ-1200V ROHM device (SCT2280KE) at our disposal, we performed the tests and compared it with the 160mΩ-1200V CREE device, bearing in mind the difference of size. Comparing the SC waveforms at 600V for 160mΩ CREE and 80mΩ ROHM devices shown in figure 2, we can see that they exhibit different short-circuit behaviour. Considering the difference of current specification, ROHM devices show lower critical energy compared to CREE devices (see figure 3). However, the ROHM devices show three times lower maximum current peak for similar nominal ratings. This allows them to limit the current more efficiently and thus stand longer short-circuit for a given SC energy and bus voltage.

The difference of SC behaviour can be explained by the difference of MOS channel properties between each family of devices. In both devices, we can distinguish two phases in the SC waveform, first the current greatly increases in the first microsecond, then it slowly decreases until the device failure. The first phase corresponds to the effect of self-heating on the channel mobility, which is dominated by the Coulomb scattering at low temperature [3]. Then bulk mobility dominates and decreases with the temperature.

We can infer that the CREE devices are more influenced by the coulomb scattering effect than the RHOM devices. Such effect can be explained by different factors such as the lower density of interfacial traps, length of the channel and density of integration. Nonetheless, both devices show SC capability of the same order of magnitude.

In all the tests, the failure signature was characterized by a loss of gate control due to short-circuit between gate and source. This phenomenon can be due to different reasons such as the gate oxide breakdown, Aluminium migration in inter-layer dielectric or short-circuit between pads due to Aluminium melting [3]. Further investigations are required to determine the failure mechanism.

Looking at the critical energy ( $E_{SC-CRIT}$ ) and time ( $t_{SC-CRIT}$ ) in function of  $V_{CC}$  (see figure 4), we can see that they both decrease with increasing bias. As dissipated power increases, the hotspot, created by the current crowding, becomes too strong too fast, and improving the package cannot help to extract the power. Only a design improvement of the device can help to weaken the hot spot by lowering the saturation current. In the future, to optimize static and dynamic characteristics of SiC MOSFETs, its gate oxide quality will be improved by reduction of interfacial trap density, thus saturation current increase due to self-heating will be minimized and short-circuit capability improved.

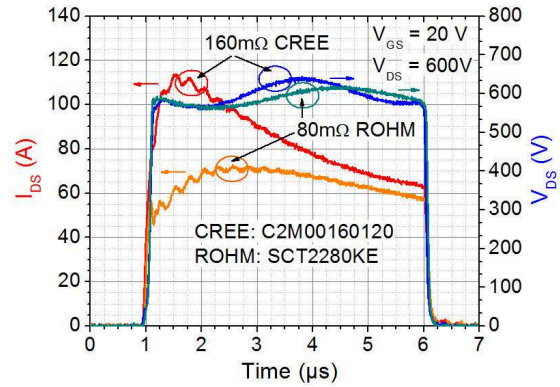


Fig. 2 - Short-circuit waveform at 600V on 80mΩ RHOM and 160mΩ CREE VMOS

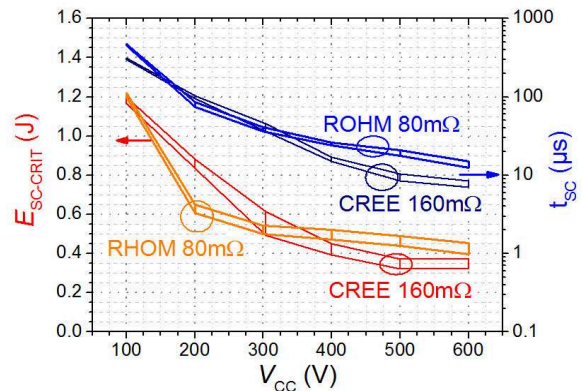


Fig. 3 – Critical energy and length of SC depending on bus voltage ( $V_{CC}$ ) up to 600V for CREE and RHOM 1200V SiC-MOSFETs

**BJT.** First generation of devices provided by Fairchild were stressed under similar pulses except that its width was defined by DUT's base bias (see figure 4). They show different behaviour; as we reached the base driver current limitation, we provide a current peak at the beginning, which creates collector current peak in the first  $40\mu\text{s}$  that stabilizes afterwards. Even though the test conditions are not ideal, this measurement provides an overview of the BJT SC capability. The figure 6 shows the longest SC waveform measured at  $370\text{V}$  for nominal current between  $8$  and  $12\text{A}$ . We tested devices under different base and collector bias conditions, the results were heterogeneous and always showed lower SC capability compared to the VMOS.

Devices breakdown is always characterized by the creation of base to emitter short-circuit. Reduction of the collector current during the short-circuit had little impact on the SC capability of the BJT. We infer that this failure is due to electrical breakdown of the inter-layer dielectric at high temperature or inappropriate electrical field repartition in the device during the SC. Structural or design improvements may enhance the short-circuit capability of the SiC BJT.

**JFET.** Another promising SiC device is the JFET [1], where the channel is situated deeper in the SiC. As the power is dissipated where the current flow is pinched, the hot spot is buried deeper than for the MOSFET. Then, superior metallic and dielectric layers suffer less from self-heating generated by the short-circuit condition.

We have tested three  $10\text{A}$  chips from the first generation provided by Infineon. To allow very fast flow of current toward the JFET, we replaced the IGBT by a SiC MOSFET. In figure 5, we can see that the raise time is less than  $1\mu\text{s}$  thanks to this upgrade.

The three tested devices have shown SC capability superior to the MOSFETs. Tests performed at  $600\text{V}$  for gate bias of  $0\text{V}$  and  $-6\text{V}$ , yielded critical energy and time of  $2.5\text{J}$  (see figure 6) and  $690\mu\text{s}$ , and  $2.9\text{J}$  and  $2.1\text{ms}$  respectively. The failure is characterized by a strong short-circuit between drain and source followed by its destruction, this was most probably due to extreme temperature peak generated by the SC as shown in a parallel study [4].

A third device was tested for a gate bias of  $-10\text{V}$ , thus limiting current at  $4\text{A}$ , which allowed sustaining short-circuit up to setup limit of  $9\text{ms}$  without failure, which represented a SC energy of  $6\text{J}$ . Depending on the device purpose or driver, this effect can be exploited in order to protect the

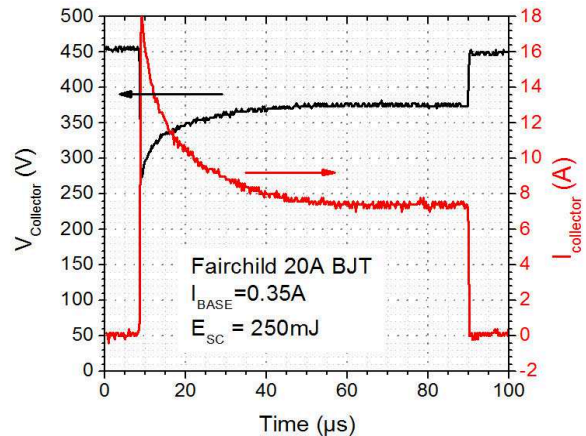


Fig. 4 - Short-circuit waveform on SiC power BJT performed with capacitive load

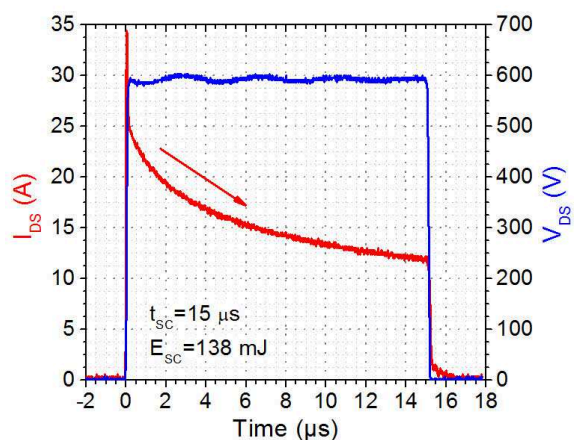


Fig. 5 -  $15\mu\text{s}$  Short-circuit waveform of a  $10\text{A}$  normally-on JFET provided by Infineon for  $0\text{V}$  gate bias

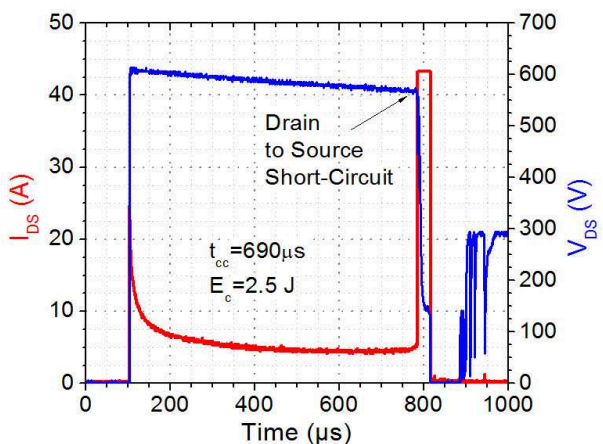


Fig. 6 - SC waveform of a  $10\text{A}$  normally-on FET provided by Infineon for  $0\text{V}$  gate bias



system or the device itself. The device design can also be modified in order to lower the current limit at  $V_{GS}=0V$ .

**Current Limiter JFET** is a perfect example of this principle. The channel dimensions are designed in such way that the device strongly limits the current at desired level with a moderate nominal resistance.

Former studies at CNM and Ampere laboratory have led to produce a prototype capable to limit the current around 3A and block voltage up to 450V with on-resistance of 150m $\Omega$  [5]. Further optimization will allow us to reach 1200V with lower on-resistance.

This prototype has been tested at 400V in this SC setup; it was mounted in cascode configuration with a 60V-50A commercial MOSFET. Waveforms, as long as 200ms shown in figure 7, were applied without failure. We can see that the waveform is similar to previously tested JFETs. Such pulse represents a total energy of 65J, which is far higher than the maximum energy reached on any of the previous devices. However, due to larger unit cell, this limitation was performed to the detriment of the conductivity of the device.

### Conclusions

We have seen that only the JFET architecture show superior SC capability, however it is difficult to compare such devices as they all present specific advantages and they all have been fabricated with different degrees of technology refinement. In LV-JFET, strong limitation necessitates at least 3 $\mu$ m of lateral channel, which limits the cell size minimization. Nonetheless, recent studies indicate that vertical devices show good results [3]. The current limiter shows that despite the higher on-resistance of LV-JFET, its low voltage drop and current limiter feature can be interesting for protection applications. Tested BJT may require design improvements to show more stable results under SC to provide comparable data. MOSFETs show weak SC capability due to the proximity of metallic or dielectric layers with the hot-spot. However, they show good technological maturity, low on-resistance and advantageous gate driving compared to JFETs or BJTs.

We also showed the effect of the gate bias modulation on the SC capability for the JFET. We could see a notable improvement of critical SC time, which can be exploited in the protection scheme when SC is detected. This study also provides values and order of magnitude essential for more thorough studies and design of test bench.

### Acknowledgements

This study was funded by the French DGA under INSERE-HT project.

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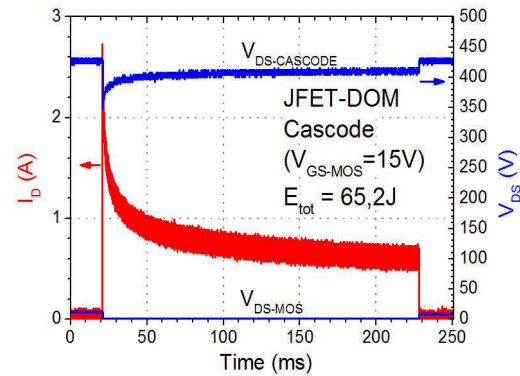


Fig. 7 - Short-circuit waveform on SiC current limiter with capacitive load